Demonstration of Technical & Economic Feasibility

Results are presented which demonstrate the technical and economic feasibility of backplane signaling at 5+ and 10+ Gigabits/second

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Xilinx
Goals of Technical Study

- Produce a representative set of backplanes that use currently available components and construction technology
- Characterize the backplanes’ performance capabilities
- Demonstrate transmission of signals using currently available, mainstream silicon product
Objectives of this Presentation

- Present a body of existing evidence, representative of the industry’s knowledge of backplane technology
- Demonstrate technical feasibility of 10Gbps NRZ Physical Electrical layer backplane communication
- Demonstrate that the proposed “Backplane Ethernet” is feasible
Presentation flow

- Backplanes analyzed
  - Matrix
  - Pictures
  - Descriptors
- Technical approach
  - Characterization
  - Signaling assumption – NRZ – least equalization
  - Simulation
  - Stat eye
  - Silicon signal
- Results
  - Picture
  - Shots of sim/stat eye/silicon
  - Conclusion for each
- Summary matrix – green squares for good
- Conclusions
Backplanes Characterized

- BP-A  XAUI Reference Design / Tyco HM-Zd / Nelco
- BP-D  Xilinx-designed / Teradyne GBX / Rogers
- BP-DF Xilinx-designed / Teradyne GBX / FR4
- BP-ER Xilinx-designed / ERNI 0XT / Rogers
- BP-E  Xilinx-designed / ERNI 0XT / FR4
- BP-F  Winchester-designed / SIP 1000 / Rogers
- BP-F20 Winchester-designed ATCA / SIP 1000-I / Rogers
- BP-F40 Winchester-designed ATCA / SIP 1000-I / Rogers
- BP-G  “Tier 1” Systems mfg / ERNI ERmet-Zd / Rogers
# Backplanes Studied

<table>
<thead>
<tr>
<th>Designator</th>
<th>Configuration</th>
<th>Connector</th>
<th>Designed by</th>
<th>Routing</th>
<th>Backplane Material, Layers</th>
<th>Line Card</th>
<th>Distances</th>
<th>Traces</th>
</tr>
</thead>
<tbody>
<tr>
<td>BP-A</td>
<td>XAU Reference Design</td>
<td>Tyco HM-zD</td>
<td>Tyco</td>
<td>Partial Route</td>
<td>0.185&quot;, Nelco 4000-2, Nelco =34 inch</td>
<td>2+30+2 =34 inch</td>
<td>8 pairs routed</td>
<td></td>
</tr>
<tr>
<td>BP-C</td>
<td>ATCA Platform</td>
<td>Tyco HM-zD</td>
<td>Kaparel PICMG</td>
<td>High Density, full route</td>
<td>0.220&quot;, Rogers Hybrid, 8 signal layers</td>
<td>FR4</td>
<td>3+20+3 =26 inch</td>
<td>W=8mil / S=8mil 55 pairs routed</td>
</tr>
<tr>
<td>BP-D</td>
<td>Full Mesh and Star</td>
<td>Teradyne GBX</td>
<td>Xilinx</td>
<td>High Density, full route</td>
<td>0.220&quot;, FR4, 8 signal layers</td>
<td>FR4</td>
<td>3+20+3 =26 inch</td>
<td>W=8mil / S=8mil 55 pairs routed</td>
</tr>
<tr>
<td>BP-DF</td>
<td>Full Mesh and Star</td>
<td>Teradyne GBX</td>
<td>Xilinx</td>
<td>High Density, full route</td>
<td>0.220&quot;, Rogers Hybrid, 8 signal layers</td>
<td>FR4</td>
<td>3+21+3 =27 inch</td>
<td>W=8mil / S=8mil, 8 signal layers, 40 pair (star) 16 pair (mesh) routed</td>
</tr>
<tr>
<td>BP-ER</td>
<td>Full Mesh and Star</td>
<td>ERNI 0xT</td>
<td>Xilinx</td>
<td>High Density, full route</td>
<td>0.265&quot;, Rogers Hybrid, 8 signal layers</td>
<td>FR4</td>
<td>3+21+3 =27 inch</td>
<td>W=8mil / S=8mil, 8 signal layers, 40 pair (star) 16 pair (mesh) routed</td>
</tr>
<tr>
<td>BP-E</td>
<td>Full Mesh and Star</td>
<td>ERNI 0xT</td>
<td>Xilinx</td>
<td>High Density, full route</td>
<td>0.225&quot;, Rogers Hybrid, 8 signal layers</td>
<td>FR4</td>
<td>3+21+3 =27 inch</td>
<td>W=8mil / S=8mil, 8 signal layers, 40 pair (star) 16 pair (mesh) routed</td>
</tr>
<tr>
<td>BP-F</td>
<td>Full Mesh and Star</td>
<td>Winchester SIP 1000</td>
<td>Winchester</td>
<td>Partial Route, Representative adjacent aggressors</td>
<td>Rogers Hybrid, Probe =34 inch</td>
<td>4+26+4 =34 inch</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BP-F20</td>
<td>ATCA Form Factor Selective Route</td>
<td>Winchester SIP 1000 I-Platform</td>
<td>Winchester</td>
<td>Partial Route, Representative adjacent aggressors</td>
<td>Rogers Hybrid, Rogers 20 inch</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BP-F40</td>
<td>ATCA Form Factor Selective Route</td>
<td>Winchester SIP 1000 I-Platform</td>
<td>Winchester</td>
<td>Partial Route, Representative adjacent aggressors</td>
<td>Rogers Hybrid, Rogers 40 inch</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BP-G</td>
<td>Dual Star</td>
<td>ERNI ERMET-zD</td>
<td>Tier 1 Customer</td>
<td>Actual application route</td>
<td>0.230&quot; Rogers Hybrid</td>
<td>Probe</td>
<td>3.5+15.5 +3.5 =22.5 Inch</td>
<td></td>
</tr>
</tbody>
</table>
Analysis Procedure

1. Measure Through and Crosstalk S-Parameters
2. Generate Linear Eq Parameters
3. Generate DFE Eq Parameters
4. Utilize Signal specifications from OIF and UXPi
5. Simulate in Time Domain
6. Plot Statistical Eye
7. Drive Backplane with silicon
8. Monitor Channel Output with Scope
EXAMPLE Results

Simulated Signal + X-Talk - after Linear Equalizer

10Gbps Signal from Xilinx Virtex-II Pro-X FPGA Measured Eye @ Channel Output, No Equalization

Stat Eye Signal + X-Talk - after DFE Equalizer

Stat Eye Signal + X-Talk - after Linear Equalizer
Comparison of Statistical Eye to Time Domain Eye

- Compare Simulated and Stat Eyes
  - with no Equalization,
  - no crosstalk.
  - 800 bits random data.
  - Sim hor. opening = 0.55 UI
  - Sim vert. opening = 0.3 units.

- Compare Simulated and Stat Eyes
  - Stat hor. opening (Q=8) = 0.51 UI
  - Stat vert. opening = 0.35 units.
### BP-A (XAUI / HM-Zd) Configuration

<table>
<thead>
<tr>
<th>Backplane</th>
<th>Config</th>
<th>Connector</th>
<th>Backplane Material</th>
<th>Lengths Inches</th>
<th>Traces</th>
<th>Vias</th>
</tr>
</thead>
<tbody>
<tr>
<td>BP-A XAUI</td>
<td>Reference Design</td>
<td>Tyco HM-Zd</td>
<td>Nelco 4000-2</td>
<td>2+30+2 =34 inch</td>
<td>Low Density, Partial Route</td>
<td>Thru vias, Not Backdrilled</td>
</tr>
</tbody>
</table>

#### Through

![Through Diagram](image1)

#### Crosstalk

![Crosstalk Graph](image2)

- `diagonal.txt`
- `horizontal.txt`
- `vertical.txt`

**Graph Details:**
- **X-Axis:** Frequency (Hz)
- **Y-Axis:** dB (S_{dd21})
BP-A (XAUI) 6Gbps Results

Simulated Signal + X-Talk - after Linear Equalizer

6.25Gbps Signal from Xilinx Virtex-II Pro-X FPGA
Measured Eye @ Channel Output

Stat Eye Signal + X-Talk - after DFE Equalizer

Stat Eye Signal + X-Talk - after Linear Equalizer
# BP-C (PICMG ATCA) Configuration

<table>
<thead>
<tr>
<th>Backplane</th>
<th>Config</th>
<th>Connector</th>
<th>Backplane Material</th>
<th>Lengths Inches</th>
<th>Traces</th>
<th>Vias</th>
</tr>
</thead>
<tbody>
<tr>
<td>BP-C</td>
<td>Standard Backplane</td>
<td>Tyco</td>
<td>HM-Zd</td>
<td>FR4</td>
<td></td>
<td>Thru vias, Not Backdrilled</td>
</tr>
</tbody>
</table>

**Through**

**PICMG Forward Transfer**

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>Magnitude (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$10^8$</td>
<td>-50</td>
</tr>
<tr>
<td>$10^9$</td>
<td>-40</td>
</tr>
<tr>
<td>$10^{10}$</td>
<td>-30</td>
</tr>
<tr>
<td>$10^{11}$</td>
<td>-20</td>
</tr>
</tbody>
</table>

**Crosstalk**

**PICMG Crosstalk Transfer**

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>$10^8$</td>
<td>-80</td>
</tr>
<tr>
<td>$10^9$</td>
<td>-60</td>
</tr>
<tr>
<td>$10^{10}$</td>
<td>-40</td>
</tr>
<tr>
<td>$10^{11}$</td>
<td>-20</td>
</tr>
</tbody>
</table>
BP-C (PICMG ATCA) Results – Layer 34

Simulated Signal + X-Talk - after Linear Equalizer

Signal from Xilinx Virtex-II Pro-X FPGA
Measured Eye @ Channel Output

Stat Eye Signal + X-Talk - after DFE Equalizer

Stat Eye Signal + X-Talk - after Linear Equalizer
# BP-D (Xilinx/GbX) Configuration

<table>
<thead>
<tr>
<th>Backplane</th>
<th>Config</th>
<th>Connector</th>
<th>Backplane Material</th>
<th>Lengths Inches</th>
<th>Traces</th>
<th>Vias</th>
</tr>
</thead>
<tbody>
<tr>
<td>BP-D</td>
<td>Concept Full Mesh and Star</td>
<td>Teradyne GBX</td>
<td>Rogers Hybrid (Daughters are FR4)</td>
<td>3+20+3 =26 inch</td>
<td>W=8mil / S=8mil, 8 signal layers, High Density, Full Route</td>
<td>Thru vias, Backdrilled</td>
</tr>
</tbody>
</table>

**Through**

![Through graph](image)

**Crosstalk**

![Crosstalk graph](image)
BP-D (Xilinx/GBX) Results

Simulated Signal + X-Talk - after Linear Equalizer

10Gbps Signal from Xilinx Virtex-II Pro-X FPGA Measured Eye @ Channel Output, No Equalization (this is actually from FR4 version of board)

10Gbps Signal from Xilinx Virtex-II Pro-X FPGA Measured Eye @ Channel Output, No Equalization (this is actually from FR4 version of board)

Stat eye unavailable

Stat Eye Signal + X-Talk - after DFE Equalizer

Stat Eye Signal + X-Talk - after Linear Equalizer
**BP-ER (Xilinx/0XT) Configuration**

<table>
<thead>
<tr>
<th>Backplane</th>
<th>Config</th>
<th>Connector</th>
<th>Backplane Material</th>
<th>Lengths Inches</th>
<th>Traces</th>
<th>Vias</th>
</tr>
</thead>
<tbody>
<tr>
<td>BP-ER</td>
<td>Concept Full Mesh and Star</td>
<td>ERNI 0XT</td>
<td>Rogers BP FR4 Line</td>
<td>3+21+3 =27 inch</td>
<td>W=8mil / S=8mil, 8 signal layers, High Density, Full Route</td>
<td>Thru vias, Backdrilled</td>
</tr>
<tr>
<td>Xilinx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Through**

Emi Rogers Through

**Crosstalk**

Emi Rogers Xtalk

-50  -40  -30  -20  -10  0  10  20  30  40  50

-100 -80 -60 -40 -20  0  20  40  60  80  100

-100 -80 -60 -40 -20  0  20  40  60  80  100

Frequency (Hz)  

Frequency (Hz)
BP-ER (Xilinx/0XT) Results

Simulated Signal + X-Talk - after Linear Equalizer

10Gbps Signal from Xilinx Virtex-II Pro-X FPGA
Measured Eye @ Channel Output, No Equalization

1

0 50 100 150 200

H-UI=.55
V-UI=.55

time, psec

Eye

Stat Eye Signal + X-Talk - after DFE Equalizer

Stat Eye Signal + X-Talk - after Linear Equalizer
# BP-E (Xilinx/0XT) Configuration

<table>
<thead>
<tr>
<th>Backplane</th>
<th>Config</th>
<th>Connector</th>
<th>Backplane Material</th>
<th>Lengths Inches</th>
<th>Traces</th>
<th>Vias</th>
</tr>
</thead>
<tbody>
<tr>
<td>BP-E</td>
<td>Concept Full Mesh and Star</td>
<td>ERNI 0XT</td>
<td>FR4 (Daughters are FR4)</td>
<td>3+21+3 =27 inch</td>
<td>W=8mil / S=8mil, 8 signal layers, High Density, Full Route</td>
<td>Thru vias, Backdrilled</td>
</tr>
<tr>
<td>Xilinx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## Through

### EMI Through

```
<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>10^8</td>
<td>0</td>
</tr>
<tr>
<td>10^9</td>
<td>-10</td>
</tr>
<tr>
<td>10^10</td>
<td>-20</td>
</tr>
<tr>
<td>10^11</td>
<td>-30</td>
</tr>
</tbody>
</table>
```

Through vias,

## Crosstalk

### Crosstalk

```
<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>10^8</td>
<td>0</td>
</tr>
<tr>
<td>10^9</td>
<td>-20</td>
</tr>
<tr>
<td>10^10</td>
<td>-40</td>
</tr>
<tr>
<td>10^11</td>
<td>-60</td>
</tr>
</tbody>
</table>
```

Crosstalk with:
- vert.txt
- horiz.txt
- diag.txt
BP-E (Xilinx/0XT) Results

Simulated Signal + X-Talk - after Linear Equalizer

10Gbps Signal from Xilinx Virtex-II Pro-X FPGA Measured Eye @ Channel Output, No Equalization

Stat Eye Signal + X-Talk - after DFE Equalizer

Stat Eye Signal + X-Talk - after Linear Equalizer

HUI=.50
VUI=.40

time, psec
## BP-F (Winchester/SIP) Configuration

<table>
<thead>
<tr>
<th>Backplane</th>
<th>Config</th>
<th>Connector</th>
<th>Backplane Material</th>
<th>Lengths Inches</th>
<th>Traces</th>
<th>Vias</th>
</tr>
</thead>
<tbody>
<tr>
<td>BP-F</td>
<td>Concept Selective Route</td>
<td>Winchester SIP</td>
<td>Rogers Hybrid (Daughters are FR4)</td>
<td>4+26+4 =34 inch</td>
<td>Low Density, Partial Route</td>
<td>Thru Vias, Backdrilled</td>
</tr>
</tbody>
</table>

### Through

**Winchester Forward Transfer**

- Length 34
- Length 30
- Length 26

### Crosstalk

**Gated Crosstalk**

- Frequency (Hz)
- Magnitude (dB)
BP-F (Winchester /SIP) Results

Simulated Signal + X-Talk - after Linear Equalizer

10Gbps Signal from Xilinx Virtex-II Pro-X FPGA
Measured Eye @ Channel Output

Eye

HUI=.55
VUI=.45

time, psec

Stat Eye Signal + X-Talk - after DFE Equalizer

Stat Eye Signal + X-Talk - after Linear Equalizer
# BP-F20 & F40 (Winchester/SIP) Configuration

<table>
<thead>
<tr>
<th>Backplane</th>
<th>Config</th>
<th>Connector</th>
<th>Backplane Material</th>
<th>Lengths Inches</th>
<th>Traces</th>
<th>Vias</th>
</tr>
</thead>
<tbody>
<tr>
<td>BP-F20 &amp; F40</td>
<td>Winchester</td>
<td>SIP1000-I</td>
<td>Rogers Hybrid</td>
<td>20 inches</td>
<td></td>
<td>Thru Vias, Backdrilled</td>
</tr>
<tr>
<td>Winchester</td>
<td></td>
<td></td>
<td></td>
<td>And 40 inches</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Diagram:**

- A close-up of a circuit board with traces and connections.
- Another view showing the backplane and connector setup.
BP-F20 (Winchester /SIP) Results

Simulated Signal + X-Talk  - after Linear Equalizer

10Gbps Signal from Xilinx Virtex-II Pro-X FPGA
Measured Eye @ Channel Output, No Equalization
8 Crosstalk Aggressors

Stat Eye Signal + X-Talk  - after DFE Equalizer

Stat Eye Signal + X-Talk  - after Linear Equalizer
BP-F40 (Winchester /SIP) Results

Simulated Signal + X-Talk - after Linear Equalizer

10Gbps Signal from Xilinx Virtex-II Pro-X FPGA Measured Eye @ Channel Output, No Equalization

Stat Eye Signal + X-Talk - after DFE Equalizer

Stat Eye Signal + X-Talk - after Linear Equalizer
# BP-G (Tier 1 Syst/ERmetZd) Configuration

<table>
<thead>
<tr>
<th>Backplane</th>
<th>Config</th>
<th>Connector</th>
<th>Backplane Material</th>
<th>Lengths Inches</th>
<th>Traces</th>
<th>Vias</th>
</tr>
</thead>
<tbody>
<tr>
<td>BP-G</td>
<td>Dual Star</td>
<td>ERNI ERmet-Zd</td>
<td>Rogers Hybrid</td>
<td>3.5+15.5+3.5=22.5&quot;</td>
<td></td>
<td>Thru Vias, Backdrilled</td>
</tr>
<tr>
<td>A “Tier 1” Syst Mfg</td>
<td></td>
<td></td>
<td>(Daughters are cable)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Through**

**Crosstalk**

![Through](image1)

![Crosstalk](image2)
BP-G (Tier 1/ERmetZd) Results

Simulated Signal + X-Talk - after Linear Equalizer

10Gbps Signal from Xilinx Virtex-II Pro-X FPGA Measured Eye @ Channel Output

Eye 1

HUI=.55
VUI=.45

time, psec

Stat Eye Signal + X-Talk - after DFE Equalizer

Stat Eye Signal + X-Talk - after Linear Equalizer
Conclusions

- The backplanes shown have been, and can be built using presently available technology.
- 10Gbps serial communication is demonstrated over multiple connectors.
- Channels are driven with actual production 10Gbps silicon.
- Basic 10Gbps NRZ signaling works over the backplanes studied.
- Both Linear and DFE equalization work over the backplanes studied.