Method to reduce DS jitter in EPoC

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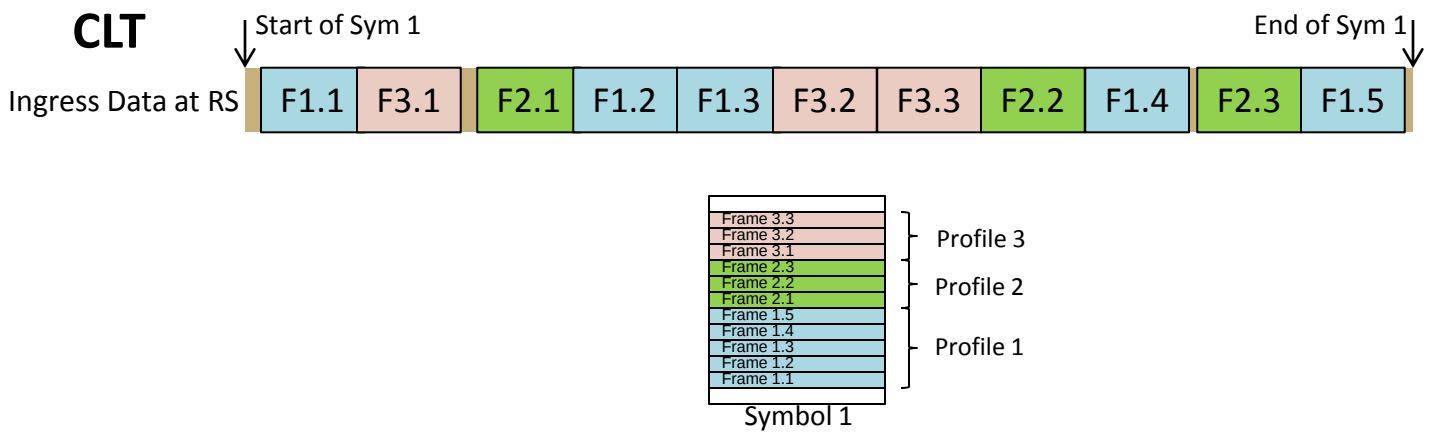
Supporters

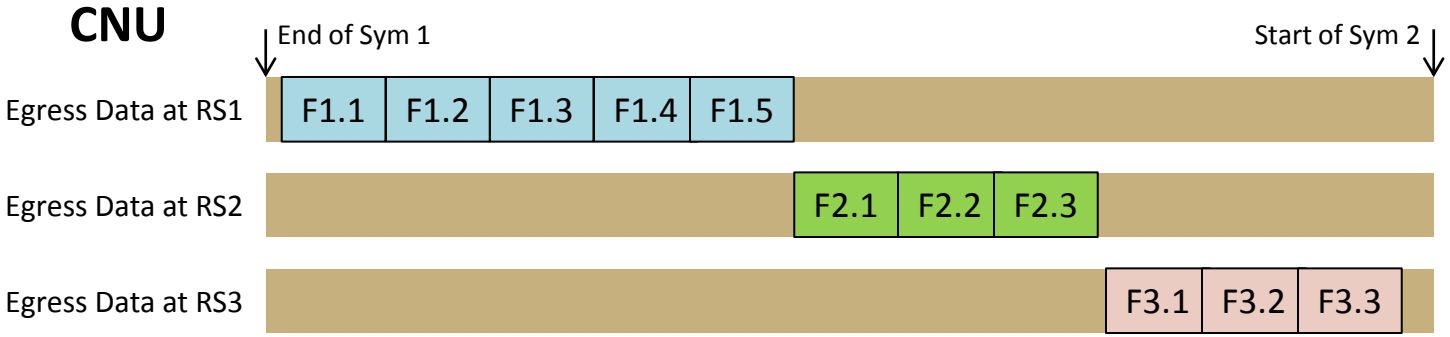
Problem

- With multiple profiles in the DS path the play-out of frames at the receiver may experience excessive jitter

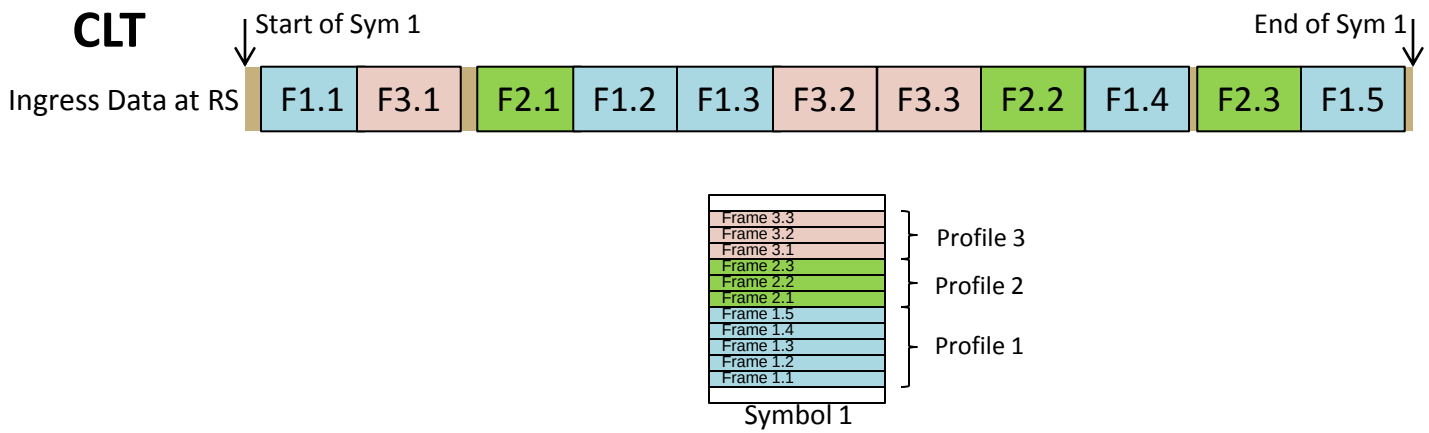
MMP Frame play-out



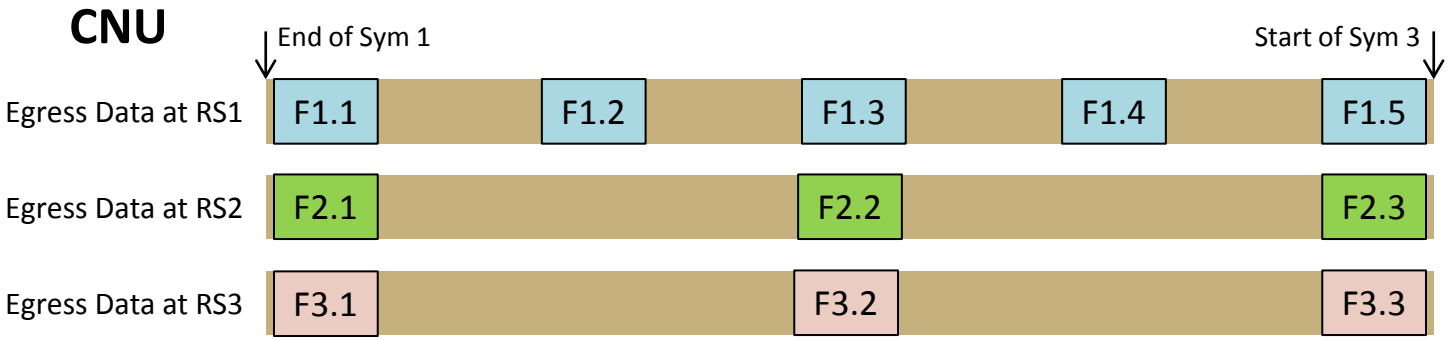
If play-out is relative to beginning of Symbol



MMP Frame play-out

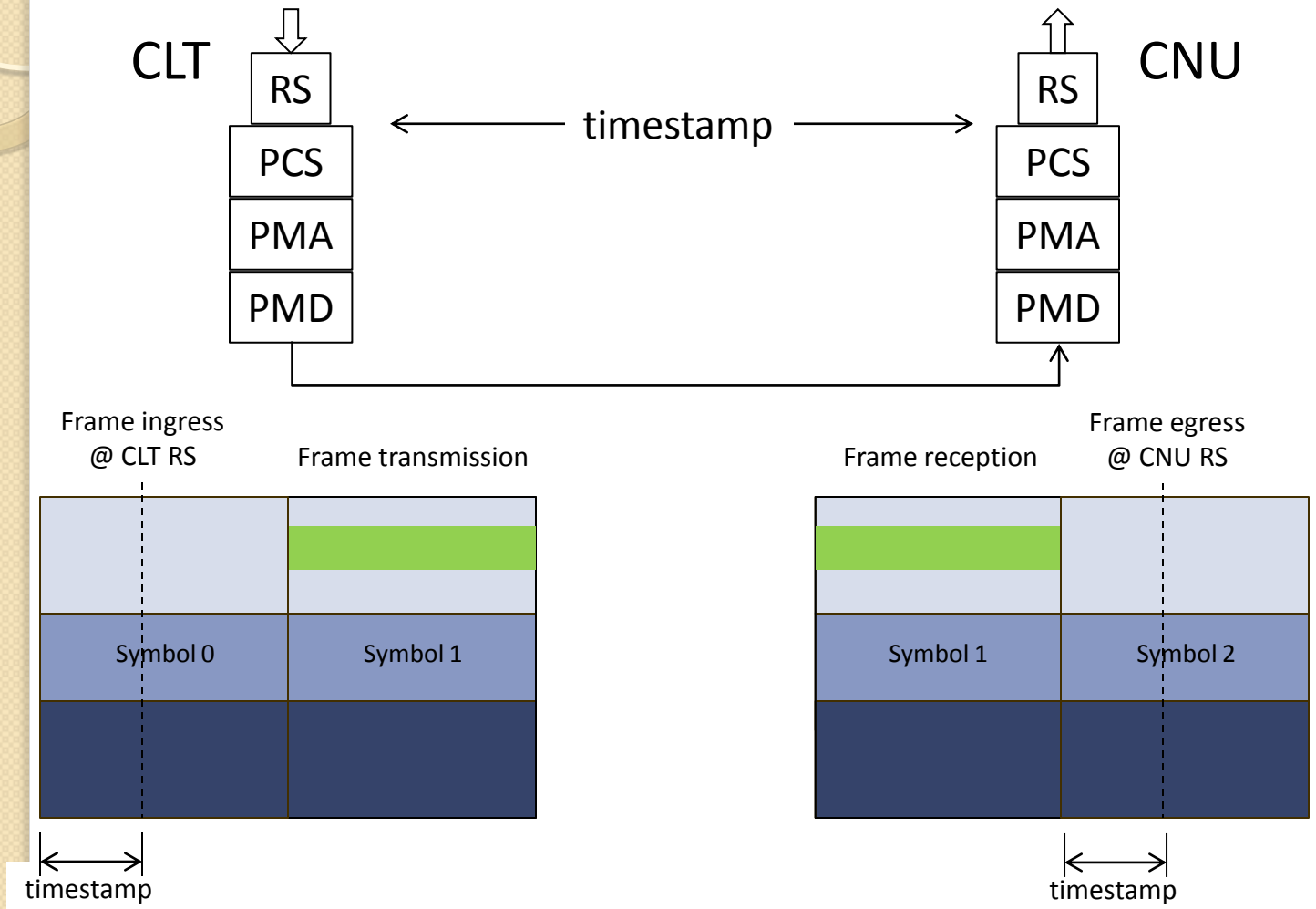


If play-out is relative to beginning of Profile

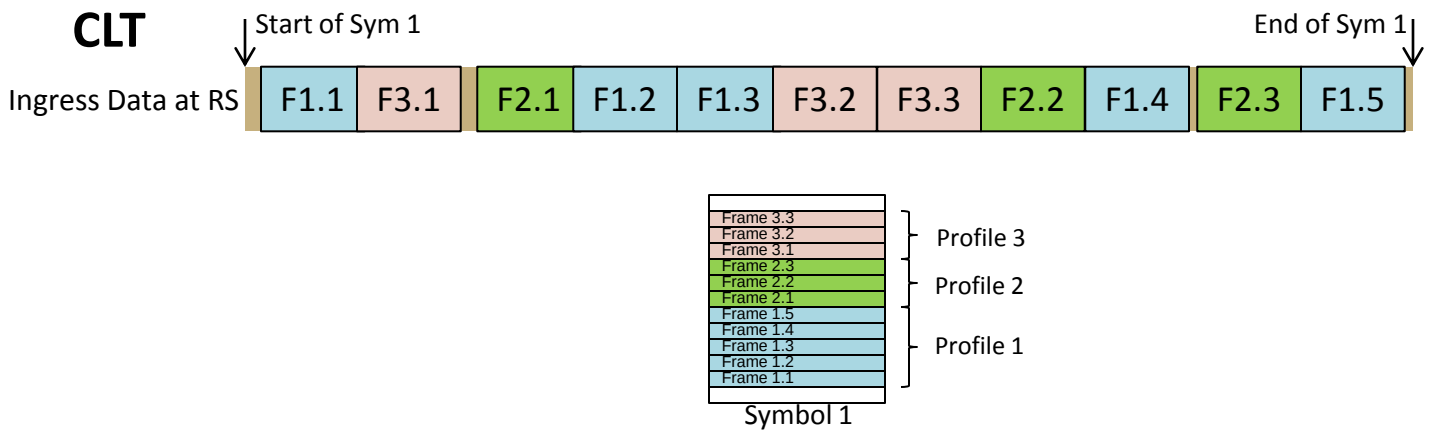


Solution - Basic idea

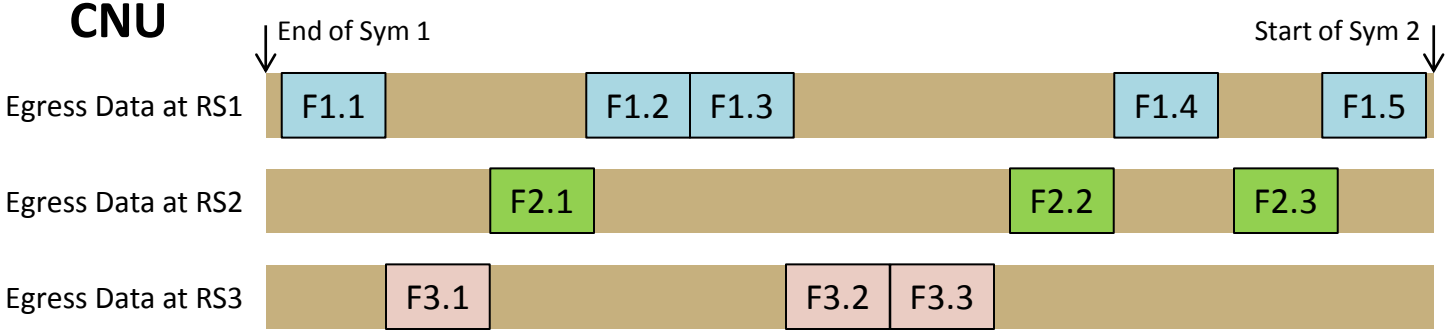
- At CLT input to the PHY (RS) add a timestamp to each frame relative to the beginning of the current symbol
- At the CNU RS delay the output of each frame towards the MAC relative to the beginning of symbol boundary by an amount equal to the timestamp
- This guarantees a delay of exactly (within bounds of timestamp clock) two symbol periods in the PHY
  - 1 Symbol buffer on transmit
  - 1 Symbol buffer on receive


CLT
RS
PCS
PMA
PMD
timestamp
RS
PCS
PMA
PMD
CNU
Frame ingress
@ CLT RS
Frame transmission
Frame reception
Frame egress
@ CNU RS
Symbol 0
Symbol 1
Symbol 1
Symbol 2
timestamp
timestamp

MMP Frame play-out



Desired Play-out having a timestamp from start of frame would minimize jitter



Timestamp details

- Base timestamp on TQ clock from start of symbol
  - Then counter length is less than 12 bits (assuming symbol time <65 us)
  - Co
    (in

Table 76–3—Preamble/SFD replacement mapping

Column	Lane	Field	Preamble/SFD	Modified preamble/SFD
0	0	—	0x55	Same
	1	—	0x55	Same
	2	SLD	0x55	0xd5
	3	—	0x55	Same
1	0	—	0x55	Same
	1	LLID[15:8]	0x55	<mode, logical_link_id[14:8]>[a]
	2	LLID[7:0]	0x55	<logical_link_id[7:0]>[b]
	3	CRC8	0xd5	The 8 bit CRC calculated over column 0 lane 2 through column 1 lane 2

Questions?

THANK YOU!