EPoC ICI analysis

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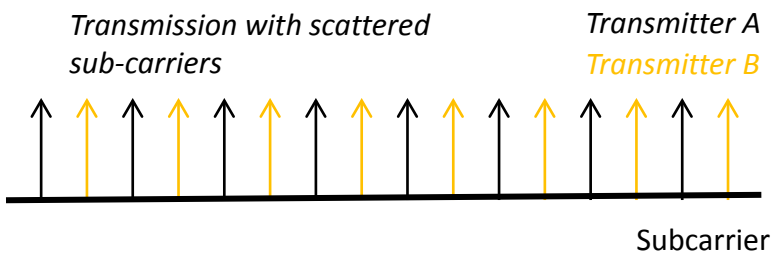
Background & Motivation

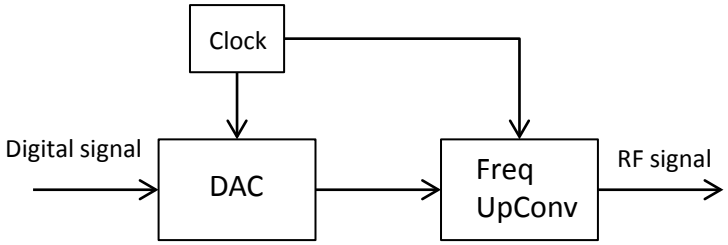
- **Tone Reordering (see remein_3bn_02_0513)**
  - Interleave sub-carriers from multiple transmitters to level capacity between them
- **Upstream Probing (see rahman_syed_3bn_02a_0513)**
  - Probe multiple CNUs simultaneously

Members of the group questioned if Inter Carrier Interference (ICI) would be an issues with multiple closely interleaved transmitters as proposed in the above presentations

ICI due to simultaneous transmission

- **Investigated ICI due to staggered sub-carriers from two transmitter as shown below**
  - 25 kHz spacing (worst case)
- **Two error components due to clock differences at DAC & Frequency Up Converter cause**
  - Sampling error
  - Carrier frequency offset

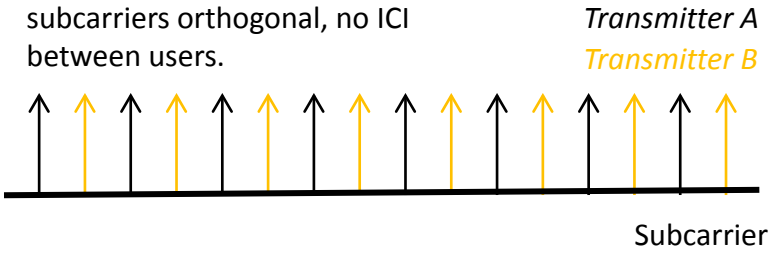




ICI due to simultaneous transmission

- **With multiple transmitters two clock may be slightly out of frequency**
- **Here we assume transmitter A is the reference and transmitter B contributes interference**

Clock well synchronized for users, subcarriers orthogonal, no ICI between users.

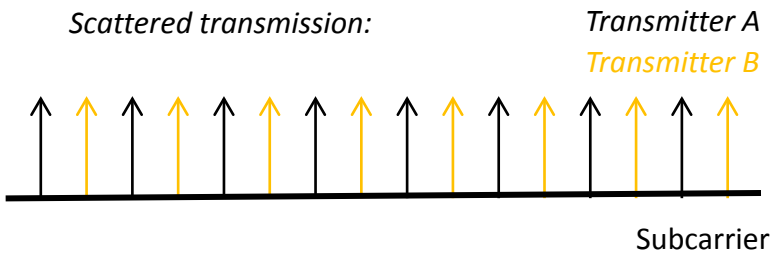


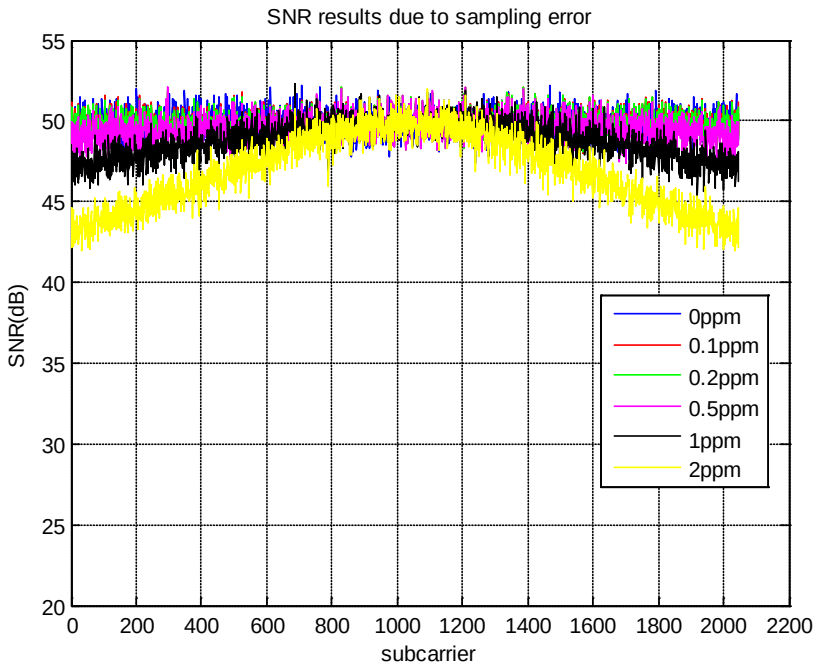
Clock error will cause carrier frequency offset between users, orthogonality will be affected, leading to interference

ICI impact – Sampling error

- **Analyzed ICI due to Sampling Error;**
- **-50dBc AWGN noise compared to receive signal level**
- **Simulated a constant clock error, the results show the ICI impact as SNR loss**
- **The simulation is based on 25KHz sub-carrier spacing (worst case)**

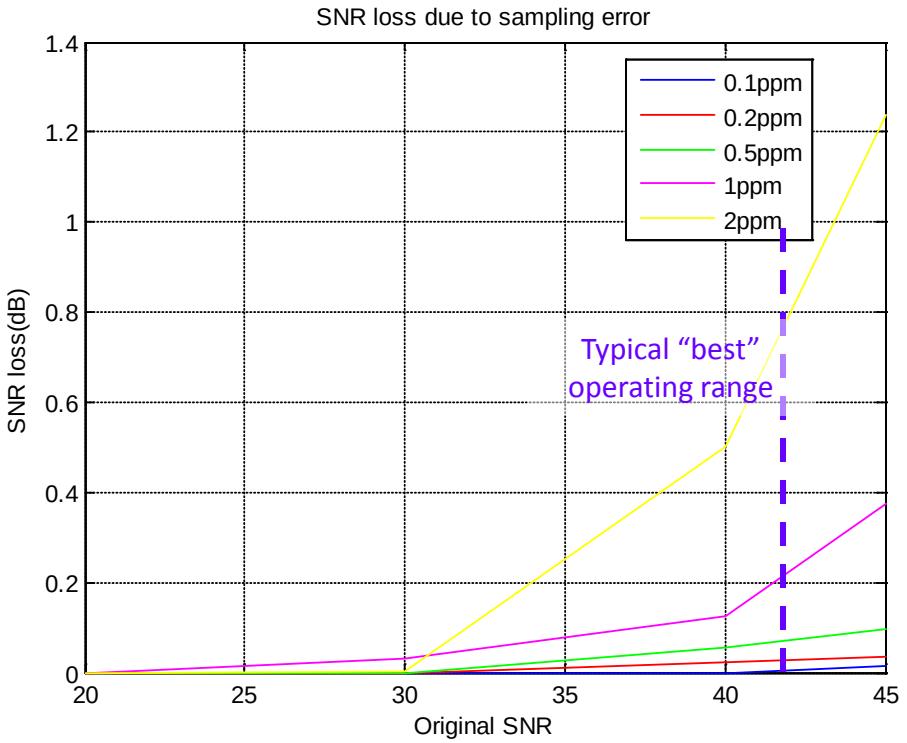
Clock error (ppm)	Average SNR Loss (dB)
0	0
0.1	0.02
0.2	0.05
0.5	0.31
1	1.06
2	2.94





ICI impact – Sampling error

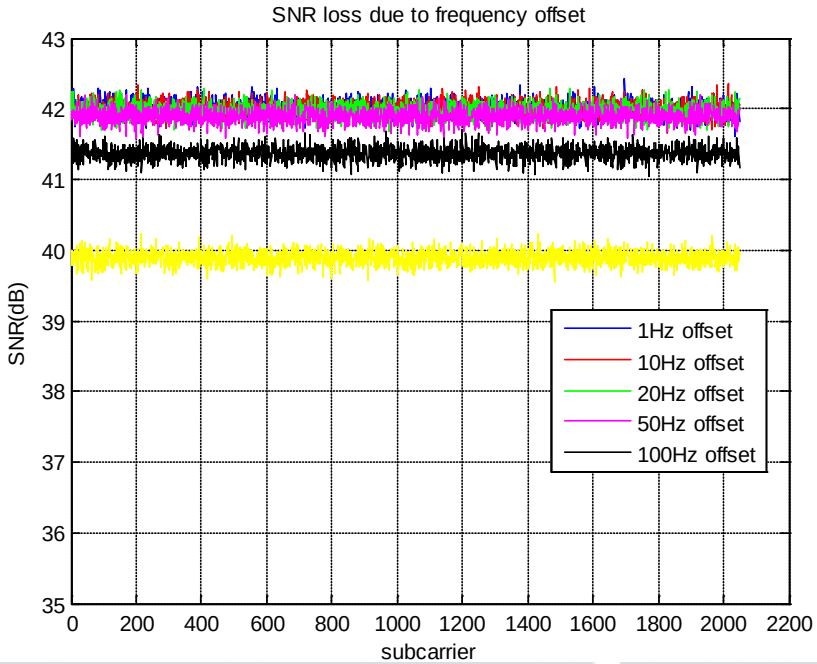
- **SNR loss due to sampling error versus original SNR for several clock accuracies**
- **Related to original SNR**
  - A higher SNR results in a larger impact
- **When original SNR is smaller than 42dB and clock error is less than 1ppm, the average loss is less than 0.3dB**



ICI impact – Carrier Frequency Offset

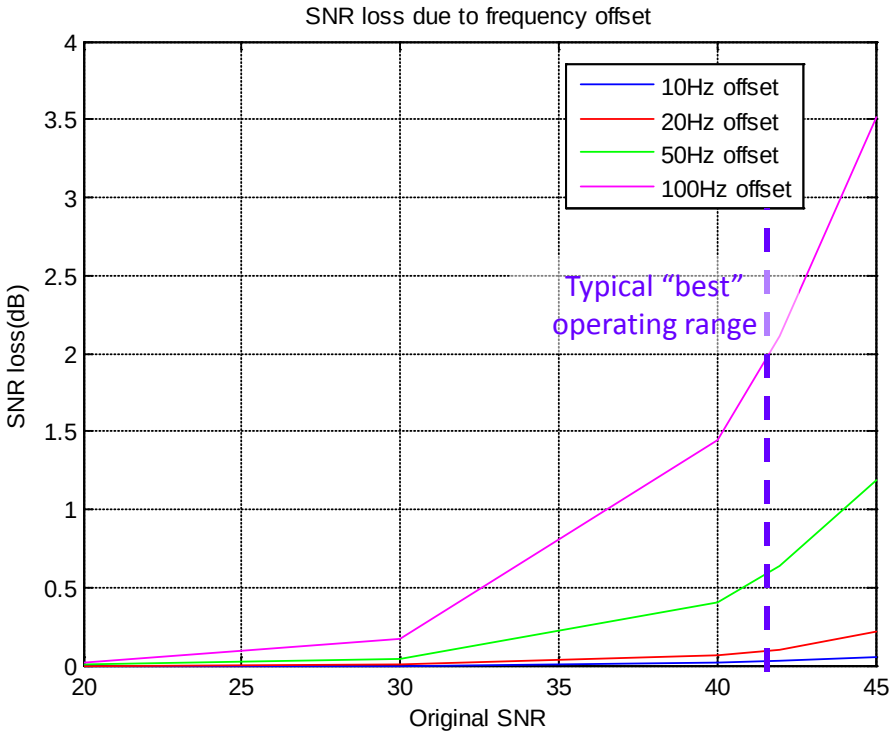
- **Analysis of the ICI impact due to Carrier Frequency Offset (CFO) ;**
- **Simulation for 42dB SNR, (sufficient for 12 b/Hz loading), near maximum possible SNR**
- **At an SNR of 42dB a 50Hz CFO will lead to <3/4 dB SNR loss**

CFO(Hz)	SNR Loss (dB)
1	0
10	0.0271
20	0.1030
50	0.6317
100	2.1100



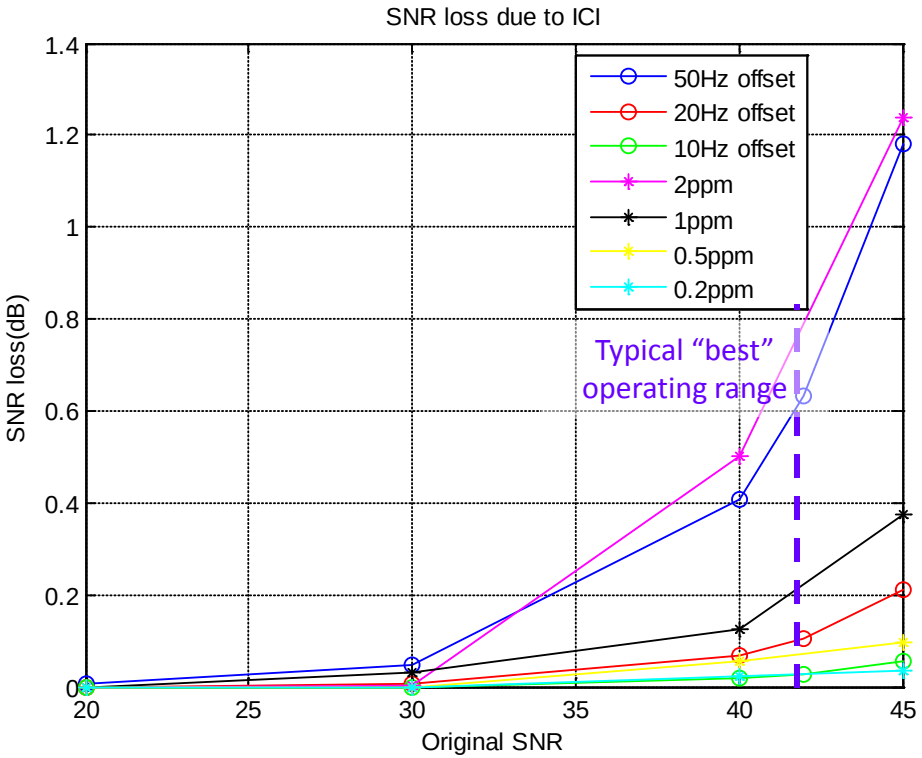
ICI impact – Carrier Frequency Offset

- **SNR loss vs SNR due to various CFO levels**
- **With CFO ≤50Hz and SNR ≤ 42 dB loss is ≤ 0.6 dB**
- **CFO depends on the clock error and frequency upconversion**
  - CFO=clock error*frequency up-conversion
  - Ex 0.5ppm*100MHz=50Hz



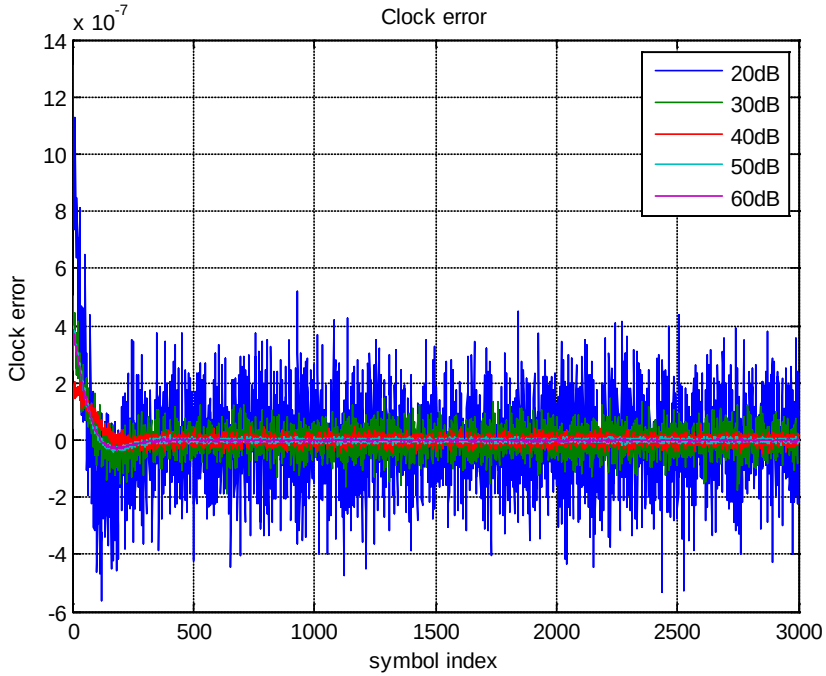
Analysis

- **Comparing SNR loss from sampling error and frequency up-conversion**
- **From graph we see that the impact of 50Hz CFO and 2ppm sampling error are ~0.1 dB different.**
- **25MHz*2ppm=50Hz, which means**
  - When frequency upconversion is equal to 25MHz, the impact of the two are about equal
  - At >25MHz, the impact of CFO is larger
  - At <25MHz, the impact of sampling error is larger



Downstream timing synchronization

- **Downstream timing synchronization is mainly impacted by the AWGN noise**
- **Figure shows synchronization results at various AWGN levels**
- **Clock error (standard deviation) after synchronization is 0.0021-0.1496ppm when SNR is 20-60dB, and decreases rapidly as SNR increases**
- **Clock error should be <<0.5ppm**



AWGN (dB)		20	30	40	50	60
Clkerr (ppm)	Std	0.1496	0.0462	0.0147	0.0049	0.0021

Conclusions

(1 of 2)

- **The supported RF bandwidth of an upstream channel shall be 192 MHz (Motion 10), frequency up-conversion for upstream is above 100MHz, so in most cases the impact of CFO is dominant**
- **With < 50Hz CFO (0.5ppm clock error) and an original SNR <42dB, SNR loss is less than 0.6dB (previous slide)**
  - 42dB SNR:
    - From the SNR distribution diagram (ref. 1 for downstream, upstream is worse than that), very few CM can get SNR more than 42dB;
    - 42dB SNR has > 6dB margin at 4096QAM modulation with LDPC code;
  - 0.5ppm clock error:
    - At 100MHz frequency up-conversion, 50Hz offset = 0.5ppm clock error
    - After synchronization is complete, very little clock error (CFO) will be left, in most cases it will be <<0.5ppm, for example, if downstream band is at 300MHz, 0.5ppm = 150Hz CFO, and will lead to 2-9dB SNR loss for downstream
  - 0.6dB SNR loss
    - Less than 0.6dB SNR loss is simulated with 0.5ppm clock error, this value decreases with a smaller clock error
    - SNR loss improves quickly as clock error decreases, for example **when clock error is 0.2ppm, SNR loss is only 0.1dB.**

(1) “Motivations for Investigating Multiple MCS for EPoC”, schmitt_01a_1112

Conclusion

- **From this analysis, we recommend:**
  1. Short term clock tolerance of 0.5ppm or better
     - If consider low/mid split, the tolerance can be higher, such as 2ppm or 1ppm
  2. Tone Reordering would not be significantly impacted by ICI and should be adopted
  3. Multiple simultaneous probing would not be significantly impacted by ICI and should be adopted

Thank you

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25 vs 50 kHz spacing

- **25 kHz is the worse case, the impact of CFO is clearly much larger than 50kHz**