UPDATE TO DOWNSTREAM FREQUENCY INTERLEAVING AND DE-INTERLEAVING FOR OFDM

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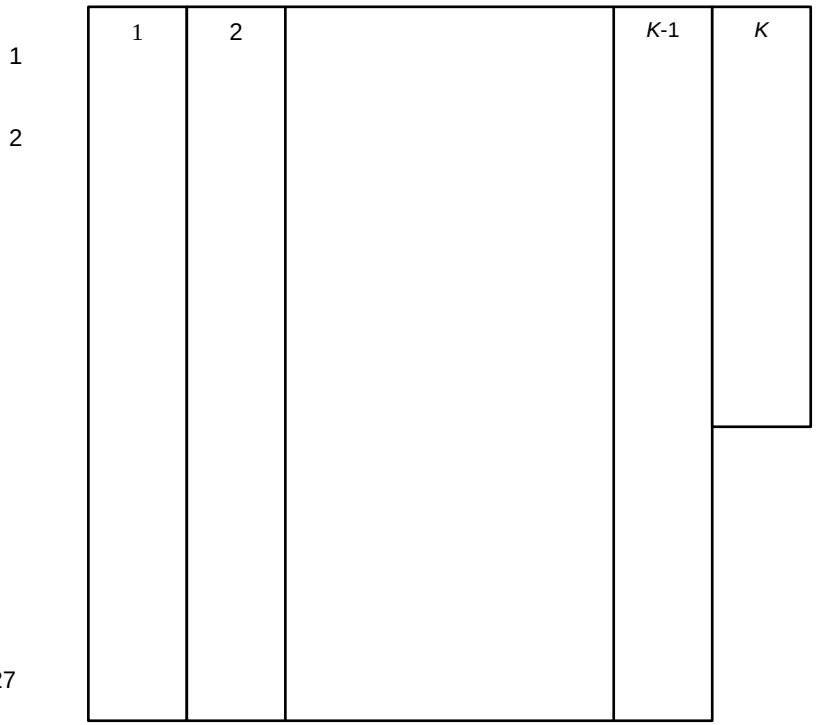
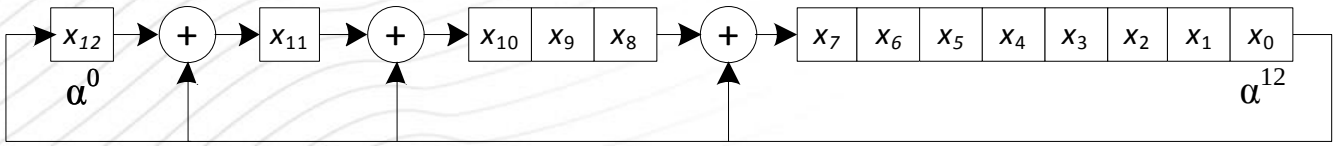
CURRENT FREQUENCY INTERLEAVER

- 2-D store
- 127 rows and *K* columns
- N_I data subcarriers and scattered pilots
- $K = ceil(\frac{N_I}{127})$
- $C = N_I - 127(K-1)$ subcarriers in the last column
- *x*[12:6] row address
- *x*[5:0] column address

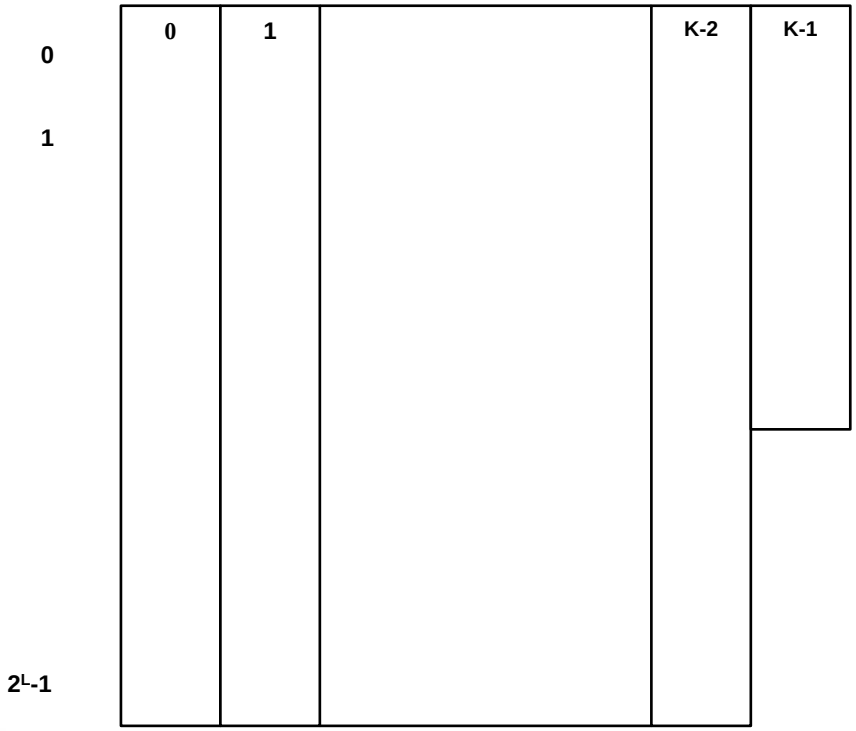
- *Multiple clock cycles per subcarrier*
- *4K (127 by 32) lookup table for the de-interleaver*



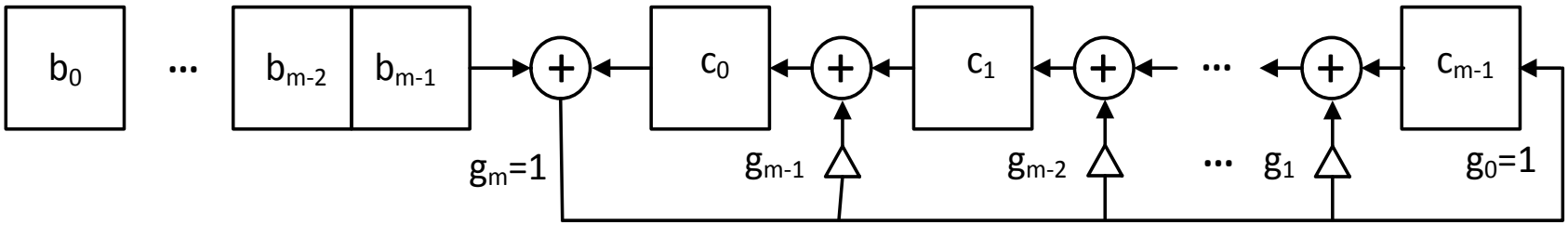


TWO-DIMENSIONAL STORE BLOCK STRUCTURE

- 2-D store
- 2^L rows and K columns
- L and K are chosen depending on FFT size
- N_I data subcarriers and scattered pilots
- $K = ceil(\frac{N_I}{2^L})$
- $C = N_I - 2^L(K-1)$ subcarriers in the last column



CRC ADDRESS GENERATOR

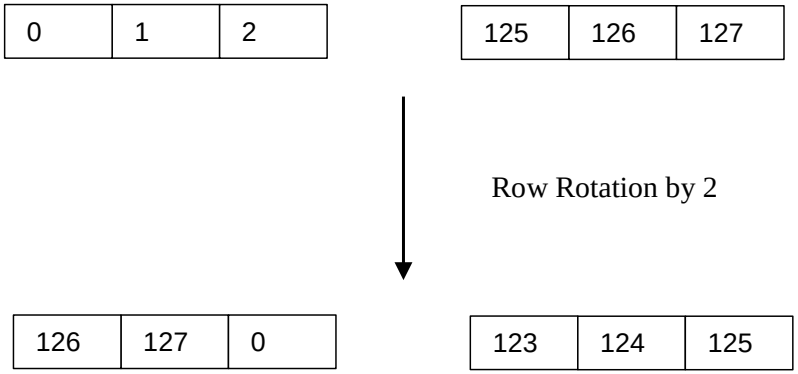


- **m-stage linear feedback shift register (LFSR) for calculating the CRC of each row address**
- **Defined using a primitive generator polynomial of degree m = L:**
  $$G(X) = g_m X^m + g_{m-1} X^{m-1} + g_{m-2} X^{m-2} + \bullet\bullet\bullet + g_2 X^2 + g_1 X^1 + g_0$$
- **Finite (Galois) field GF[2]: g_k = 0 or 1**
- **Input sequential row address b_{m-1}, b_{m-2}, …, b_1, b_0**
- **Output permuted row address = CRC value c_{m-1}, c_{m-2}, …, c_1, c_0**

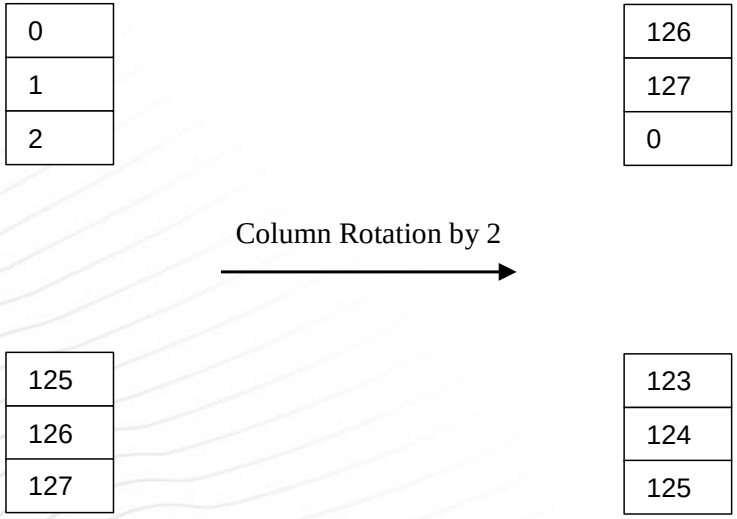
FREQUENCY INTERLEAVING PROCESS

- **Write successive consecutive subcarriers into the 2-D store in the row given by the L bit CRC value of each L bit row address.**
- **Rotate the subcarriers in each row written by the same L bit CRC value of the row address modulo the number of columns in that row (either modulo K for a row below C or modulo K-1 for row C and higher) using a right circular shift.**
- **Rotate the subcarriers in each column by the L bit CRC value of [K-1 minus the column address] using a downward circular shift. Note that the last column K-1 with a CRC value of 0 in not rotated.**
- **Read the subcarriers out of the 2-D store column-wise from row 0, column 0 to row C-1, column K-1.**

ROW AND COLUMN ROTATION



(a)



(b)

- **Permuted output subcarrier number in the 2-D store in row r, column c as sc(r,c) given by:**

$$sc(r,c) = sc_0\left[\left(r - CRC(K-c)\right) mod\ 2^L\right] + \left(c - \left(r - CRC(K-c)\right) mod\ 2^L\right) mod\ M,$$

$$where\ M = \begin{cases} K, for\ \left(r - CRC(K-c)\right) mod\ 2^L < C \\ K-1, otherwise \end{cases}$$

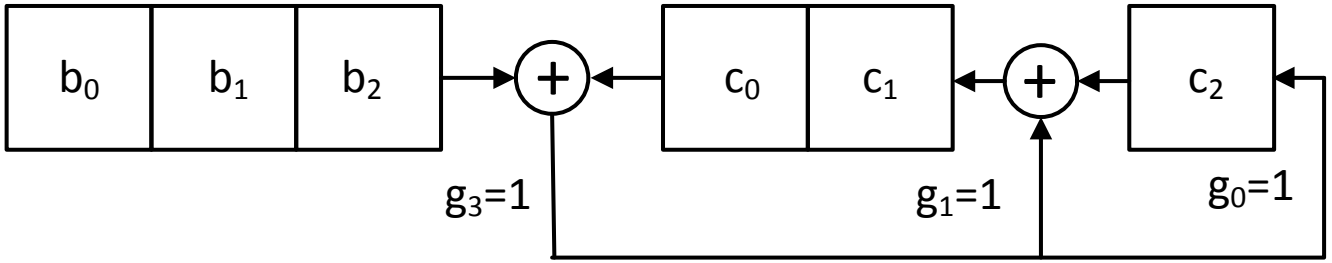
- **$sc_0[n]$ is an array of 2^L elements where each element contains the cumulative number of subcarriers previously written into the 2-D store**
  - Represents the starting (i.e. lowest) subcarrier number in a permuted row
- **Note that if the last column contains fewer subcarriers than 2^L, the cumulative value in $sc_0[n]$ takes into account those previously written permuted output rows that were shorter by one subcarrier**
- ***Large 2-D store Lookup Table is not needed***
- ***Direct calculation without variable number of clock cycles***

FREQUENCY DE-INTERLEAVING PROCESS

- **Write the subcarriers into the 2-D store column-wise from column 0, row 0 to column K-1, row C.**
- **Rotate the subcarriers in each column by the L bit CRC value of [K-1 minus the column address] using an upward circular shift (reverse of interleaver). Note that the last column K-1 with a CRC value of 0 in not rotated.**
- **Rotate the subcarriers in each row written by the same L bit CRC value of the row address modulo the number of columns in that row (either modulo K for a row below C or modulo K-1 for row C and higher) using a left circular shift (reverse interleaver).**
- **Read the subcarriers out of the 2-D store row-wise in the row order given by the L bit CRC value of each L bit row address skipping the last column at or beyond row C.**

64-Point Subcarrier Example

CRC ADDRESS GENERATOR



- **3-stage linear feedback shift register (LFSR) for calculating the CRC of each row address**
- **Defined using a primitive generator polynomial of degree 3:**

$$G(X) = X^3 + X^1 + 1$$

- **Input sequential row address b_2 , b_1, b_0**
- **Output permuted row address = CRC value c_2 , c_1, c_0**

NON-INTERLEAVED SUBCARRIERS

Read ROW	Column 0 Subcarrier	Write ROW	Column 0 Subcarrier	COLUMN: Rotation:	0 0	1 0	2 0	3 0	4 0	5 0	6 0	7 0
0				0	0	8	16	24	32	40	48	56
1				0	1	9	17	25	33	41	49	57
2				0	2	10	18	26	34	42	50	58
3				0	3	11	19	27	35	43	51	59
4				0	4	12	20	28	36	44	52	60
5				0	5	13	21	29	37	45	53	61
6				0	6	14	22	30	38	46	54	62
7				0	7	15	23	31	39	47	55	63

ROW-COLUMN (SYSTEMATIC) BLOCK INTERLEAVER

Read ROW	Column 0 Subcarrier	Write ROW	Column 0 Subcarrier	COLUMN: Rotation:	0 0	1 0	2 0	3 0	4 0	5 0	6 0	7 0
0	0	0	0	0	0	1	2	3	4	5	6	7
1	8	1	8	0	8	9	10	11	12	13	14	15
2	16	2	16	0	16	17	18	19	20	21	22	23
3	24	3	24	0	24	25	26	27	28	29	30	31
4	32	4	32	0	32	33	34	35	36	37	38	39
5	40	5	40	0	40	41	42	43	44	45	46	47
6	48	6	48	0	48	49	50	51	52	53	54	55
7	56	7	56	0	56	57	58	59	60	61	62	63

CRC ROW ADDRESS WRITE AND ROTATE

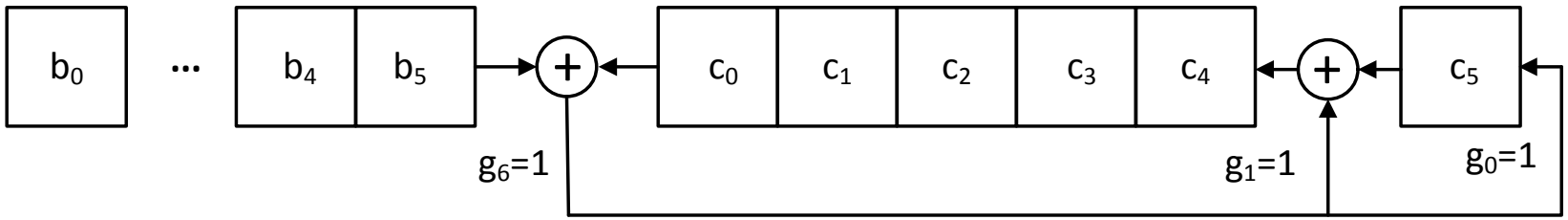
Read ROW	Column 0 Subcarrier	Write ROW	Column 0 Subcarrier	COLUMN: Rotation:	0 0	1 0	2 0	3 0	4 0	5 0	6 0	7 0
0	0	0	0	0	0	1	2	3	4	5	6	7
1	40	6	8	6	47	40	41	42	43	44	45	46
2	56	3	16	3	62	63	56	57	58	59	60	61
3	16	5	24	5	21	22	23	16	17	18	19	20
4	48	7	32	7	52	53	54	55	48	49	50	51
5	24	1	40	1	27	28	29	30	31	24	25	26
6	8	4	48	4	10	11	12	13	14	15	8	9
7	32	2	56	2	33	34	35	36	37	38	39	32

CRC ROW ADDRESS WRITE AND ROTATE PLUS COLUMN ROTATE

Read ROW	Column 0 Subcarrier	Write ROW	Column 0 Subcarrier	COLUMN: Rotation:	0 2	1 4	2 1	3 7	4 5	5 3	6 6	7 0
0	0	0	0	0	10	53	35	42	17	24	60	7
1	40	6	8	6	33	28	2	57	48	15	19	46
2	56	3	16	3	0	11	41	16	31	38	50	61
3	16	5	24	5	47	34	56	55	14	5	25	20
4	48	7	32	7	62	1	23	30	37	44	8	51
5	24	1	40	1	21	40	54	13	4	59	39	26
6	8	4	48	4	52	63	29	36	43	18	6	9
7	32	2	56	2	27	22	12	3	58	49	45	32

EPoC Frequency Interleaver

CRC ADDRESS GENERATOR



- **6-stage linear feedback shift register (LFSR) for calculating the CRC of each row address**
- **Defined using a primitive generator polynomial of degree 6:**

$$G(X) = X^6 + X^1 + 1$$

- **Input sequential row address b_5, b_4, b_3 , b_2 , b_1, b_0**
- **Output permuted row address = CRC value c_5, c_4, c_3 , c_2 , c_1, c_0**

EPoC INTERLEAVER OUTPUT (PARTIAL)

# Subcarriers	3745
# Rows	64
# Columns	59
Last Column	33

Read ROW	Column 0 Subcarrier	Write ROW	Column 0 Subcarrier	COLUMN: Rotation:	0 44	1 4	2 52	3 22	4 38	5 14	6 62	7 26	8 42
0	0	0	0	0	390	350	283	2944	3020	2821	2870	3186	3262
1	1930	48	59	48	2319	2162	2212	1130	1089	1007	939	1372	1331
2	2866	24	117	24	3254	3097	3147	3410	3486	3287	3336	201	160
3	936	40	176	40	1323	1283	1216	1596	1555	1473	1405	2013	2089
4	3334	12	234	12	152	1	3731	659	618	536	468	2948	3024
5	1404	60	293	1	2081	1930	1799	2471	2547	2348	2456	1134	1093
6	468	20	351	20	3016	2924	862	72	3658	3517	3625	3414	3490
7	2398	36	410	36	1085	993	2791	1884	1843	1703	1694	1600	1559
8	3568	6	468	6	3482	3390	392	2819	906	766	757	663	622
9	1638	54	527	54	1551	1459	2321	1005	2718	2578	2686	2475	2551
10	702	30	585	30	614	522	3256	3285	436	296	287	76	3662
11	2632	46	644	46	2543	2451	1325	1471	2248	2108	2216	1888	1847
12	234	10	702	10	3654	3620	154	534	3183	3043	3151	2823	910
13	2164	58	761	58	1839	1689	2083	2346	1369	1229	1220	1009	2722
14	3100	18	819	18	902	752	3018	3515	198	5	3735	3289	440
15	1170	34	878	34	2714	2681	1087	1701	2010	1934	1803	1475	2252

CONCLUSION

- **Complexity, timing and large memory size issues in the current frequency interleaver implementation**
  - Variable number of multiple clock cycles per subcarrier address
  - Large 4K (127 by 32) element lookup table for the de-interleaver
- **A new random (non-systematic) frequency interleaver shown**
  - CRC value of each L bit row input address for row write address permutation
- **Rotation of both rows and columns to prevent periodicity**
  - Pseudo-random subcarrier frequency dispersion
  - Non-systematic random ordering of subcarriers across entire spectrum
- **Significantly lower complexity implementation**
  - Large lookup table avoided with direct calculation
  - Time varying address generation avoided with direct calculation

Thank You