PHY High Level Block Diagrams – R03
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(work in progress)

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As presented in September 2013:

EPoC Downstream Transmitter Block Diagram (starting point)

NOTE: All digital domain
EPOC Downstream CLT Transmitter Block Diagram

NOTE: All digital domain
NOTE: Sub-Carrier Configuration includes sub-carrier use and QAM mapping
NOTE: Not converted yet to IEEE 802 Vertical Form
All New R02 (in progress):

Still needed:
Framing, burst builder,
Probing, ranging, markers

Assumption: Upstream PLC will be similar to downstream, with added functionality to control bursts separate from data

EPoC Upstream CNU Transmitter Block Diagram

NOTE: All digital domain
NOTE: Sub-Carrier Configuration includes sub-carrier use and QAM mapping
NOTE: Not converted yet to IEEE 802 Vertical Form
All New R02 (in progress):

Does scrambler go before FEC? 1D-to-2D subcarrier assignment, etc. TDD functionality

EPoC Upstream CNU Transmitter Block Diagram

NOTE: All digital domain
NOTE: Sub-Carrier Configuration includes sub-carrier use and QAM mapping
NOTE: Not converted yet to IEEE 802 Vertical Form
Upstream
Summary

- Downstream CLT Transmitter near complete
- Upstream CNU Transmitter
  - Work in progress
- Needed: PHY path block delays
  - Work in progress
THANK YOU