Single Wavelength 112Gb/s PAM4 Transmission Over 10km SSMF Using a 1.3μm EML

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Objectives

- To investigate the link power budget of a 112Gb/s PAM4 over 10km link by using post-DSP only, or both pre- and post-DSP
# 102~112Gb/s PAM-4 Experiments

<table>
<thead>
<tr>
<th>Reference</th>
<th>Link distance</th>
<th>TX output power (dBm)</th>
<th>ROP @ BER=1e-3</th>
<th>Optical TX</th>
<th>DAC+ Driver Amp BW</th>
<th>RX 3-dB BW</th>
<th>Waveform capture &amp; off-line Equalizer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stasser_3bs_01_0714</td>
<td>2 km</td>
<td>+3.3dBm</td>
<td>-7.5 dBm</td>
<td>EML 32GHz 6dB ER</td>
<td>PPG + driver (32GHz)</td>
<td>40Gb/s</td>
<td>80GS/s DSO (analog BW=33GHz), FFE (16 taps)</td>
</tr>
<tr>
<td>Bhatt_3bs_01_0714</td>
<td>2, 10 km</td>
<td>+0.8dBm</td>
<td>3.8e-3 @ -5.3dBm</td>
<td>SiP MZI 19GHz</td>
<td>DAC (15GHz) + driver (27GHz)</td>
<td>33GHz</td>
<td>DSO (2-ch)</td>
</tr>
<tr>
<td>Mazzini_3bs_0814 (ad hoc)</td>
<td>2.2 km</td>
<td>+?dBm</td>
<td>-8.5 dBm (estimated)</td>
<td>LN MZI 35GHz</td>
<td>PPG with No driver</td>
<td>33GHz</td>
<td>160 Gsps DSO (analog BW=63GHz), FFE (22 taps)</td>
</tr>
<tr>
<td>Hirai_3bs_01_0714</td>
<td>0 km</td>
<td>+5 dBm</td>
<td>-6 dBm</td>
<td>LN MZI (? GHz)</td>
<td>DAC (15GHz) + driver</td>
<td>33GHz</td>
<td>100GS/s ADC (~200 taps) Nyquist Shaping</td>
</tr>
<tr>
<td>Way_3bs_01_0914</td>
<td>10 km</td>
<td>+6.5dBm</td>
<td>(I) -5 dBm (II) -6 dBm</td>
<td>EML 32GHz 7.4dB ER</td>
<td>AWG + driver (31GHz)</td>
<td>40GHz</td>
<td>160 Gsps DSO (analog BW=63GHz), (I) post FFE (21 taps); (II) pre-FFE (19 taps)+post-FFE (21 taps)</td>
</tr>
</tbody>
</table>

Total end-to-end link budget of 10~12.3 dB (2 (MUX) + 2 (DEMUX) + 4 or 6.3 (channel) + 2 (TDP)) needs to be met.
Single-wavelength 112Gb/s PAM-4 Experiment (I)  
Post-DSP Only
Single-wavelength 112Gb/s PAM-4 Experiment (II) Pre- and Post-DSP

- Offline PAM4 DSP (FFE, 19 taps)
- 56GS/s AWG (6dB BW = 23GHz)
- Linear Driver (31GHz)
- 1314 nm EML (32GHz) +6.5dBm
- 10km SSMF
- VOA
- PIN/TIA
- Received Optical Power
- 160GSPS/63GHz real-time scope
- Offline PAM4 DSP (FFE, 21 taps)

Graph showing BER vs. ROP (dBm) with 10 km and OBTB traces.
# 112Gb/s PAM4 Experiment Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAC 6dB bandwidth</td>
<td>23</td>
<td>GHz</td>
</tr>
<tr>
<td>DAC ENOB within 6dB bandwidth</td>
<td>&gt; 4.5</td>
<td>bits</td>
</tr>
<tr>
<td>Driver amplifier 3dB bandwidth</td>
<td>31</td>
<td>GHz</td>
</tr>
<tr>
<td>EML 3dB bandwidth</td>
<td>32</td>
<td>GHz</td>
</tr>
<tr>
<td>Extinction ratio</td>
<td>7.4 (4.7 with pre-DSP)</td>
<td>dB</td>
</tr>
<tr>
<td>PIN/TIA 3dB bandwidth</td>
<td>40</td>
<td>GHz</td>
</tr>
<tr>
<td>Receiver input spectral noise density</td>
<td>≤ 40</td>
<td>pA/√Hz</td>
</tr>
<tr>
<td>Receiver responsivity @ 1314nm</td>
<td>0.4</td>
<td>A/W</td>
</tr>
<tr>
<td>ADC bandwidth</td>
<td>63</td>
<td>GHz</td>
</tr>
<tr>
<td>ADC ENOB (up to 30GHz)</td>
<td>&gt; 5</td>
<td>bits</td>
</tr>
</tbody>
</table>
Practical Product Challenges

• Signal Integrity
  – 112Gb/s PAM4 transmission among PAM4 chip, drivers, and TOSA/ROSA with FPC, could incur signal integrity degradation at the junctions of these components and at PCB traces.
  – Success of co-packaging of PAM4 die, driver die, and E/O & O/E dies remains to be proven

• ADC
  – Can CMOS-based ADC perform as well as instrument-level ADC (they are not based on CMOS today)?

• Uncooled CWDM versus Cooled LAN-WDM
  – Link power budget is too tight to tolerate CWDM optical performance
    • More optical power fluctuation penalty
    • More optical fiber dispersion penalty
Summary

- Depending on various penalty factors that need to be added, and depending on what the pre-FEC threshold is, the link power budget is tight for 112Gb/s PAM4 over 2km, and even tighter for over 10km

- In this experiment, there is still room for improvement on
  - Receiver responsivity (0.4A/W → > 0.6A/W)
  - Receiver spectral noise density (40 pA/√Hz → < 25~30 pA/Hz)
  - Receiver bandwidth (40GHz → 32~35GHz)

- Pre- and post-DSP help improve the receiver sensitivity @ BER=1e-3 by 1~1.5dB in comparing to the case of post-DSP only, achieving a total end-to-end budget of 12.5dB