

CHANNEL OPERATING MARGIN (COM) PROPOSAL FOR CDAUI-8



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■ SUPPORTERS

- **Demonstrate a DFE-LESS Receive Architecture for Channel Compliance**
- **Why DFE-LESS?**
 - DFE less - No Error-Propagation and related MTTFPA Concerns
 - Lower Power, Simpler implementation
- **Methodology:**
 - Use the public-domain Simulation Tool (COM) and Channels
 - Establish a base-line to match previously published results
 - DFE based implementation: [healey_3bs_01_0315](#)
 - Obtain Simulation results with DFE-less Channel Compliance configuration
- **Proposed Configuration:**
 - No DFE, 2nd Post-cursor in the TX, Modified CTLE, and a 2nd Low-frequency CTLE

- http://www.ieee802.org/3/bs/public/14_07/mellitz_3bs_01_0714.pdf (11-July-14)
 - Rich Mellitz, Intel
 - Chip-to-Chip (w/ mezzanine) channels
 - Channels 1 to 7
 - IL: 7, 9, 11, 15, 17, 2 x19dB @13.28GHz
 - XT: 4FEXT, 3NEXT

- http://ieee802.org/3/bs/public/channel/TEC/shanbhag_02_0914.pdf (30-Sep-14)
 - Megha Shanbhag, Nathan Tracy, TE Connectivity
 - Medium reach/Chip-to-chip channel using a single connector (Armor)
 - IL: 19.1dB @13.28GHz
 - XT: 7FEXT, 0 NEXT

- Start with CAUI-4 COM configuration (as in [healey 3bs 01 0315](#))
- Set the number of signal levels $L = 4$, $DER_0 = 1E-06$, and $fb = 26.5625Gb$
- Set $Add = 0.02UI$ and $SNR_TX = 31dB$
- Increase CTLE range (-15 to 0 in steps of 1) and set DFE tap range = [1 0.2 0.2 0.2 0.2]
- Reduce R_LM to 0.92
- Package model:
 - 'Designed Package' used in [healey 3bs 01 0315](#) provides approx. 2dB improvement
 - In this case, we tweaked the package parameters to obtain improvement in the same ball park
 - $Rd = 50\text{ Ohms}$, $Cp = 1.15e-04\text{ nF}$, and $Cd = 1.5e-04\text{ nF}$

- Channel operating margin (COM) for the baseline configuration

Test Case	1	2	3	4	5	6	7	8
Insertion Loss (dB) at fb/2	19.2	14.34	7.22	18.93	17.24	11.14	9.24	18.75
healey_3bs_01_0315 (final pass)	1.16	2.22	2.41	1.09	0.65	2.04	2.09	2.2
Baseline for this implementation	-0.03	0.96	1.52	0.23	-0.02	1.25	1.19	1.73

- The resulting baseline is on average about 1dB worse
- Package parameters can be tweaked further to improve the baseline to obtain a closer match. But feasibility needs further investigation.

GO DFE-LESS & ADD 2ND POST-CURSOR

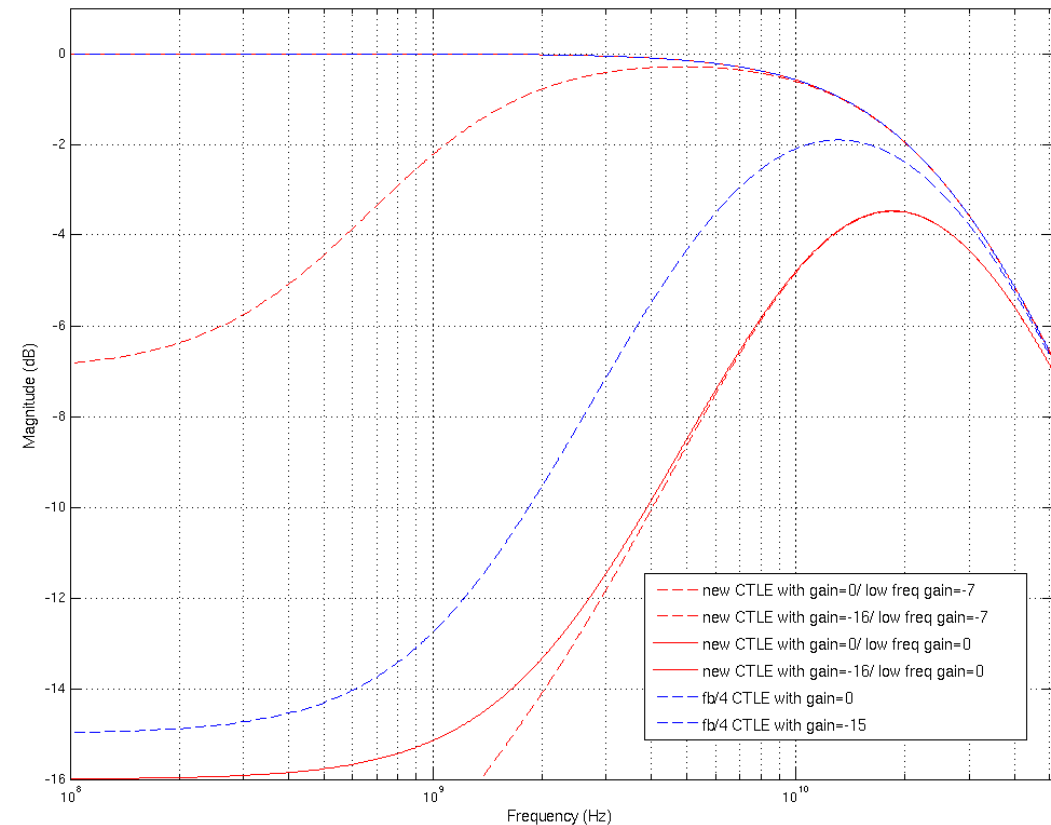
- Take away the DFE (set Nb = 0), Set DER0 = 1.3E-04 (No Fear of Error Propagation)
 - 1.3E-04 represents 4 links cascaded

Test Case	1	2	3	4	5	6	7	8
healey_3bs_01_0315 (final pass)	1.16	2.22	2.41	1.09	0.65	2.04	2.09	2.2
This implementation	-2.31	0.2	2.79	-2.58	-1.50	1.58	1.9	-0.68

- Add 2nd post-cursor to TX-FIR:

Test Case	1	2	3	4	5	6	7	8
This implementation	-1.43	1.53	3.32	-1.54	-0.12	2.49	2.47	0.89

- Increase CTLE b/w to fb/2
- A 2nd pole-zero pair is introduced at 1G (CTLE-LOW)
 - Configuration is similar to the main CTLE
 - DC gain range set to [-7:0] dB
- Relax SNR_TX to 29dB
- Increase level-mismatch Ratio to 0.95



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healey_3bs_01_0315	1.16	2.22	2.41	1.09	0.65	2.04	2.09	2.2
Baseline with DFE	-0.03	0.96	1.52	0.23	-0.02	1.25	1.19	1.73
Set Nb=0 (no DFE) & DER0 =1.3E-04	-2.31	0.2	2.79	-2.58	-1.50	1.58	1.9	-0.68
Add 2 nd post cursor in TX-FFE	-1.43	1.53	3.32	-1.54	-0.12	2.49	2.47	0.89
Modified CTLE +TX_SNR and R_LM adjust.	0.473	2.15	3.34	0.74	1.03	2.95	2.96	3.15

- The final results are comparable to Implementation with DFE

- **Proposed a feasible DFE-less receive architecture:**
 - No Error-propagation/MTTFPA Concerns
 - Simpler implementation/Lower Power
- **COM values greater than 2dB possible on several Channels**
- **Required enhancements needed to COM to accommodate the proposed architecture are extensions of existing features**
- **Package Models have a significant impact on overall link performance**