Electrical Interface Ad-hoc Meeting

- Opening/Agenda/Work-items

IEEE P802.3bs 400Gb/s Ethernet Task Force
8th February 2016

Opening

- The charter of the Electrical Interface Ad hoc is:
  - Address all issues in relation to the electrical interfaces to ensure progress towards a technically complete draft.
    - *Identify issues or omissions in the draft*
    - *Find consensus now, rather than in comment resolution.*
- Next Ad-hoc Meeting
  - 15th February
- Attendees names and affiliations will be taken from the Webex participants list.
  - Please use an e-mail address indicating affiliation when signing in. If you attend via phone only, or if your employer and affiliation are different, please send me an e-mail.

Patent Policy

- http://www.ieee802.org/3/patent.html

Agenda

Ad-hoc Opening/Agenda	Andre Szczepanek	szczepanek_01_020816_elect
Electrical Ad Hoc Work-Items	Andre Szczepanek	szczepanek_01_020816_elect

Agenda & Minutes

- Any objections to the Agenda ?
- Any objections to the minutes from the last meeting ?
  - http://www.ieee802.org/3/bs/public/adhoc/elect/01Feb_16/minutes_draft_01-Feb_2016_elect.pdf

Electrical Ad Hoc Work-Items

& Straw Poll results

120E Pattern generator characteristics table proposals

- Proposal #1 : CAUI-4 C2M like:

Parameter	Value
Total Jitter (pk-pk)	0.28 UI
Random Jitter (pk-pk)	0.15 UI
Max even-odd jitter (pk-pk)	0.017 UI

Per CAUI-4 C2M

Per KP4/OIF-56G-VSR-PAM4

- Proposal #2 : C2C and VSR-PAM4 like
  - Define Jitter as “Clock jitter” per C2C and VSR-PAM4, and use Clause 94.3.12.6.1 measurement method

Parameter	Value
Clock Random Jitter RMS (max)	0.01 UI
Clock Deterministic jitter pk-pk (max)	0.04 UI
Max even-odd jitter (pk-pk)	0.019 UI

Per CDAUI-4 C2C Tx TP0a

Straw Poll results

- I support a CAUI-4 C2M like definition of pattern generator jitter for the Host & Module stressed input test procedures
  - 2
- I support a CDAUI-8 C2C TP0a like definition of pattern generator (clock) jitter for the Host & Module stressed input test procedures
  - 4

Comments received on Straw Poll

- Tables 120E-6/8 only specify the initial starting point for pattern generator calibration
  - The Rj must subsequently be adjusted to meet the Eye width and eye height targets
  - “The purpose of this table is to get the mix of high and low probability and EO jitter roughly right.”
- Annex 120D uses the 94.3.12.6.1 method for specifying Clock Jitter, but the method proposed by Adam Healey in healey_3bs_01_0915.pdf is better.

Proposed Editors comment

- Remove Tables 120E–6, & 120E–8
- Change
  - “Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates a jitter profile given in Table 120E–6”
- to
  - “Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates the CDAUI-8 C2C Output jitter profile given in Table 120D–1”
- Change
  - “Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates a jitter profile given in Table 120E–8”
- to
  - “Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates the CDAUI-8 C2C Output jitter profile given in Table 120D–1”

Issues deferred by comment resolution

- R_{LM} measurement method
- SNR_{TX}/SNDR values
- Allow for use of a module transmitter TXFIR in eye measurement method
- Additional Jitter tolerance measurement frequencies
- CRU Bandwidth
- Improvements to 120D (C2C) output Jitter measurement methodology

Backup

Participants, Patents, and Duty to Inform

All participants in this meeting have certain obligations under the IEEE-SA Patent Policy.

- **Participants [Note: Quoted text excerpted from IEEE-SA Standards Board Bylaws subclause 6.2]:**
  - **"Shall inform the IEEE (or cause the IEEE to be informed)" of the identity of each "holder of any potential Essential Patent Claims of which they are personally aware" if the claims are owned or controlled by the participant or the entity the participant is from, employed by, or otherwise represents**
  - **"Should inform the IEEE (or cause the IEEE to be informed)" of the identity of "any other holders of potential Essential Patent Claims" (that is, third parties that are not affiliated with the participant, with the participant's employer, or with anyone else that the participant is from or otherwise represents)**
- **The above does not apply if the patent claim is already the subject of an Accepted Letter of Assurance that applies to the proposed standard(s) under consideration by this group**
- **Early identification of holders of potential Essential Patent Claims is strongly encouraged**
- **No duty to perform a patent search**

Patent Related Links

All participants should be familiar with their obligations under the IEEE-SA Policies & Procedures for standards development.

Patent Policy is stated in these sources:

IEEE-SA Standards Boards Bylaws

http://standards.ieee.org/develop/policies/bylaws/sect6-7.html#6

IEEE-SA Standards Board Operations Manual

http://standards.ieee.org/develop/policies/opman/sect6.html#6.3

Material about the patent policy is available at

http://standards.ieee.org/about/sasb/patcom/materials.html

If you have questions, contact the IEEE-SA Standards Board Patent Committee Administrator at patcom@ieee.org or visit http://standards.ieee.org/about/sasb/patcom/index.html

This slide set is available at https://development.standards.ieee.org/myproject/Public/mytools/mob/slideset.ppt

Call for Potentially Essential Patents

- If anyone in this meeting is personally aware of the holder of any patent claims that are potentially essential to implementation of the proposed standard(s) under consideration by this group and that are not already the subject of an Accepted Letter of Assurance:
  - Either speak up now or
  - Provide the chair of this group with the identity of the holder(s) of any and all such claims as soon as possible or
  - Cause an LOA to be submitted