



Chip To Module Twin Axial Cable Channels For 400 Gb/s: Re-examining the Insertion Loss Equation

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Supporters

- ▶ Adee Ran - Intel
- ▶ Howard Heck - Intel
- ▶ Mike Dudek – Cavium
- ▶ Piers Dawe – Mellanox
- ▶ Rick Rabinovich- IXIA
- ▶ Upen Reddy Kareti – Cisco
- ▶ Yasuo Hidaka - Fujitsu

Agenda

- ▶ Topology
- ▶ Simulation Results
- ▶ Issue
- ▶ Recommendation

Board Layout for Chip to Module Designs are Challenging

- ▶ Routing density is one challenge for a high radix switch device or a large BGA device.
- ▶ The routing loss budget of 7.5 dB to the QSFP connector might require the best of the best PCB material or retimers
- ▶ There may be other ways to extend channel reach and work with the tight loss budget

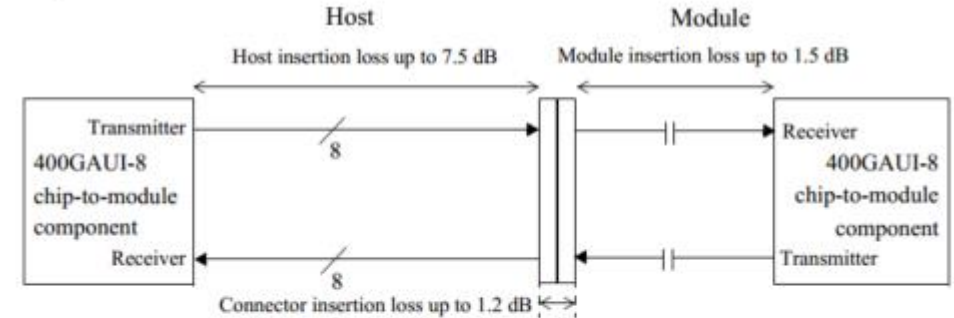


Figure 120E-3—400GAUI-8 chip-to-module insertion loss budget at 13.28 GHz

The nominal signaling rate for each lane is 26.5625 Gb/s. The chip-to-module interface is defined using a specification and test methodology that is similar to that used for CEI-56G-VSR-PAM defined in OIF-CEI-04.x [B55a].

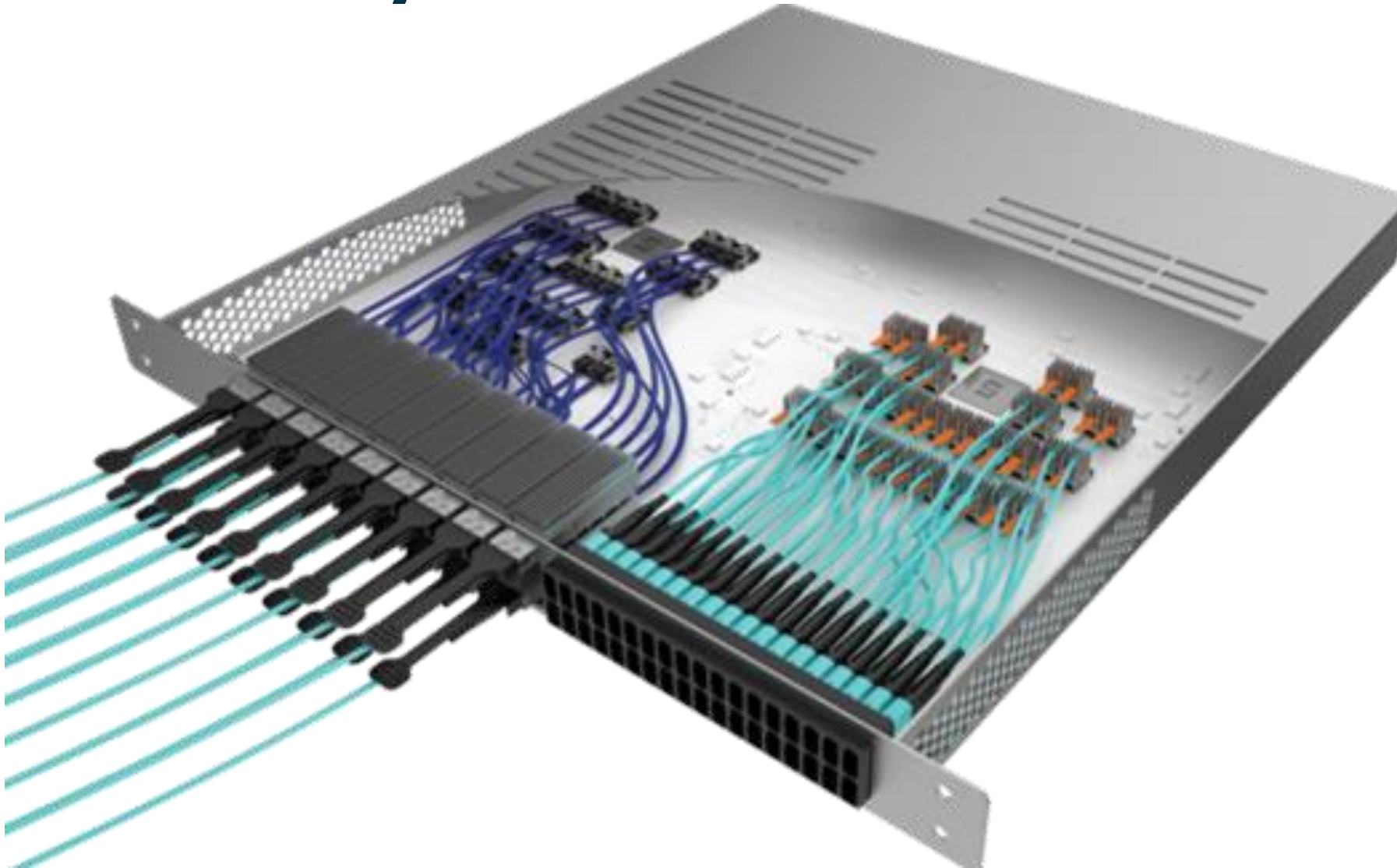
$$\text{Insertion_loss}(f) \leq 0.0801 + 0.5736\sqrt{f} + 0.6046f \quad (\text{dB}) \quad (120E-1)$$

for $0.01 \leq f \leq 26.5625$

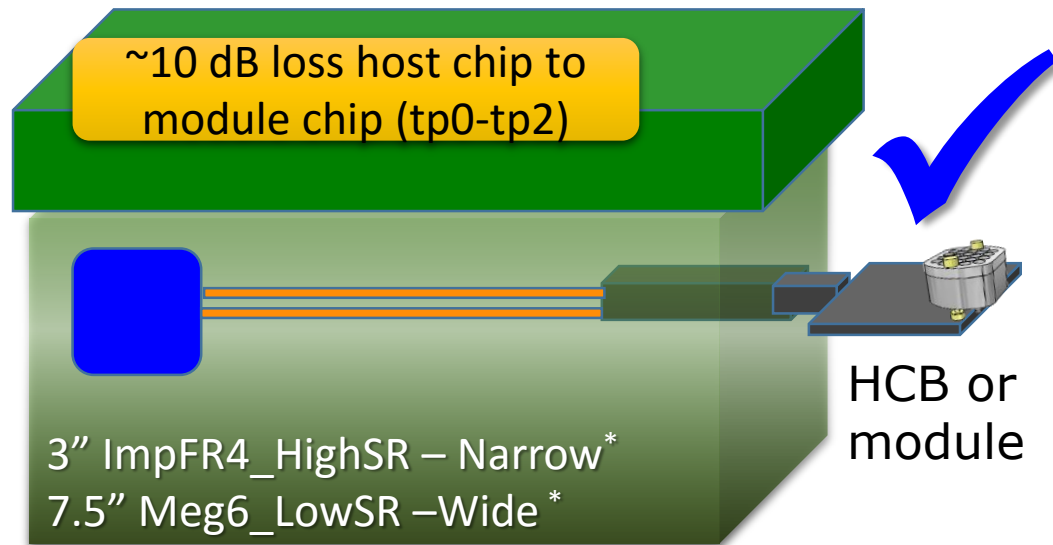
where

f is the frequency in GHz
 $\text{Insertion_loss}(f)$ is the 200GAUI-4 or 400GAUI-8 chip-to-module insertion loss

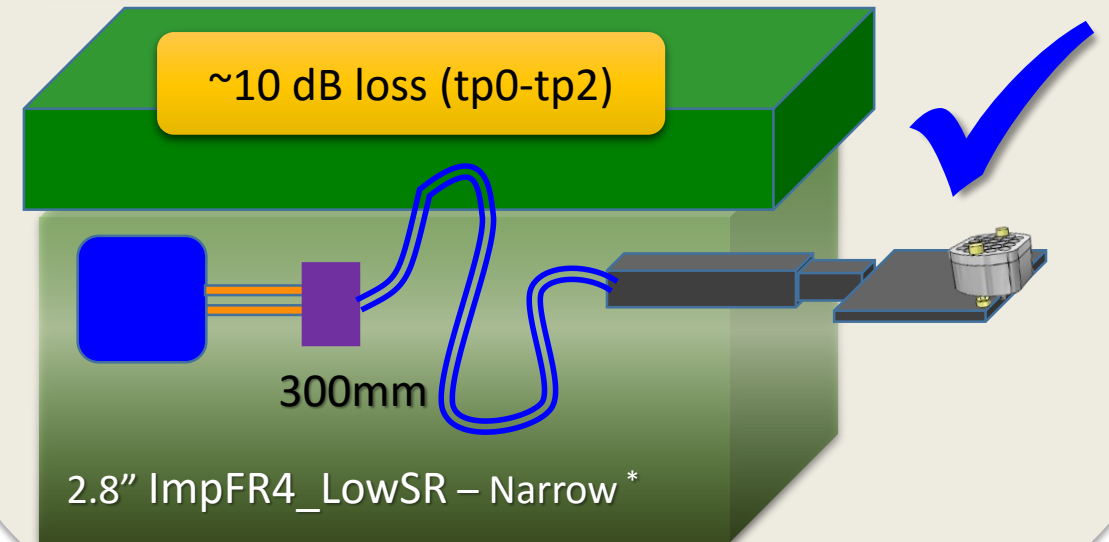
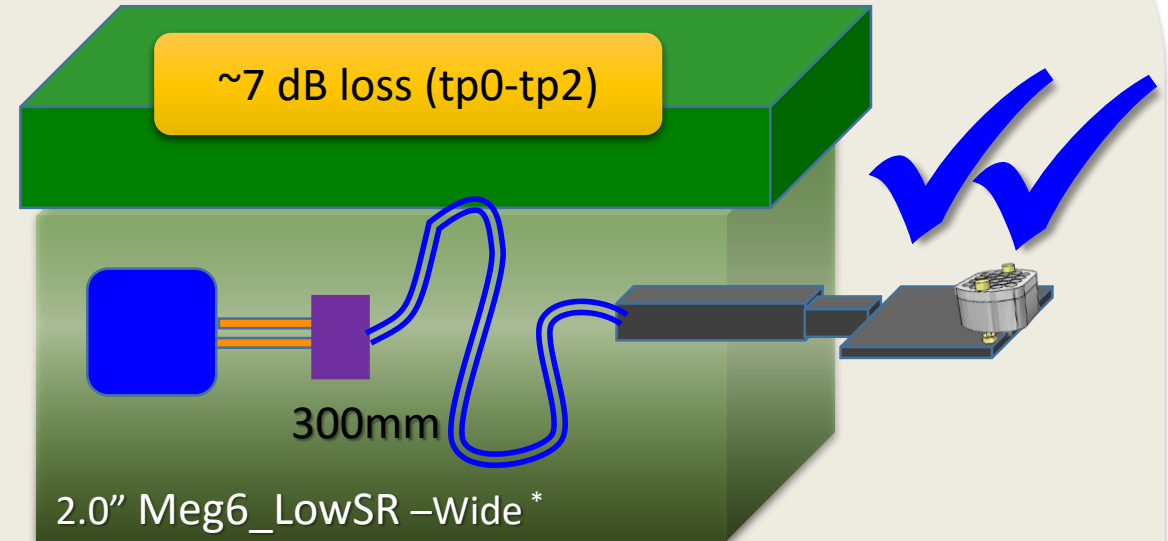
Flyover twin axial cable is another solution to alleviate density



Flyover twin axial cables fit nicely in the line card "shoebox"

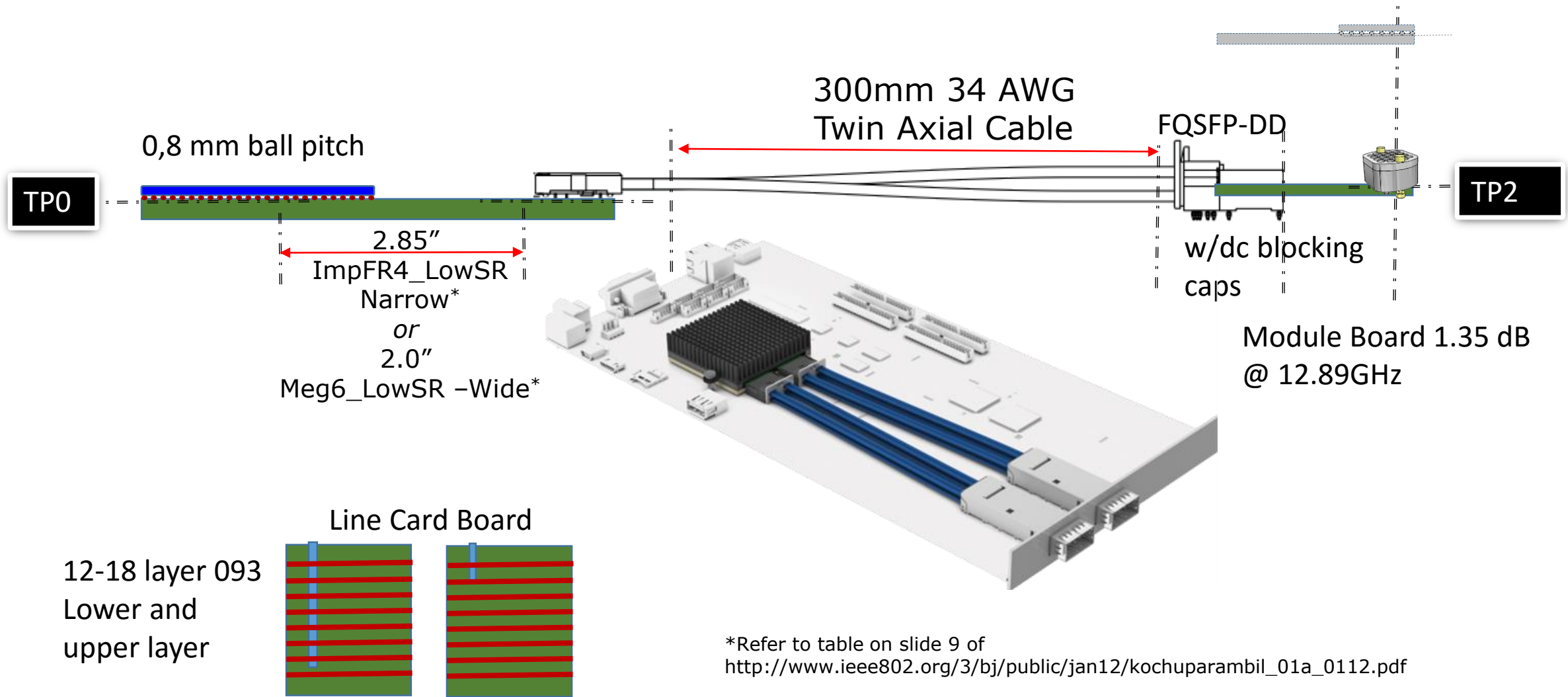


Two Channels Considered

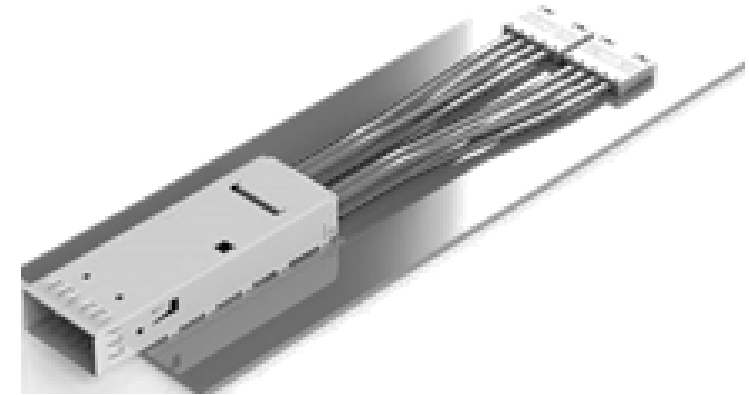
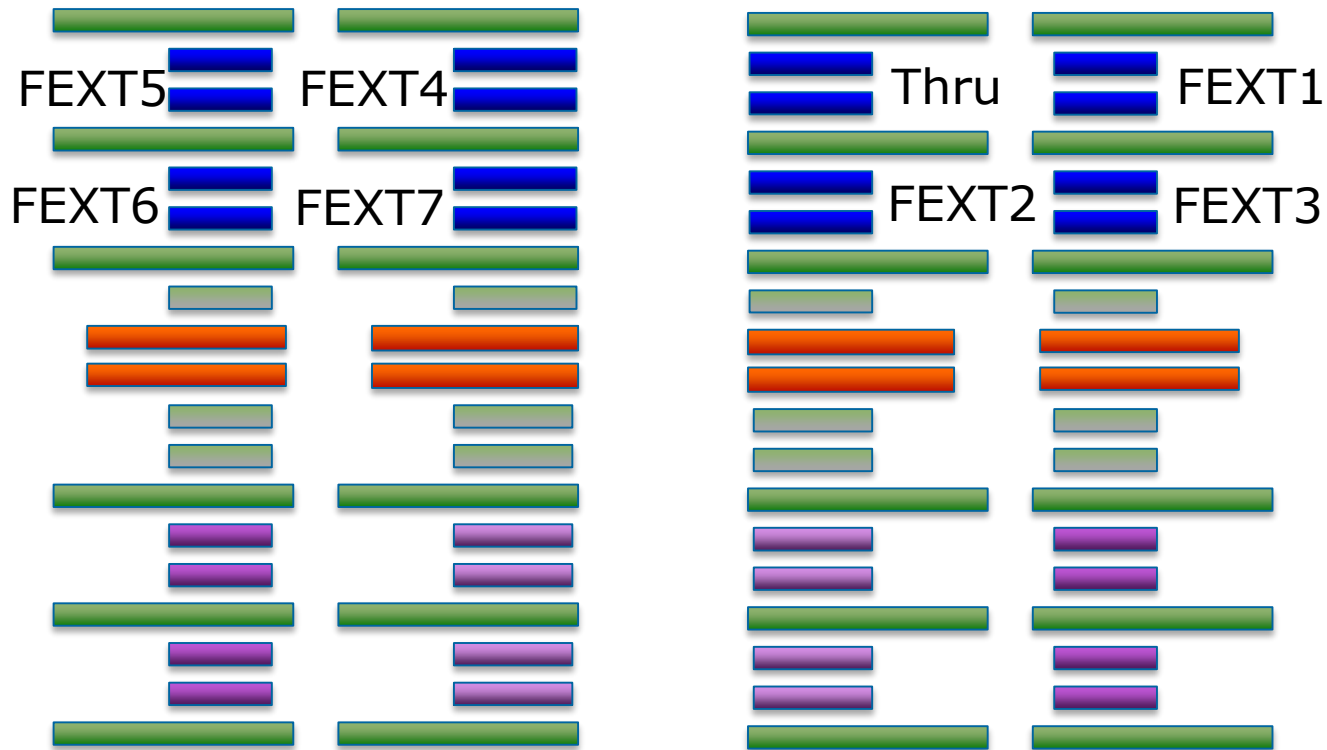


*Refer to table on slide 9 of http://www.ieee802.org/3/bj/public/jan12/kochuparambil_01a_0112.pdf

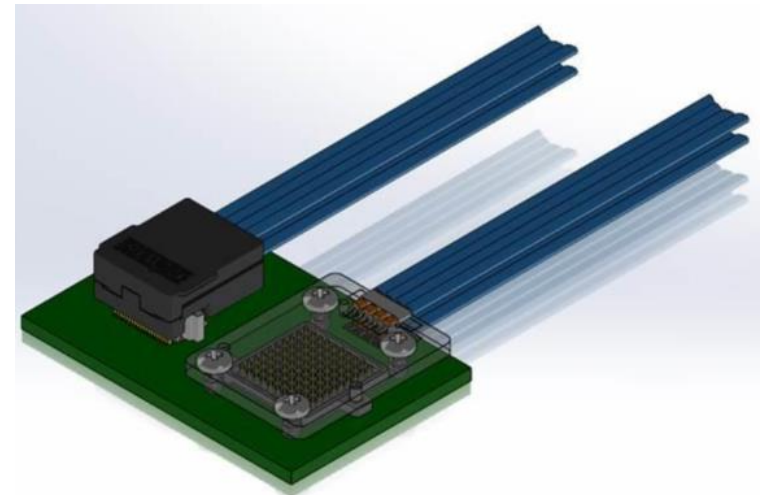
Topology – TP0 to TP2



Channel Allocation Example



Tx and Rx on separate cable bundles makes for very low NEXT



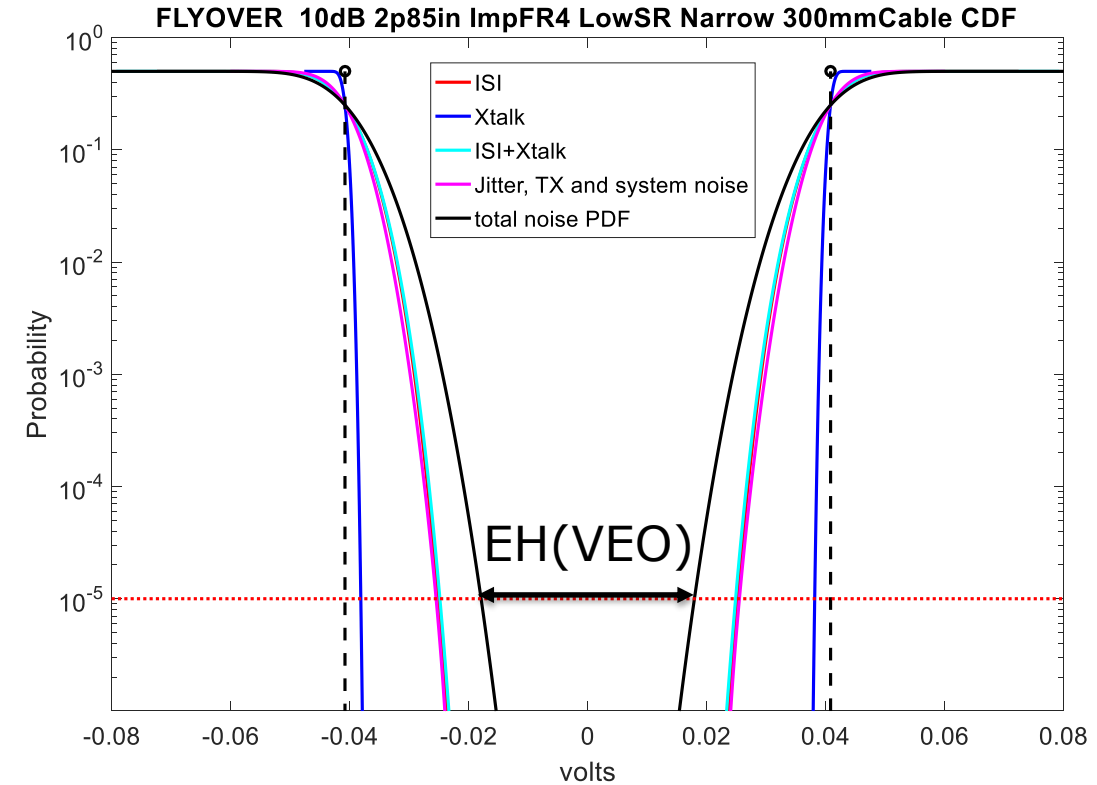
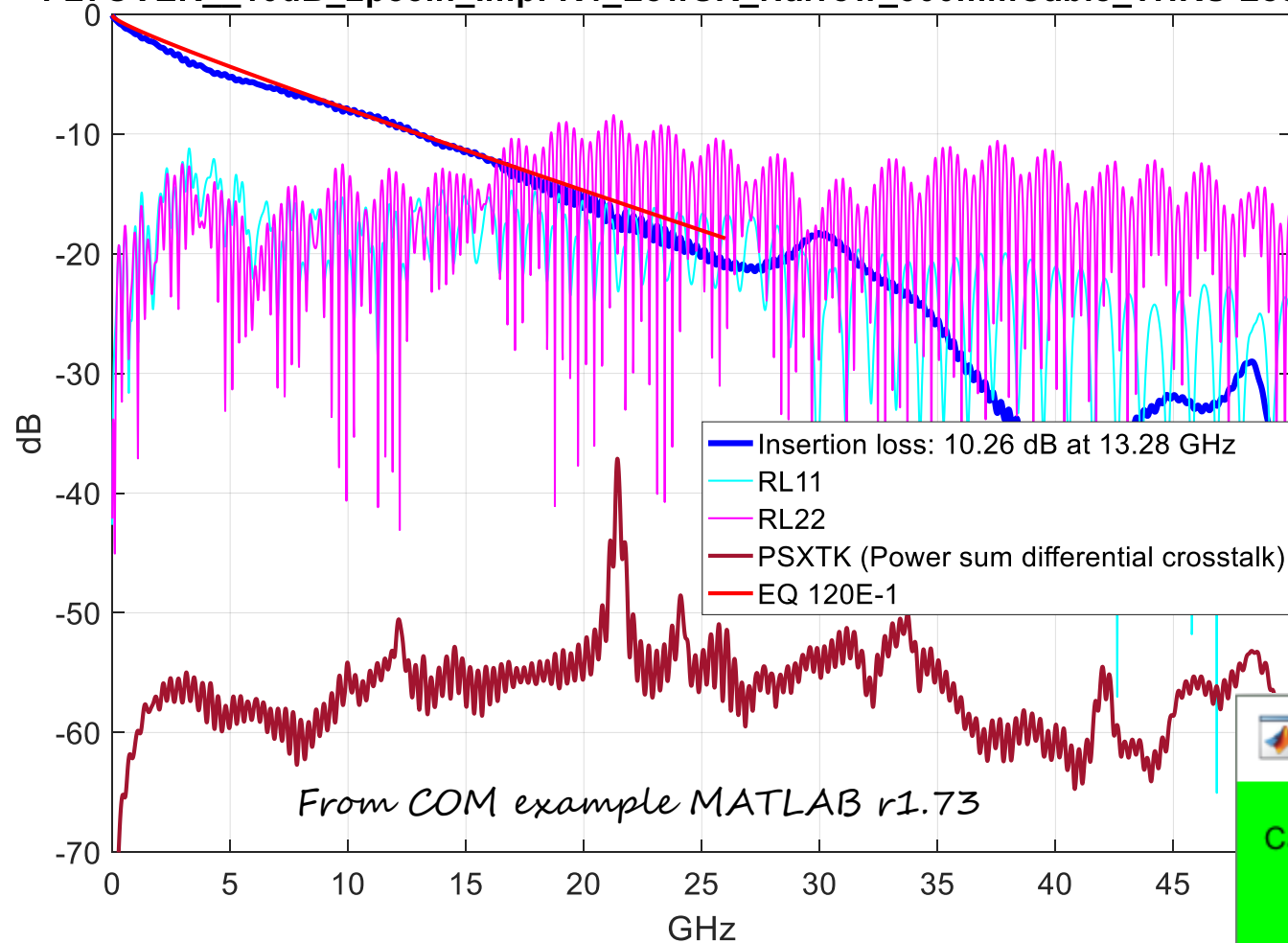
COM Table

Motivated by http://www.ieee802.org/3/bs/public/16_09/healey_3bs_01_0916.pdf,
http://www.ieee802.org/3/bs/public/17_03/dudek_3bs_01_0317.pdf and the D3.1 120d COM parameters

Table 93A-1 parameters				I/O control			
Parameter	Setting	Units	Information				
f_b	26.5625	GBd		DIAGNOSTICS	1	logical	
f_min	0.05	GHz		DISPLAY_WINDOW	1	logical	
Delta_f	0.01	GHz		Display frequency domain	1	logical	
C_d	[1.8e-4 0]	nF	[TX RX]	CSV_REPORT	1	logical	
z_p select	[1]		[test cases to run]	RESULT_DIR	.\results\C2M_{date}\		
z_p (TX)	[12]	mm	[test cases]	SAVE_FIGURES	0	logical	
z_p (NEXT)	[0]	mm	[test cases]	Port Order	[1 3 2 4]		
z_p (FEXT)	[0]	mm	[test cases]	RUNTAG	C2M_		
z_p (RX)	[0]	mm	[test cases]	Receiver testing			
C_p	[0.9e-4 0]	nF	[TX RX]	RX_CALIBRATION	0	logical	
R_0	50	Ohm		Sigma BBN step	5.00E-03	V	
R_d	[55 50]	Ohm	[TX RX]	IDEAL_TX_TERM	0	logical	
f_r	0.75	*fb		T_r	1.30E-02	ns	
c(0)	0.6		min	FORCE_TR	1	logical	
c(-1)	[-0.15:0.05:0]		[min:step:max]	Non standard control options			
c(-2)	[0:0.025:0.1]			COM_CONTRIBUTION	0	logical	
c(1)	[-0.25:0.05:0]		[min:step:max]	TDR	0	logical	
g_DC	5 3 3.5 4 4.5 5 5.5 6 6.5 7 7	dB	[min:step:max]	Operational control			
f_z	6.155 5.733 5.353 5.007 4.	GHz		COM Pass threshold	5	dB	
f_p1	5 15.6 15.6 15.6 15.6 15.6 1	GHz		Include PCB	0	Value	0, 1
f_p2	1 14.1 14.1 14.1 14.1 14.1 1	GHz		PHY_type	C2M		
A_v	0.45	V		EH_min	32	Value	EH limit
A_fe	0.45	V		EH_max	1000	Value	EH limit
A_ne	0.63	V		f_HP_P	2 1.2 1.2 1.2 1.2 1.2 1.2 1.2 1	GHz	
L	4			f_HP_Z	.1 1.075 1.05 1.025 1 1 1 1 1	GHz	
M	32			Table 93A-3 parameters			
N_b	0	UI		Parameter	Setting	Units	
b_max(1)	0.5			package_tl_gamma0_a1_a2	[0 1.734e-3 1.455e-4]		
b_max(2..N_b)	0.2			package_tl_tau	6.141E-03	ns/mm	
sigma_RJ	0.01	UI		package_Z_c	90	Ohm	
A_DD	0.02	UI					
eta_0	0.00E+00	V^2/GHz					
SNR_TX	32	dB					
R_LM	0.95						
DER_0	1.00E-05						

10 dB Loss Channel Seems to Have Acceptable Performance

FLYOVER_10dB_2p85in_ImpFR4_LowSR_Narrow_300mmCable_THRU Losses

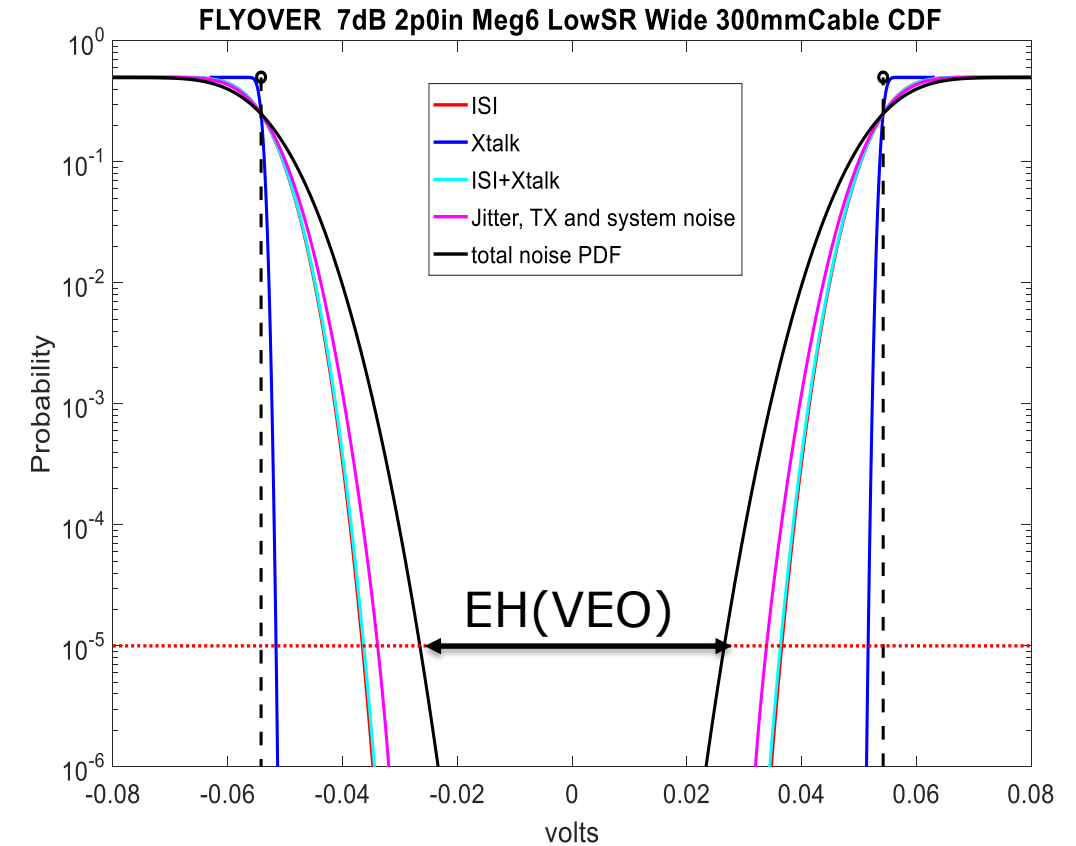
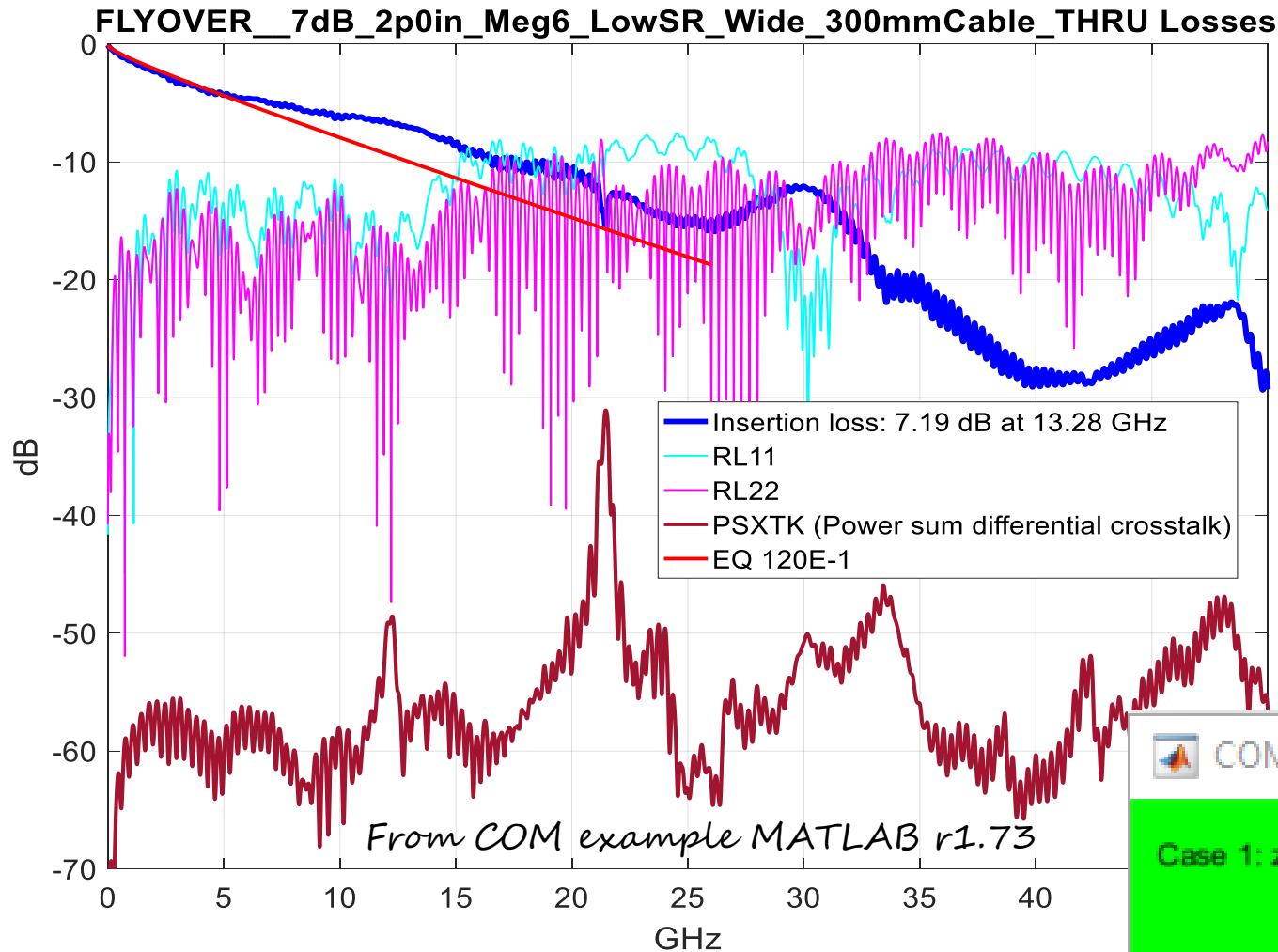


COM results

Case 1: $z_p=(12, 0, 0, 0)$ (TX, RX, NEXT, FEXT):: EH = 34.270 mV (pass)

OK

7 dB Loss Channel Seems to Have Even Better Performance

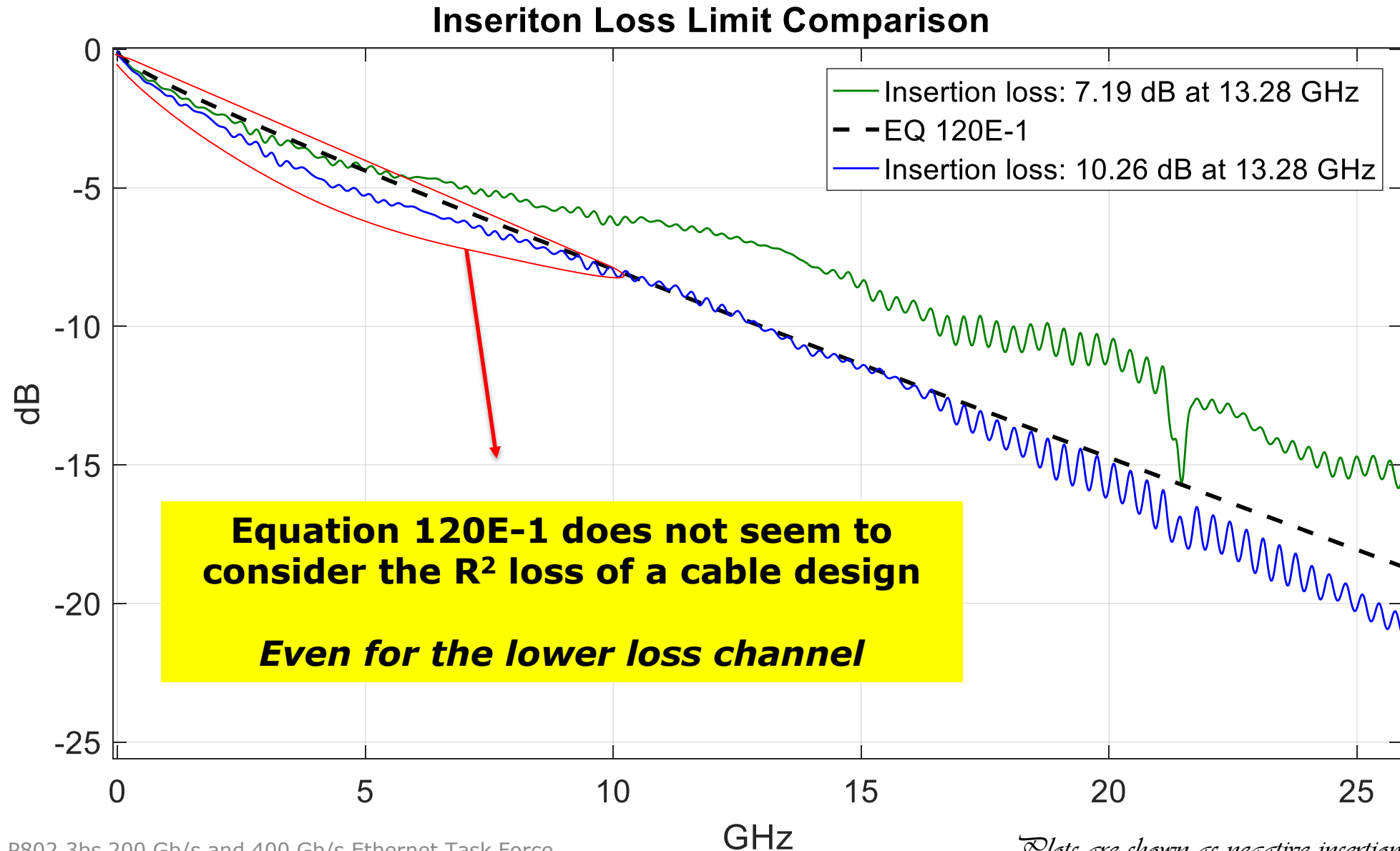


COM results

Case 1: z_p=(12, 0, 0, 0) (TX, RX, NEXT, FEXT):: EH = 51.027 mV (pass)

OK

The Issue: Cable R² Loss Not Considered



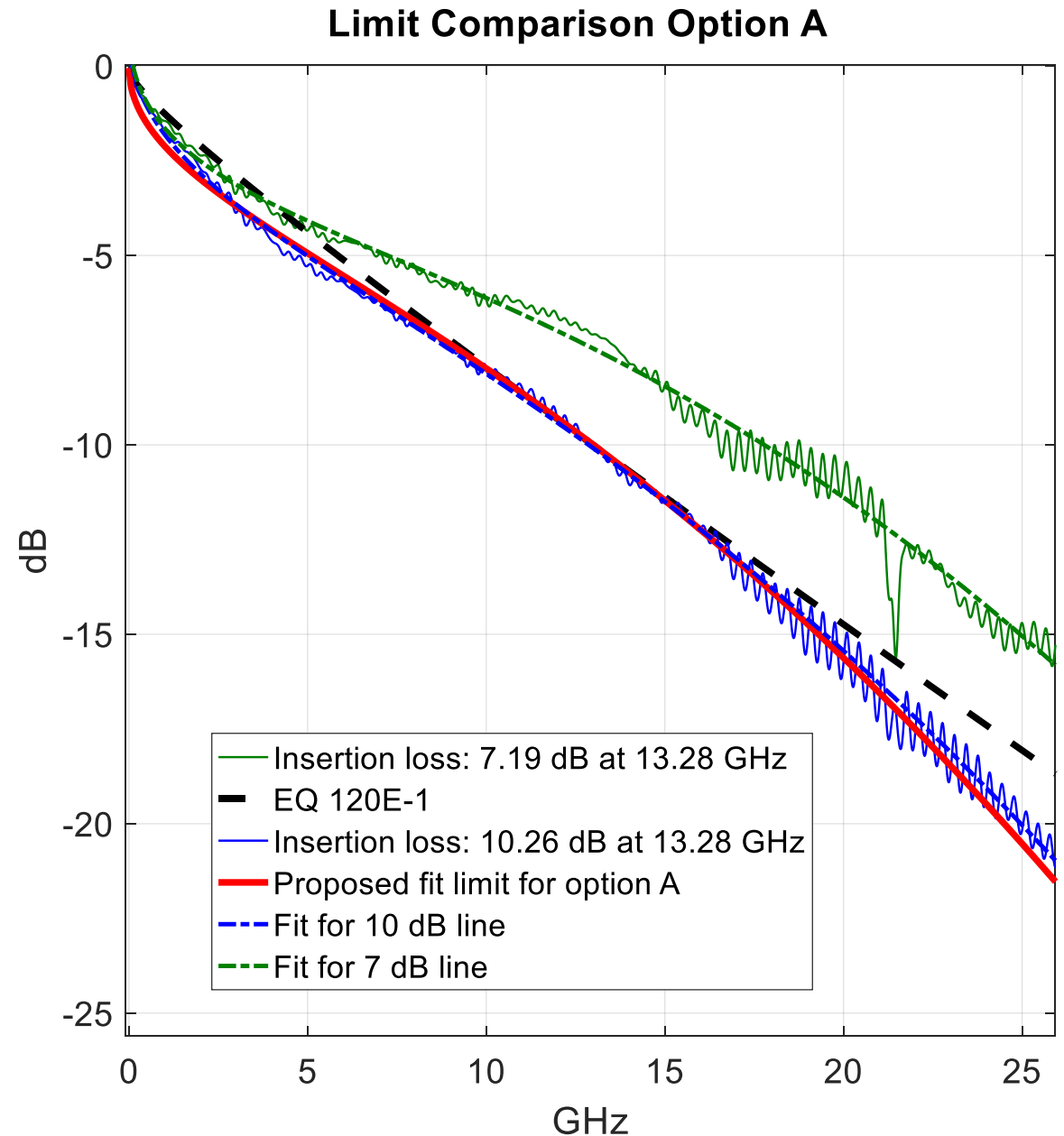
Option A

- Change equation 120E-1 to form of 93A-51 and change text to

“The supported insertion loss fit budget is characterized by Equation (120E-1) and illustrated in Figure 120E-4.” The insertion loss fit is describe in 93A.3

$$IL_{fitted}(f) = a_0 + a_1\sqrt{f} + a_2f + a_4f^2 \quad (93A-51)$$

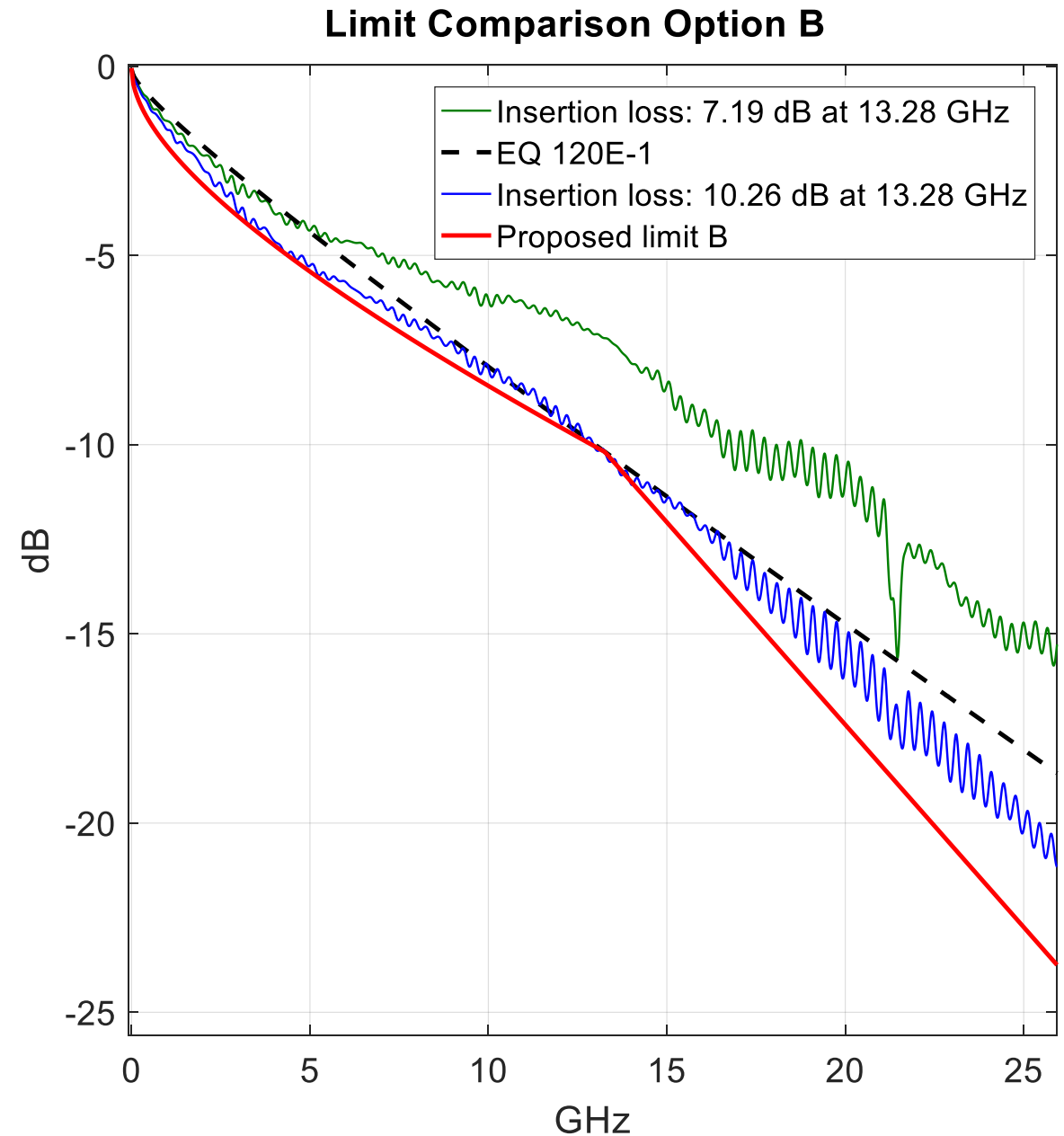
- [a0 a1 a2 a4] =
[0.05 1.65 0.155 0.0117]



Option B

- ▶ Use a limit line which encompasses r^2 cable loss.

$$\begin{aligned} & \text{Insertion_loss}(f) \\ &= \begin{cases} 0.05 + 1.8\sqrt{f} + 0.2705f \text{ (dB)} & f \leq 13.28 \\ -4.0096 + 1.07f \text{ (dB)} & f > 13.28 \end{cases} \end{aligned}$$



Option C

- ▶ Add words to the effect that cable designs may not have to meet the low frequency masks
- ▶ Maybe something like:
 - Change
 - “The supported insertion loss budget is characterized by Equation (120E–1) and illustrated in Figure 120E–4. ”
 - To
 - “The supported insertion loss budget is characterized by Equation (120E–1) and illustrated in Figure 120E–4. However some designs using low loss material such as twin axial cable may dip below the line characterized by Equation 120E-1. Any design that meets the Transmitter and Receiver specifications given in sections 120E-2 to 120E-4 is acceptable.”

Summary

- ▶ Flyover twin axial cable chip to module channel models provided for further analysis
- ▶ Broaden chip to module potential market applications to include twin axial cable
 - Choose from Option A, B, or C
- ▶ Recommendation: Option B
 - Use a limit line which encompasses r^2 cable loss and a wider range of applications

Files and Naming

mellitz_3bs_01_041817.zip Tag name: 10 dB C2M Flyover tp0-tp2 channel

FLYOVER__7dB_2p0in_Meg6_LowSR_Wide_300mmCable_FEXT_1.s4p
FLYOVER__7dB_2p0in_Meg6_LowSR_Wide_300mmCable_FEXT_2.s4p
FLYOVER__7dB_2p0in_Meg6_LowSR_Wide_300mmCable_FEXT_3.s4p
FLYOVER__7dB_2p0in_Meg6_LowSR_Wide_300mmCable_FEXT_4.s4p
FLYOVER__7dB_2p0in_Meg6_LowSR_Wide_300mmCable_FEXT_5.s4p
FLYOVER__7dB_2p0in_Meg6_LowSR_Wide_300mmCable_FEXT_6.s4p
FLYOVER__7dB_2p0in_Meg6_LowSR_Wide_300mmCable_THRU.s4p

mellitz_3bs_02_041817.zip Tag name: 7 dB C2M Flyover tp0-tp2 channel

FLYOVER__10dB_2p85in_ImpFR4_LowSR_Narrow_300mmCable_FEXT_1.s4p
FLYOVER__10dB_2p85in_ImpFR4_LowSR_Narrow_300mmCable_FEXT_2.s4p
FLYOVER__10dB_2p85in_ImpFR4_LowSR_Narrow_300mmCable_FEXT_3.s4p
FLYOVER__10dB_2p85in_ImpFR4_LowSR_Narrow_300mmCable_FEXT_4.s4p
FLYOVER__10dB_2p85in_ImpFR4_LowSR_Narrow_300mmCable_FEXT_5.s4p
FLYOVER__10dB_2p85in_ImpFR4_LowSR_Narrow_300mmCable_FEXT_6.s4p
FLYOVER__10dB_2p85in_ImpFR4_LowSR_Narrow_300mmCable_FEXT_7.s4p
FLYOVER__10dB_2p85in_ImpFR4_LowSR_Narrow_300mmCable_THRU.s4p