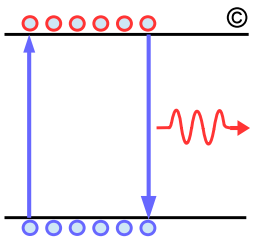


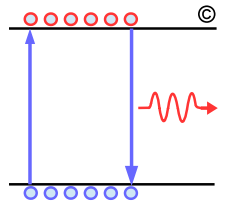
Options for CRU BW for 400 GbE PAM4 PMDs

Ali Ghiasi
Ghiasi Quantum LLC

802.3bs Electrical Adhoc Meeting

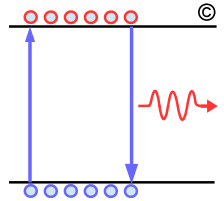
August 24, 2015

Overview

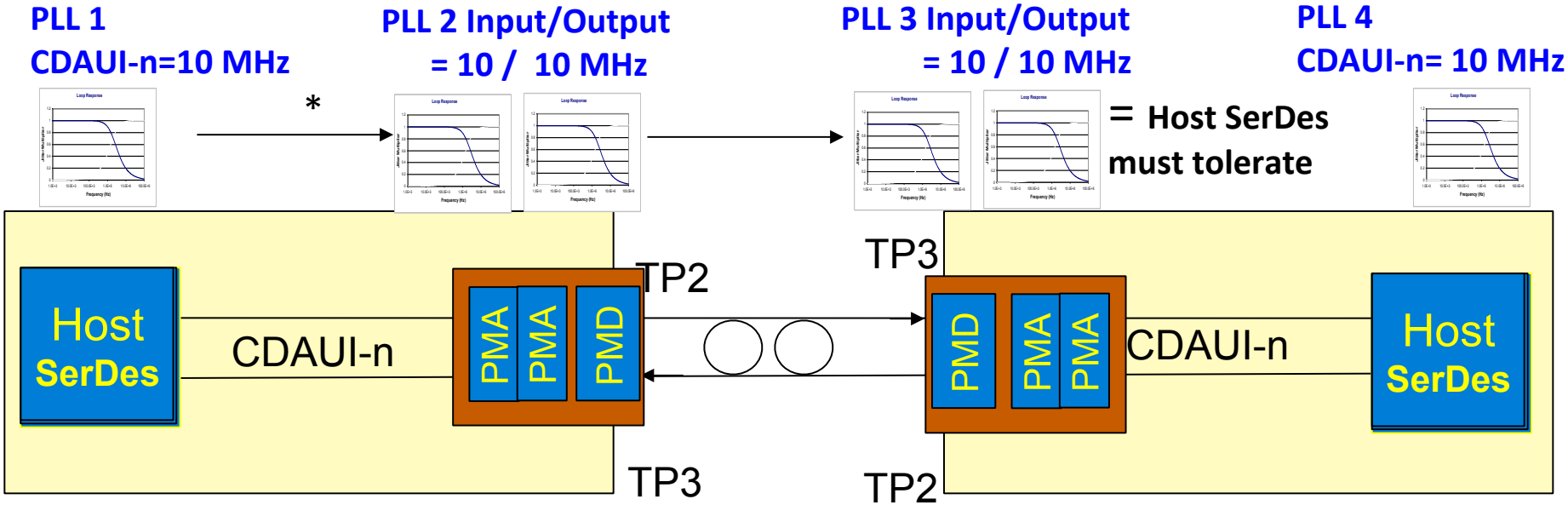


- **Previously considerations for CRU and CDR BW have been presented in details**
  - http://www.ieee802.org/3/bm/public/mar14/ghiasi_01_0314_optx.pdf
  - http://www.ieee802.org/3/bs/public/15_07/ghiasi_3bs_01_0715.pdf
- **802.3bs has no specific objective for a ports to be backward compatible with legacy 10 GbE, 40 GbE, or 100 GbE**
  - Since 802.3ae in Ethernet we have been using CRU BW of Fbaud/2578
  - CRU BW for standards at 10.3125 GBd/lane is 4 MHz
  - CRU BW for standards at 25.78 GBd/lane is 10 MHz
  - The market however requires at least the host provide a level of backward compatibility
  - CDAUI-16 based on 4 instance of CAUI-4 carries forward 10 MHz CRU
- **Next will explore options for 802.3bs CRU BW.**

Option 1: Assume 10 MHz CRU BW

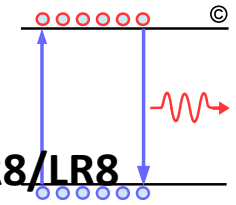


- **Propose to use 10 MHz CRU BW for CDAUI-8, 400Gbase-DR4, 400Gbase-FR8/LR8**
- **It simplifies the overall architecture at expense of requiring faster tracking BW resulting in higher power on more complex PAM4 receivers**
  - This approach is backward compatible with previous IEEE standards and compatible with CDAUI-16 which is based on CAUI-4
  - Allow implementation to follow current 100G retime modules based on CAUI-4 based on simple CDR without FIFO (insertion/deletion or phase).



* Only reverse propagating right-left not illustrated would be similar.

Option 2: Assume 4 MHz CRU BW



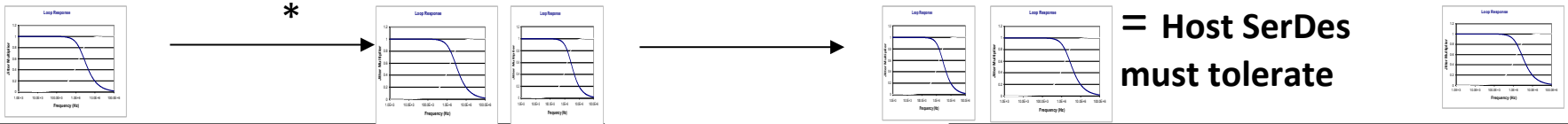
- **Propose to use 4 MHz CRU BW for CDAUI-8, 400Gbase-DR4, 400Gbase-FR8/LR8**
- **Backward compatible with 10.3125 GBd/lane PMD's**
  - More moderate tracking BW help more complex PAM4 receivers and reduce power
- **This approach is not backward compatible with IEEE standards operating 25.78 GBd/ lane or CDAUI-16 which is based on CAUI-4**
  - Require a PMA-PMA chip in the module with insertion/deletion FIFO or a dual loop PLL similar to early XAUI to 10G PMA's implementations
  - As one moves to CDAUI-8 host then FIFO in the PMA-PMA chip could be eliminate
  - CDAUI-8 host operating with legacy host based on 25.78 GBd/lane always would require the PMA-PMA chip have a FIFO or implement dual loop PLL.

PLL 1
CDAUI-16=10 MHz
CDAUI-8=4 MHz
CDAUI-8=4 MHz

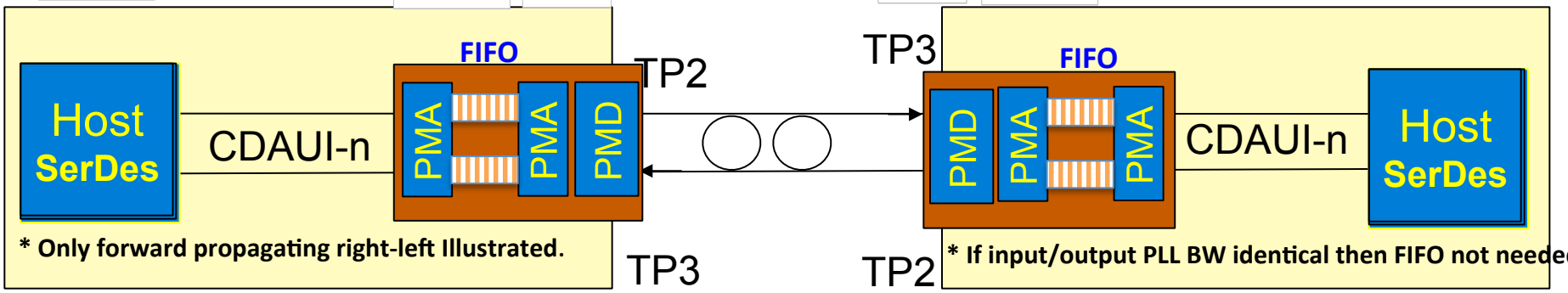
PLL 2 Input/Output *
= 10 / 4 MHz
= 4 / 4 MHz
= 4 / 4 MHz

PLL 3 Input/Output *
= 4 / 10 MHz
= 4 / 4 MHz
= 4 / 10 MHz

PLL 4
CDAUI-16= 10 MHz
CDAUI-8=4 MHz
CDAUI-16=10 MHz



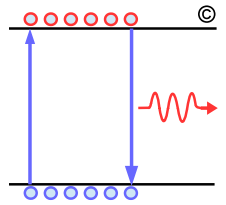
= Host SerDes must tolerate



*** Only forward propagating right-left Illustrated.**

*** If input/output PLL BW identical then FIFO not needed**

Summary



- **Reliable link operation requires that the receiver test complements transmitter test**
  - Golden CRU having high pass response mask the transmitter low frequency jitter components propagating down the link that the receiver must tolerate
- **HOM receivers are more complex with timing recovery potentially having higher latency could make it difficult to support Fbaud/2578 CRU**
  - What makes the problem more complex are
    - CDAUI-16 based on CAUI-4 forces 10 MHz CRU into the 802.3bs unless we redefine CDAUI-16 effectively make it incompatible with CAUI-4
    - Market requires that future Ethernet speed to provide a level of compatibility with legacy products
- **Two viable options explored are:**
  - Option I: 10 MHz CRU BW for all 50/100 Gb/s PAM4 PMDs allow full backward compatibility with CDAUI-16 as well as legacy support
  - Option II: 4 MHz CRU BW for all 50/100 Gb/s PAM4 PMDs would require PMA-PMA chip to have FIFO (phase and/or insertion deletion) to interface with CDAUI-16 as well as all legacy PMD's
- **Neither one of the above decision are trivial!**