

# **400 & 4x100 Gb/s PMD Alternatives Study**

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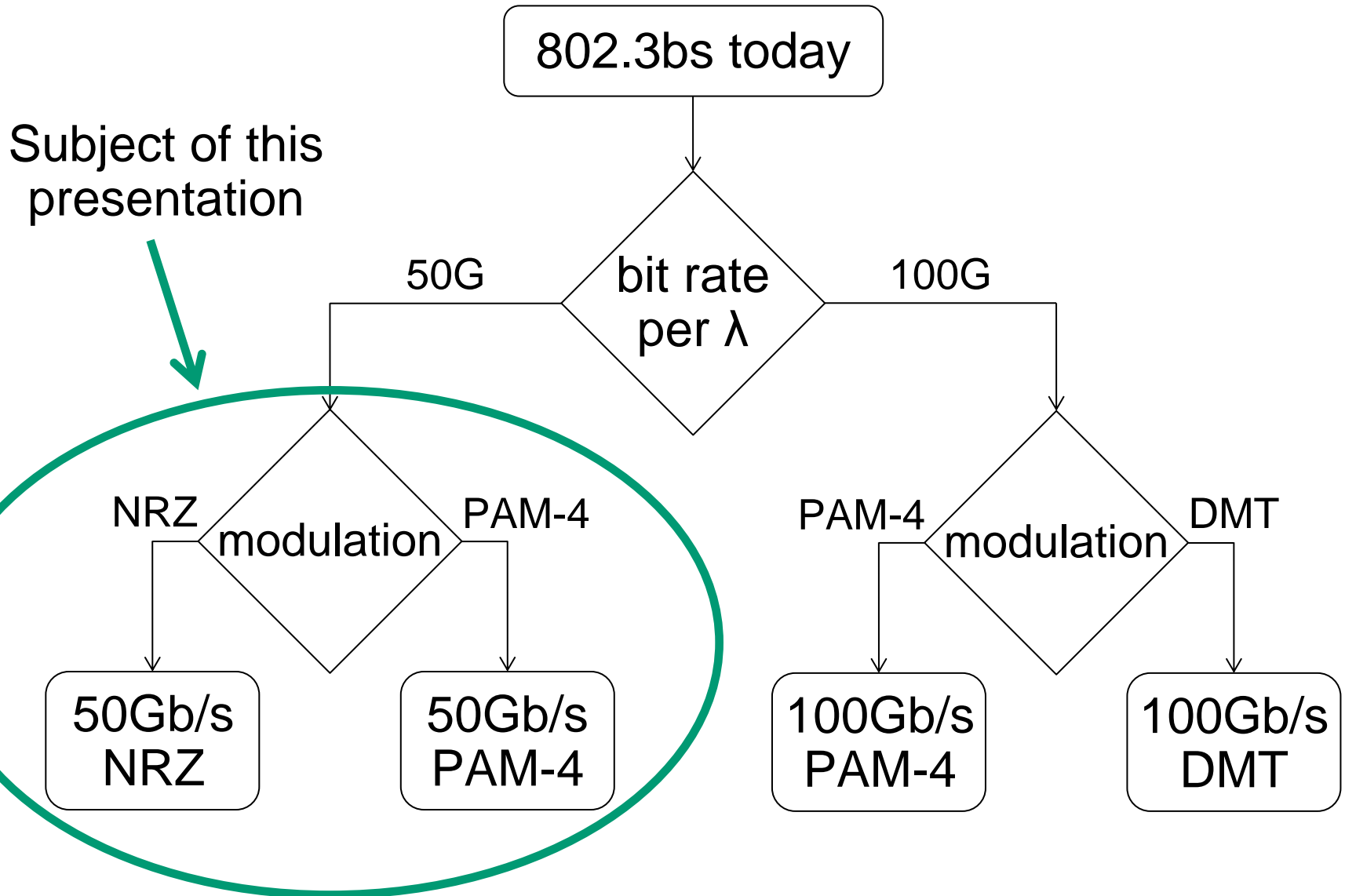
400 Gb/s Ethernet Task Force  
SMF Ad Hoc Conference Call  
19 June 2014  
Chris Cole

# Finisar Contributors

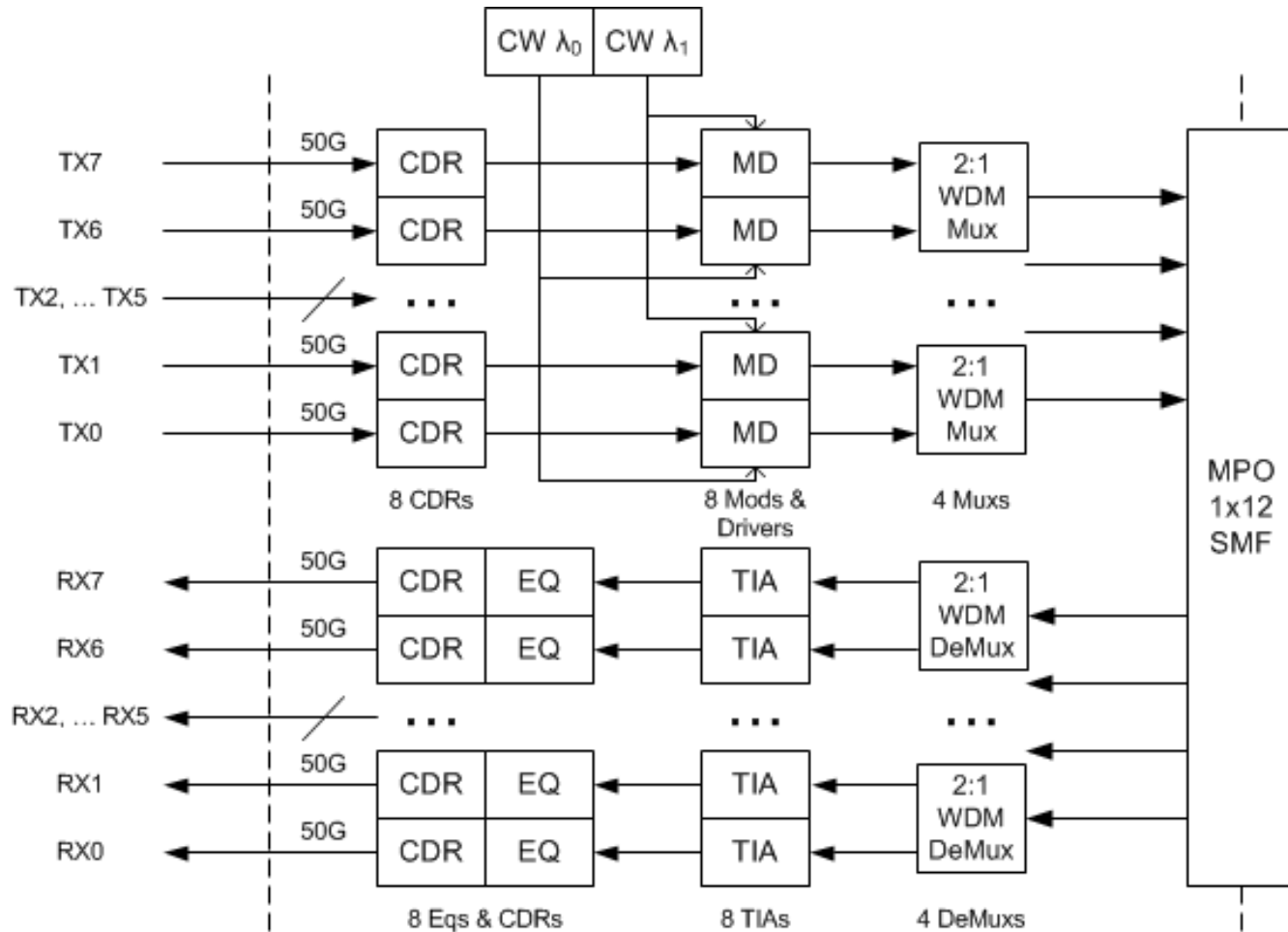
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- Gilles Denoyer
- Bernd Huebner
- Jonathan King
- Ilya Lyubomirsky
- Daniel Mahgerefteh
- Thelinh Nguyen
- Thang Pham
- Jack Xu

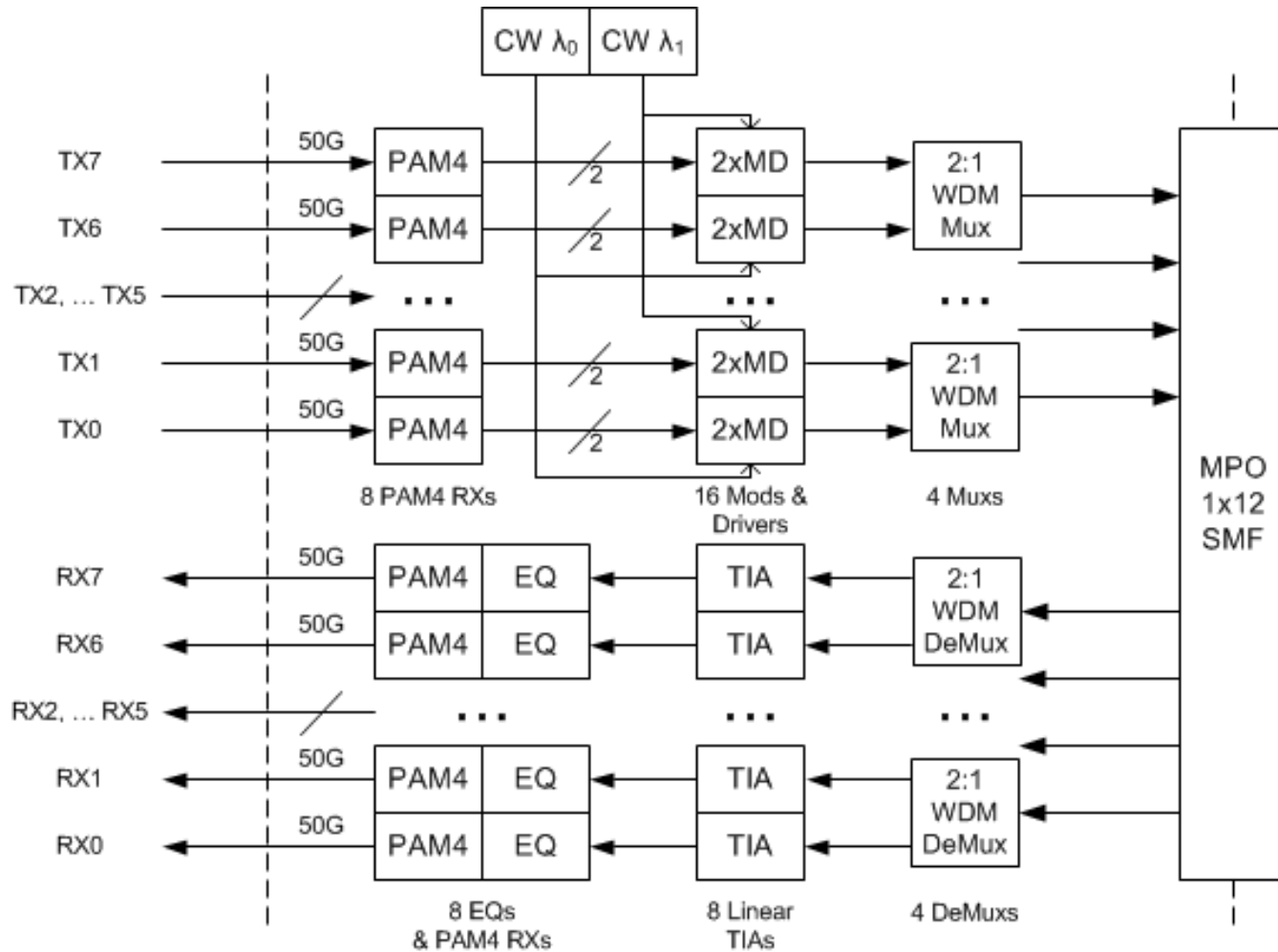
# Duplex SMF & PSM4 PMDs Decision Tree



# 400GbE-PSM4 Alt 1: Quad 2x 50G NRZ $\lambda$ s



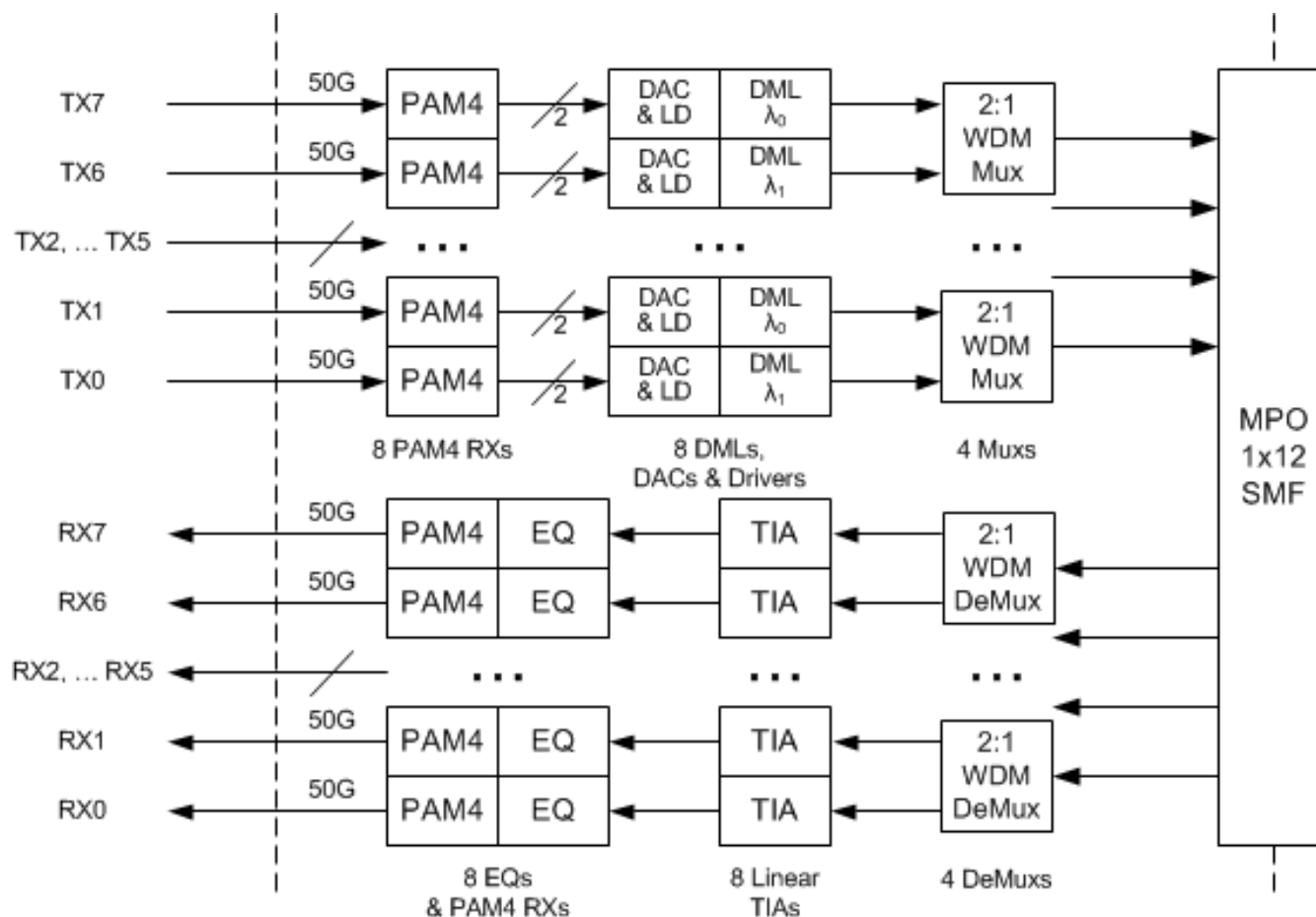
# 400GbE-PSM4 Alt 2: Quad 2x 50G PAM-4 $\lambda$ s



CDAUI-8

4x100GbE-FR2 & 400GbE-PSM4

# 400GbE-PSM4 Alt 3: Quad 2x 50G PAM-4 $\lambda$ s

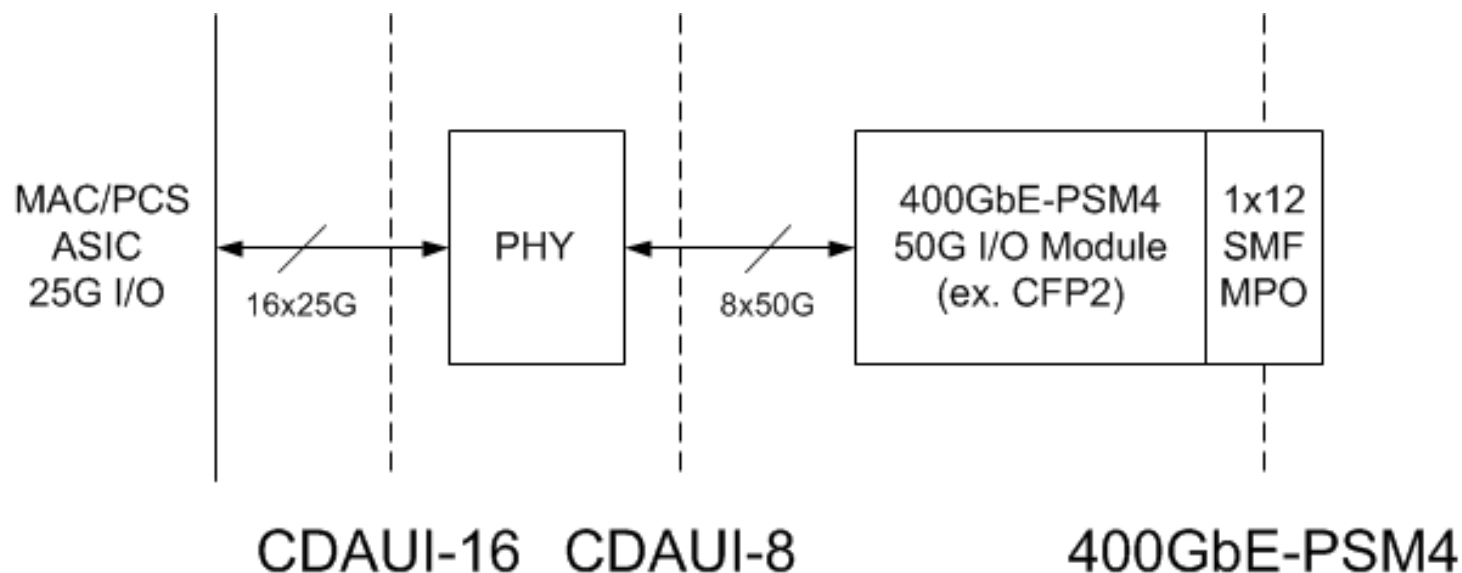


CDAUI-8

4x100GbE-FR2 & 400GbE-PSM4

# 400G CDAUI-16 I/O ASIC Host Architecture

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- CDAUI-16 I/O module (ex. CDP) has converter PHY inside

# 400GbE-PSM4 Alternatives TX Nominal Specs

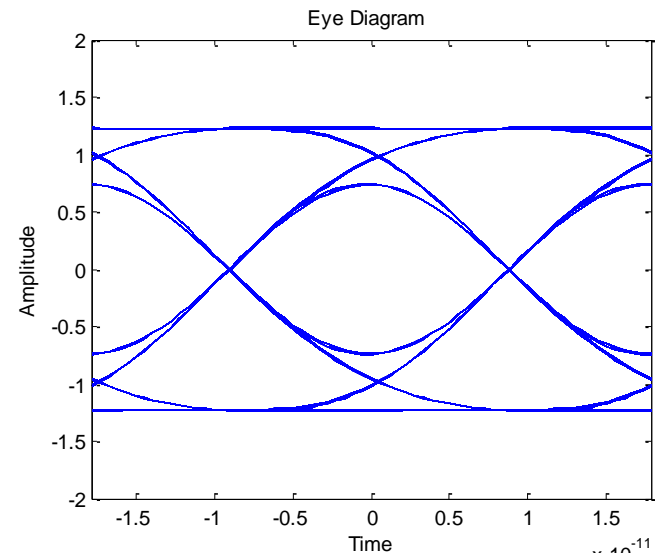
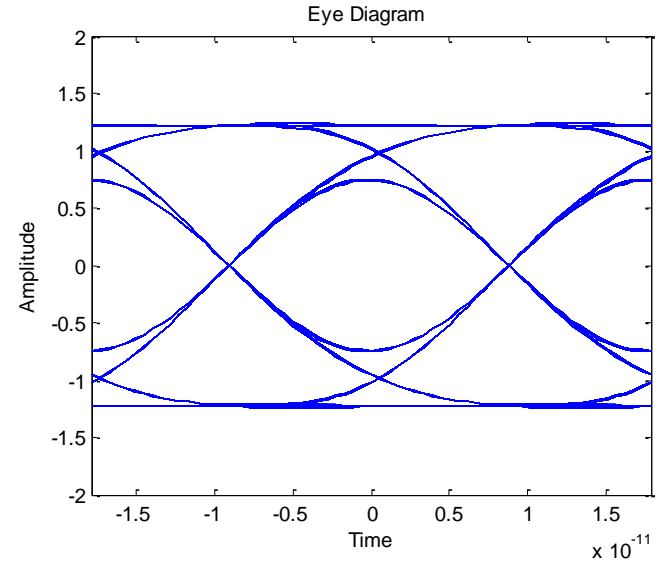
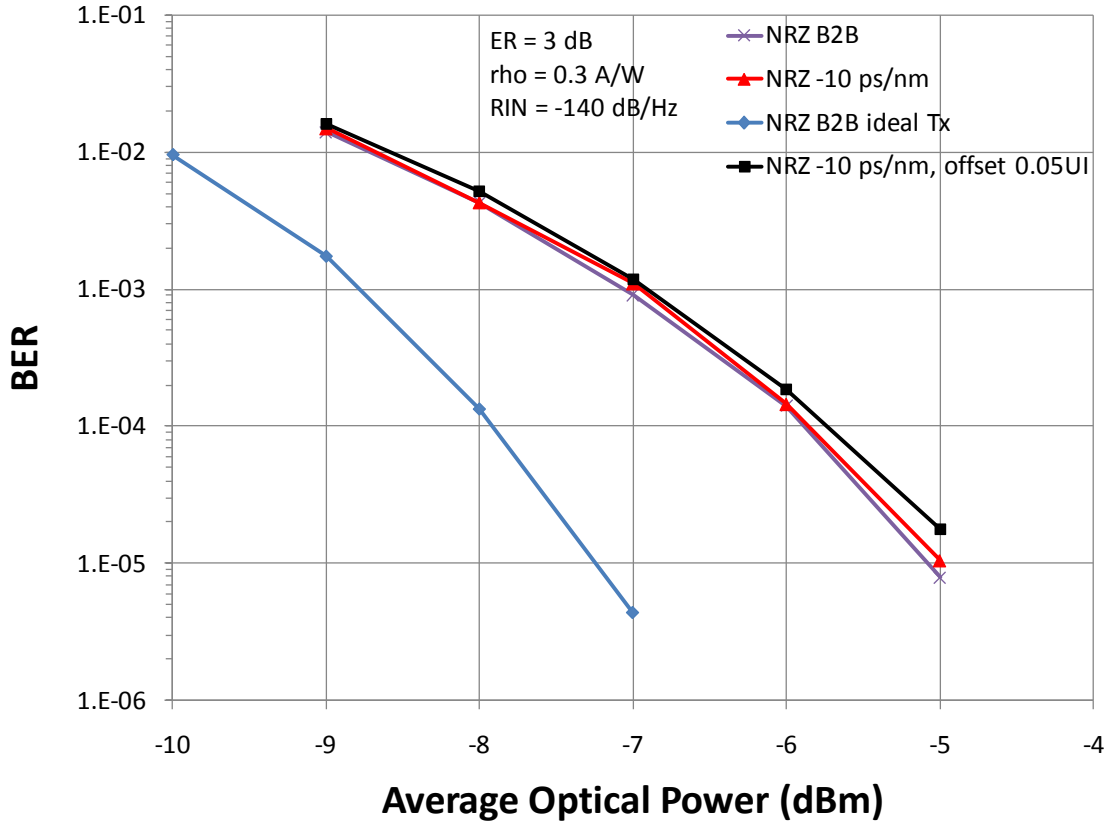
Specification	NRZ DML 100G LR4	NRZ MZ w/ KR4 FEC	PAM-4 MZ w/ KR4 FEC	PAM-4 MZ w/ KP4 FEC	PAM-4 DML w/ KR4 FEC
Symbol Rate Gbaud	25.8	51.6	25.8	26.6	25.8
Reach km	10	2.0	2.0	2.0	2.0
Operating BER	1E-12	5E-05	5E-05	2E-04	5e-5
$\lambda$ nm	1290 < 1310	1290, 1310	1290, 1310	1290, 1310	1290, 1310
TX OMA (11-00) (min) dBm @ TDP (max)	<b>-0.1</b>	<b>-2.0</b>	<b>-1.0</b>	<b>-1.0</b>	<b>2.0</b>
ER (11/00) (min) dB	4.0	4.0	7.5	7.5	4.5
TX OMA (01-00) (min) dBm @ TDP (max)	-0.1	-2.0	-6.0	-6.0	-3.0
TDP (max) dB	2.2	2.5	1.0	1.0	3.0
TX OMA (01-00) -TDP each lane (min) dBm	-2.3	-4.5	-7.0	-7.0	-6.0



# 400GbE-PSM4 Alternatives RX Nominal Specs

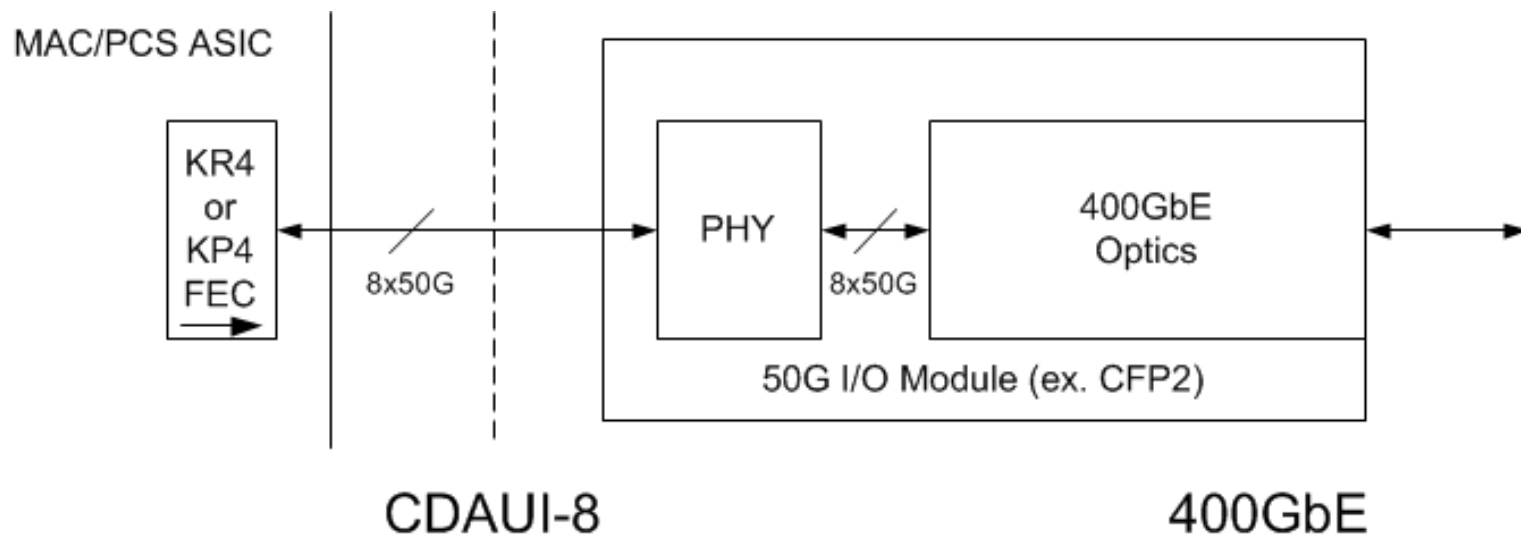
Specification	NRZ DML 100G LR4	NRZ MZ w/ KR4 FEC	PAM-4 MZ w/ KR4 FEC	PAM-4 MZ w/ KP4 FEC	PAM-4 DML w/ KR4 FEC
Gbaud	25.8	51.6	25.8	26.6	25.8
TX OMA (01-00) -TDP each lane (min) dBm	-2.3	-4.5	-7.0	-7.0	-6.0
Channel Insertion Loss dB	6.3	5.0	5.0	5.0	5.0
RX Sens. OMA pre-FEC each lane (max) dBm	<b>-8.6</b>	<b>-9.5</b>	<b>-12.0</b>	<b>-12.0</b>	<b>-11.0</b>
FEC Optical Gain dB	0.0	2.6	2.6	3.2	2.6
Pattern Gain (vs. PRBS31) dB	0.0	0.5	0.5	0.5	0.5
BW & Other Penalties (vs. 4 Ch. Limiting) dB	0.0	2.5	0.0	0.1	0.0
RX Sens. OMA LR4 equiv each lane (max) dBm	<b>-8.6</b>	<b>-8.9</b>	<b>-8.9</b>	<b>-8.4</b>	<b>-7.9</b>

# Example TDP Simulation: 51.6G NRZ MZ



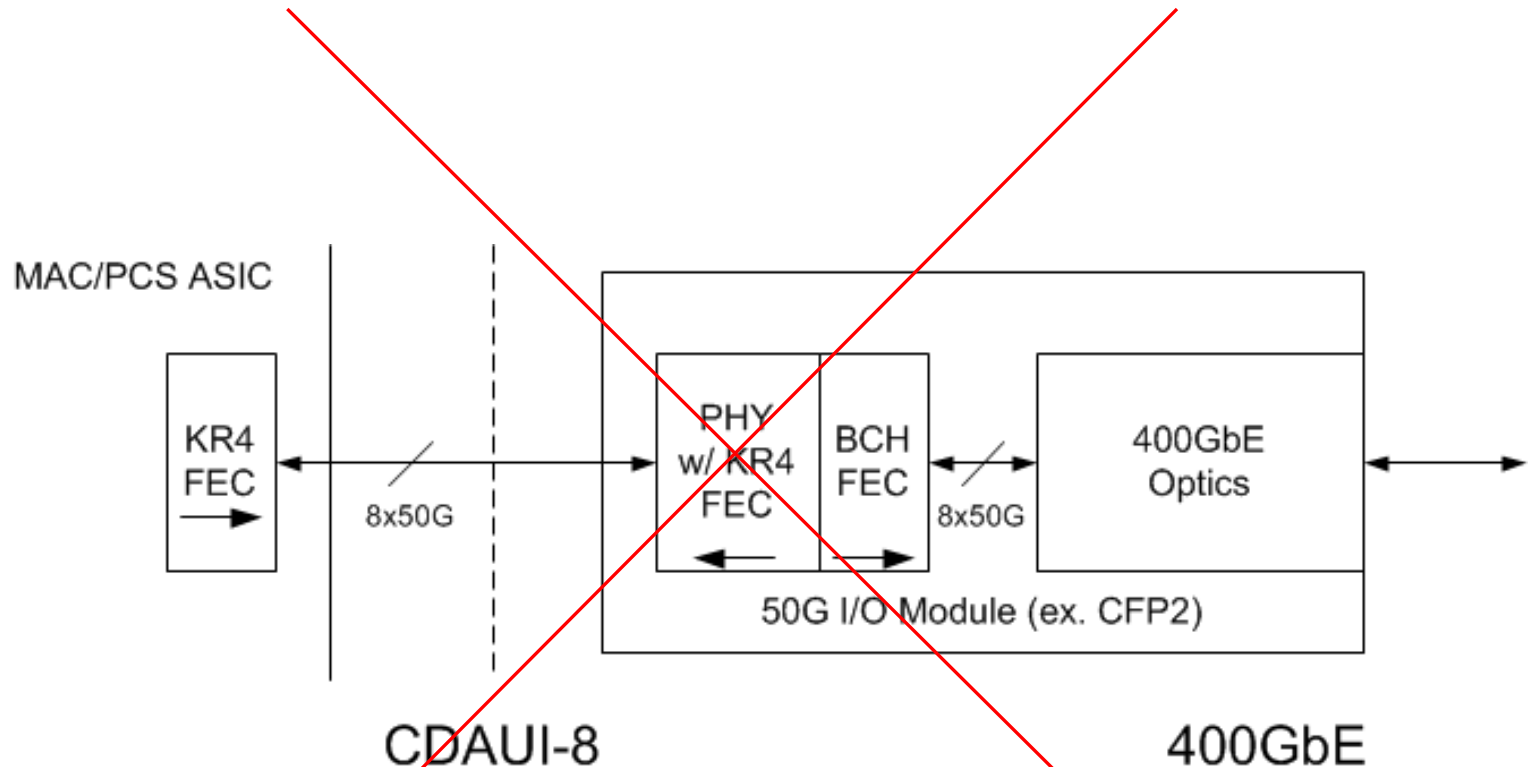
- TDP = ~2.5dB
- Consistent with early measurements

# 400G PMD KR4 or KP4 FEC Host Architecture



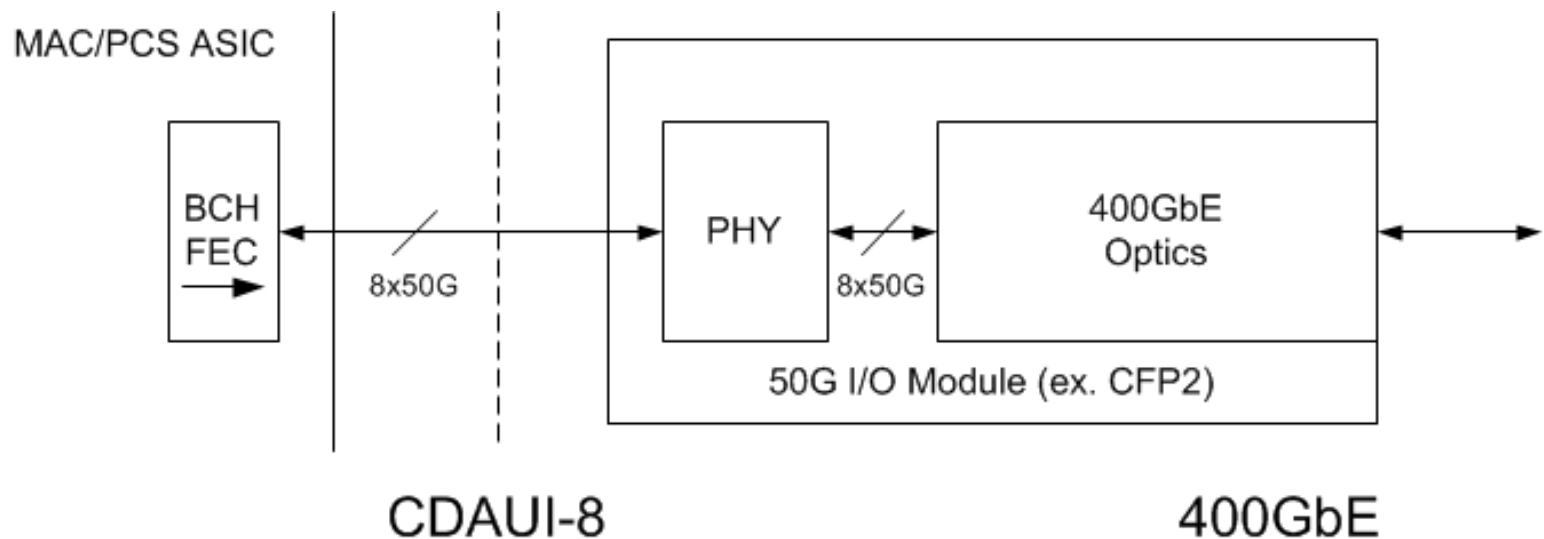
- Assumes FEC gain is allocated to the optics
- CDAUI-16 I/O ASIC also has KR4 and/or KP4 FEC

# What If We Need Strong PMD FEC Like BCH?



- PMD unfriendly architecture

# 400G PMD Strong FEC Host Architecture



- PMD friendly architecture
- Assumes no CDAUI-8 DFE

# Study Observations

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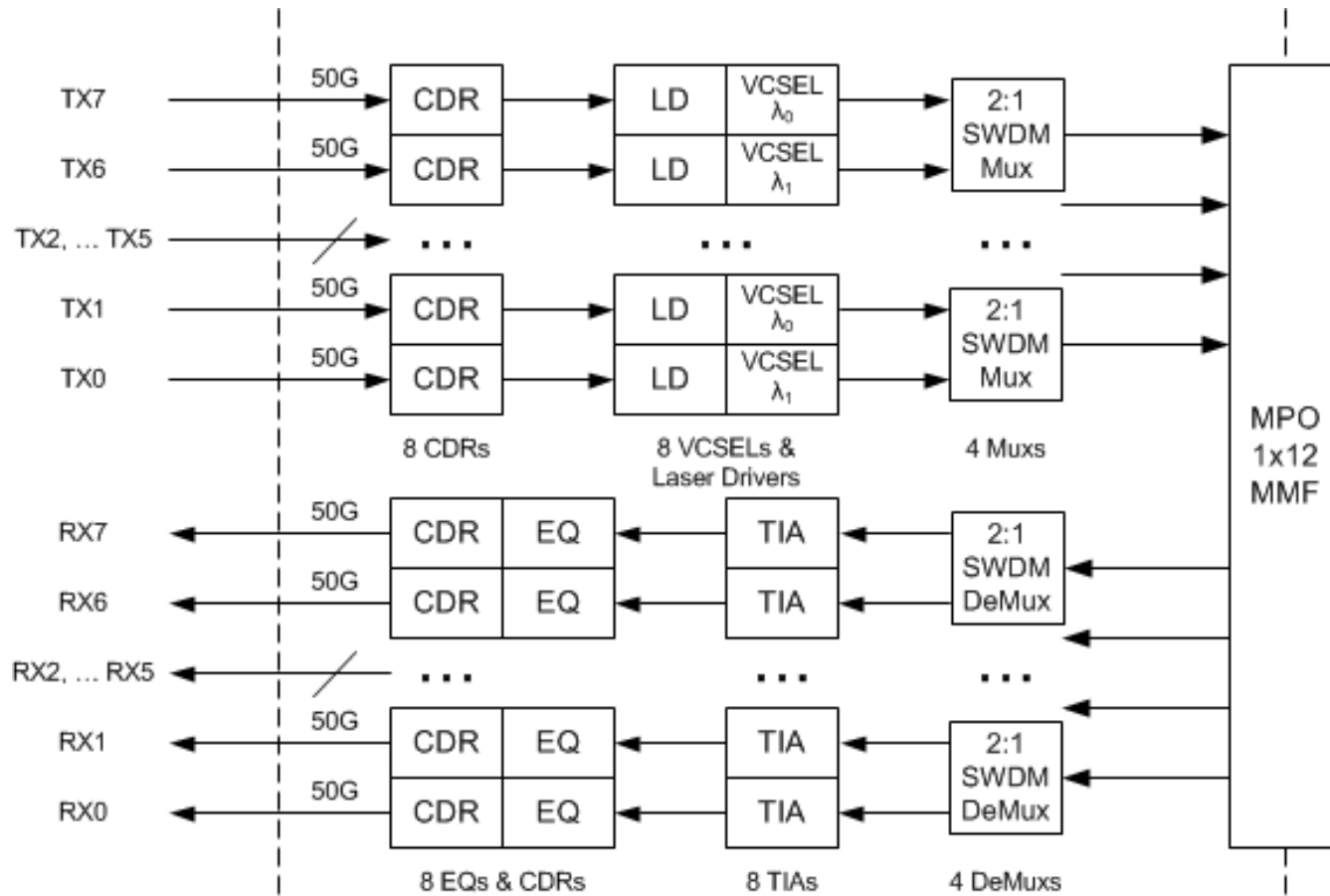
- 2x50G/λ NRZ MZ PMD
  - KR4 FEC maybe sufficient
  - Good TX and RX margin
- 2x50G/λ PAM-4 MZ PMD
  - KP4, possibly KR4, FEC maybe sufficient
  - Requires low TDP (~1dB)
  - TX OMA (min) may limit CW laser output splitting to 2 modulators/laser
- 2x50G/λ PAM-4 DML PMD
  - KR4 FEC maybe sufficient
  - High TX OMA contributes to good RX margin
- FEC (KR4, KP4, BCH, or other) belongs on the host ASIC

# Appendix: Why 50G/λ instead of 100G/λ?

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- Same reason that crooks rob banks:
  - It's where the money is
  - Equivalently it's where the volume is
- 50G per lane may support 400GBASE-SR4.2 duplex MMF
- 40/50G per lane is the next high volume rate after 25G per lane, driven by server I/O
- 40/50G per lane increases 40G port density by 4x:
  - 40/50G Serial duplex MMF & SMF
  - 160/200G (4x 40/50G Serial duplex) QSFP & CFP4
  - 40/50G Serial duplex SFP40
- 50G per lane doubles 100G port density by 2x:
  - 2x50G WDM duplex SMF & MMF
  - 200G (2x 2x50G WDM duplex) QSFP & CFP4

# 400GbE-SR4.2 Alt 1: Quad 2x 50G NRZ $\lambda$ s

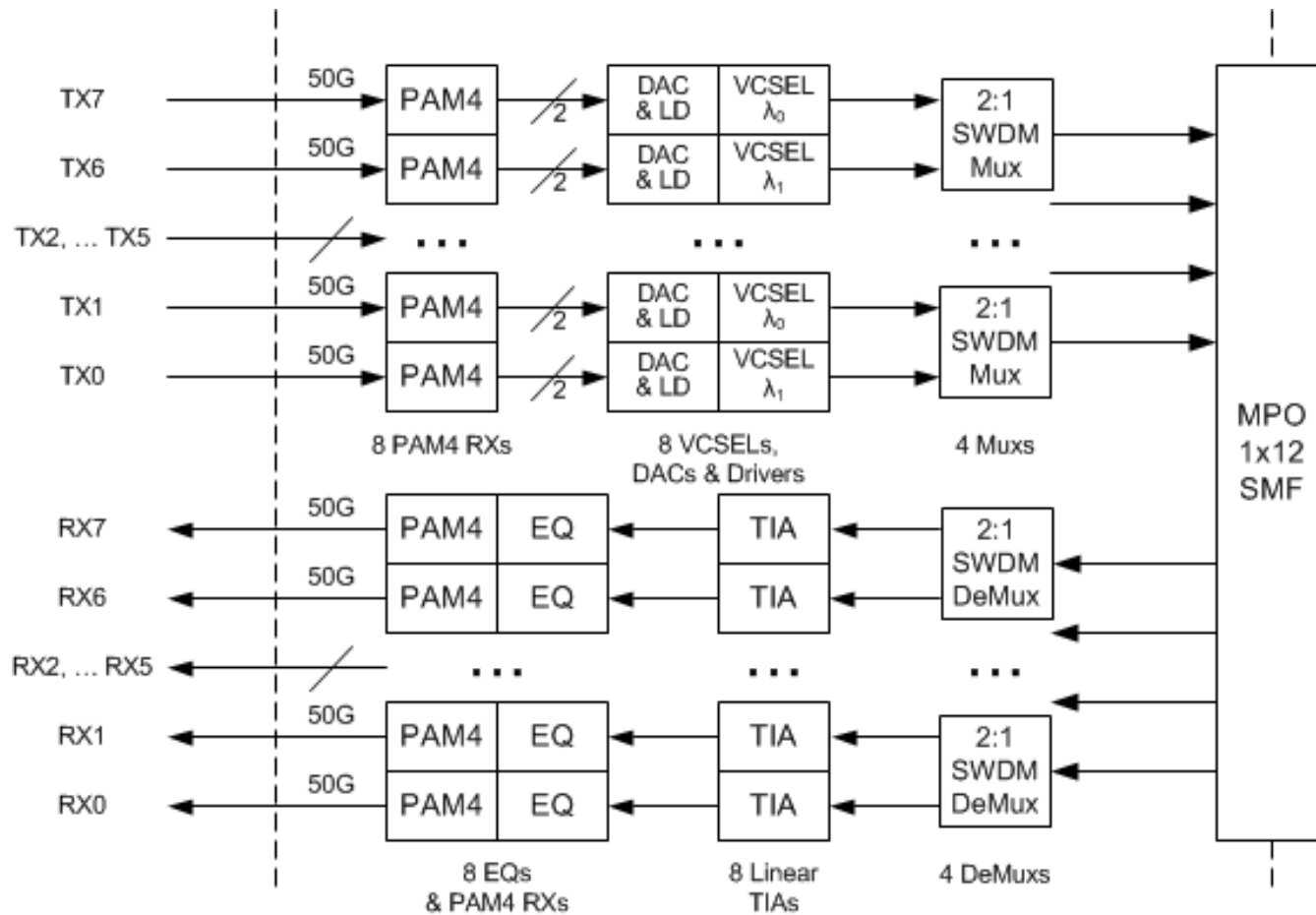


CDAUI-8

4x100GbE-SR2 & 400GbE-SR4.2



# 400GbE-SR4.2 Alt 2: Quad 2x 50G PAM-4 $\lambda$ s

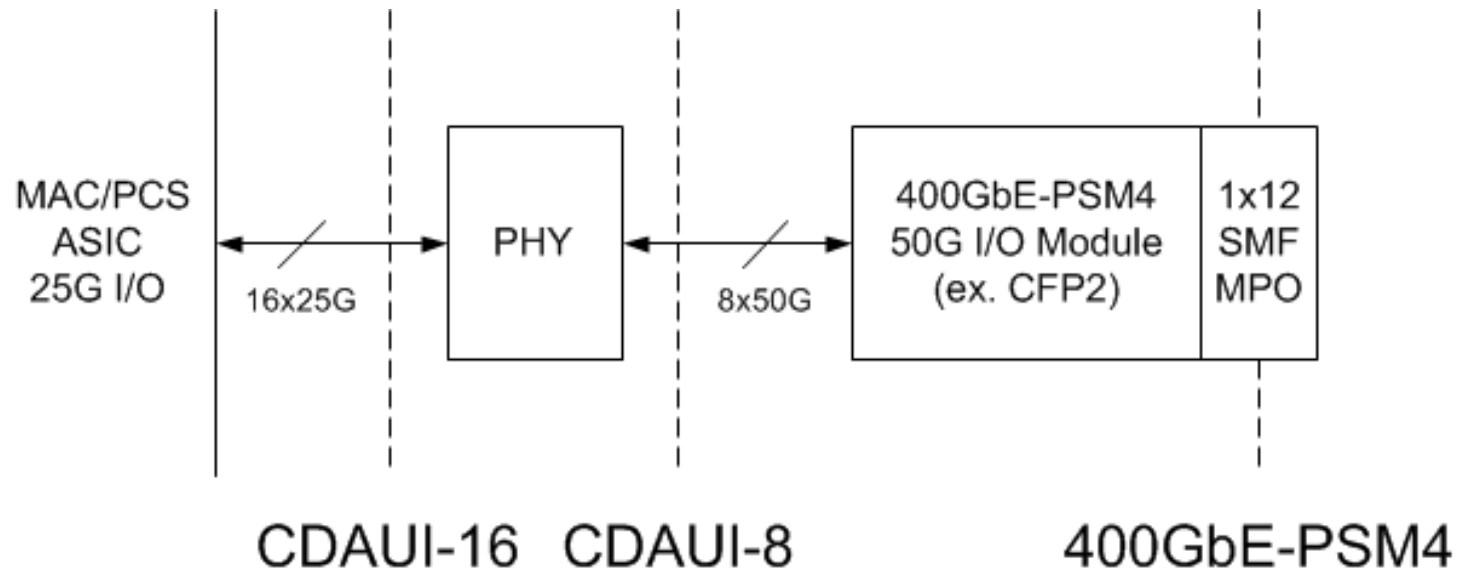


CDAUI-8

4x100GbE-SR2 & 400GbE-SR4.2

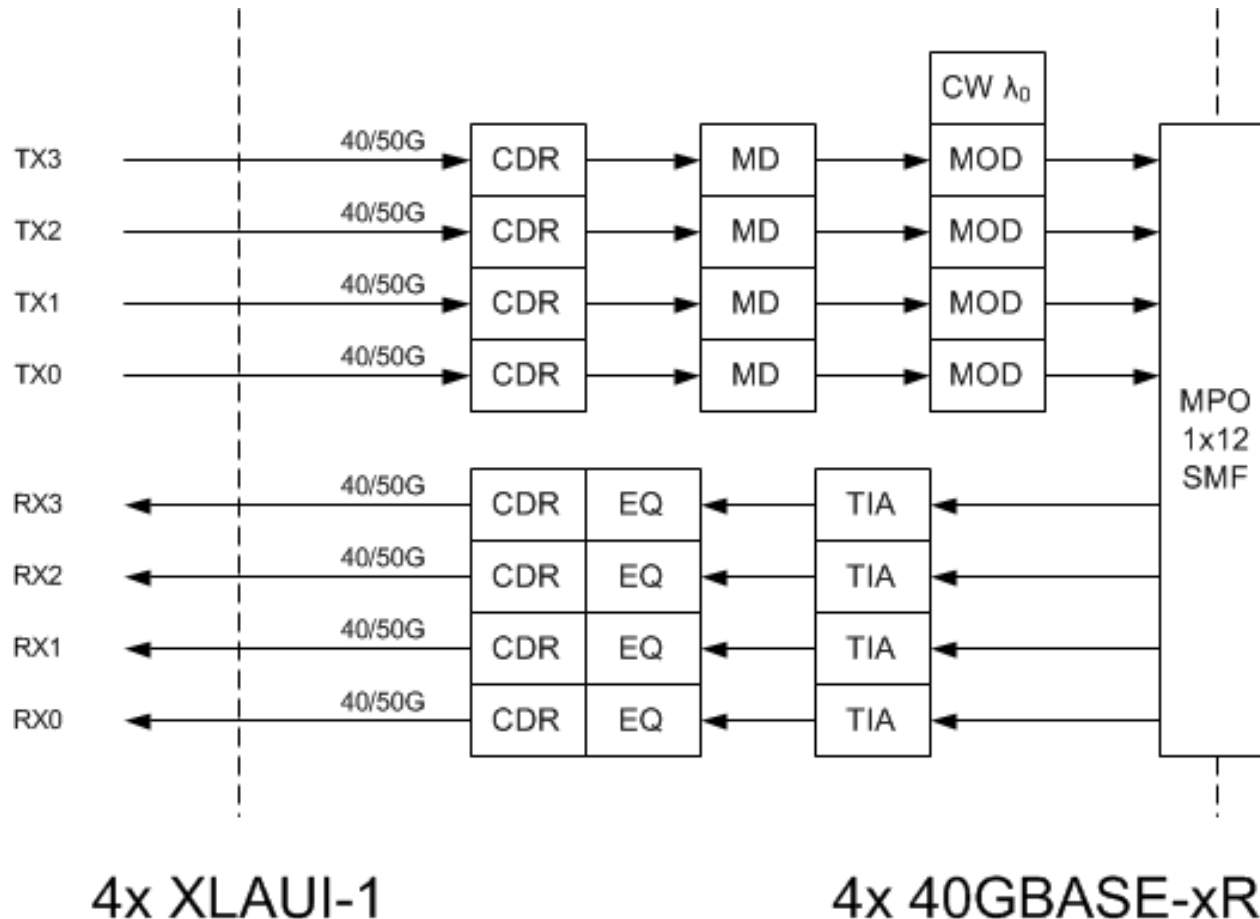
# 400G CDAUI-16 I/O ASIC Host Architecture

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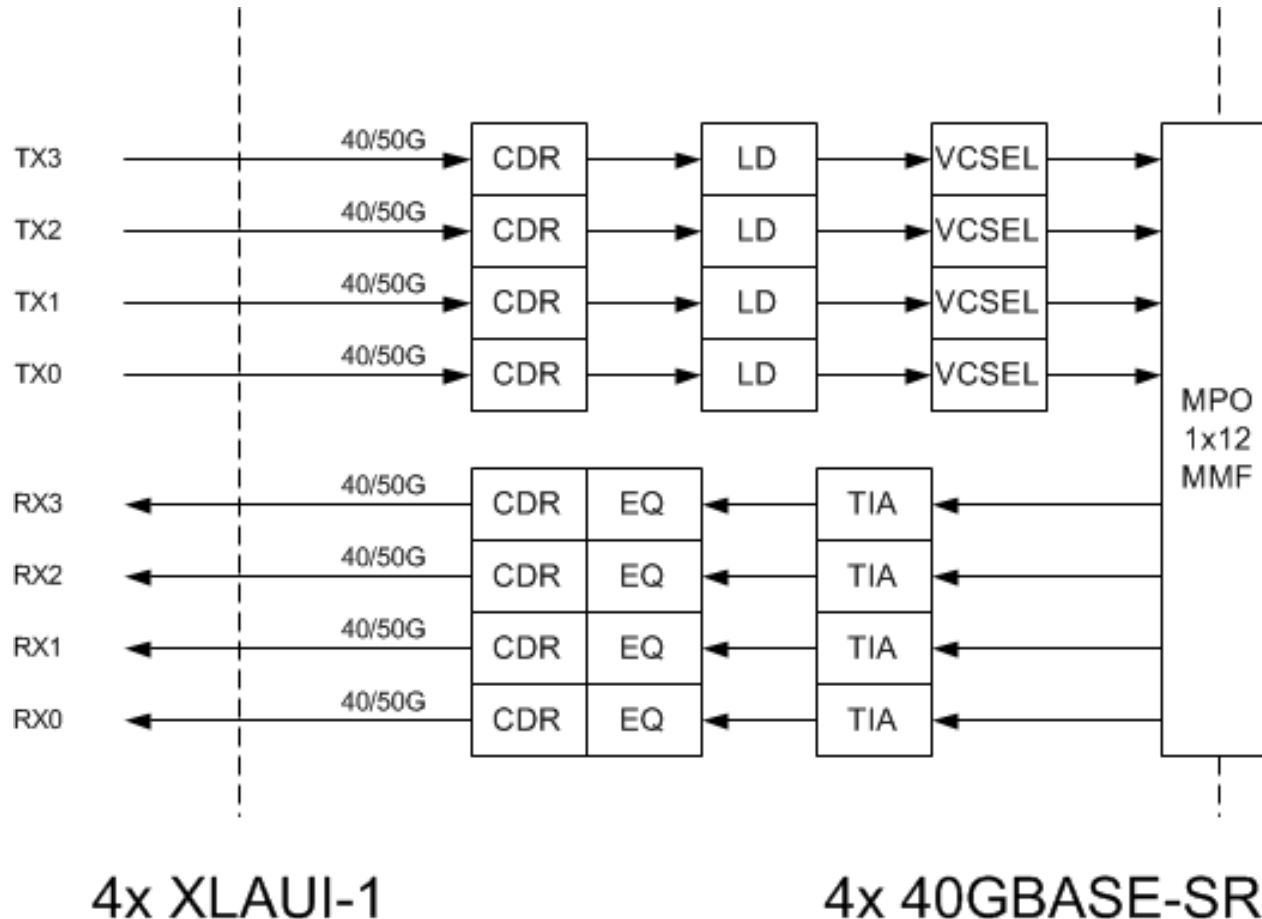
- CDAUI-16 I/O module (ex. CDP) has converter PHY inside

# 160/200G QSFP: Quad 40/50G duplex SMF



- SFP40 is single 40/50G channel
- PAM-4 alternatives shown on pages 5 & 6

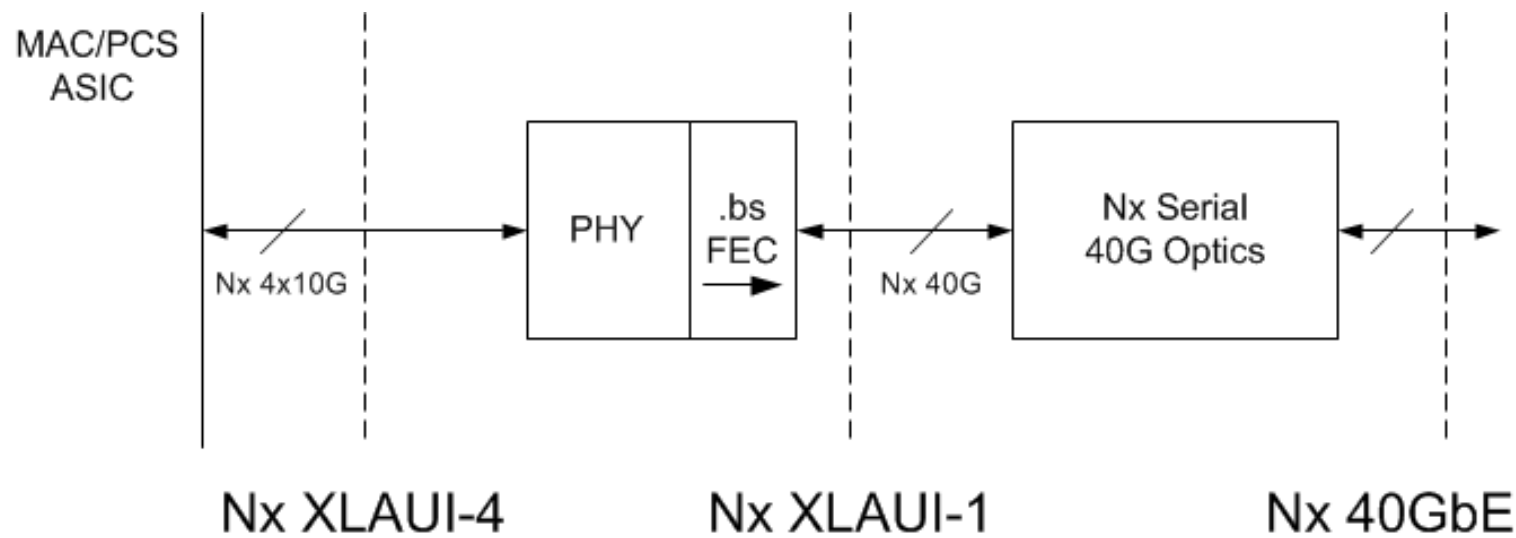
# 160/200G QSFP: Quad 40/50G duplex MMF



- SFP40 is single 40/50G channel
- PAM-4 alternative shown on page 17

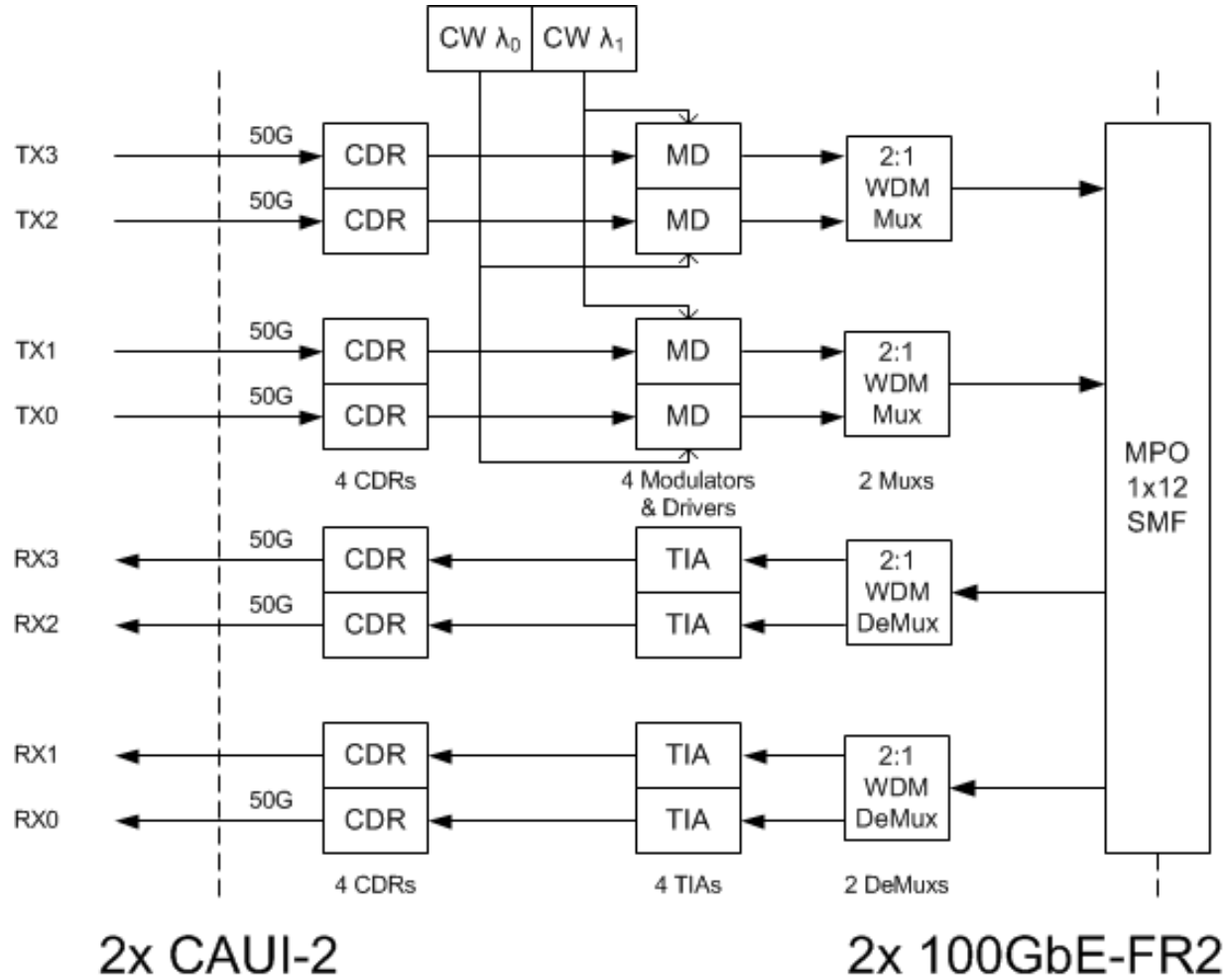
# 40G XLAUI-4 I/O ASIC Host Architecture

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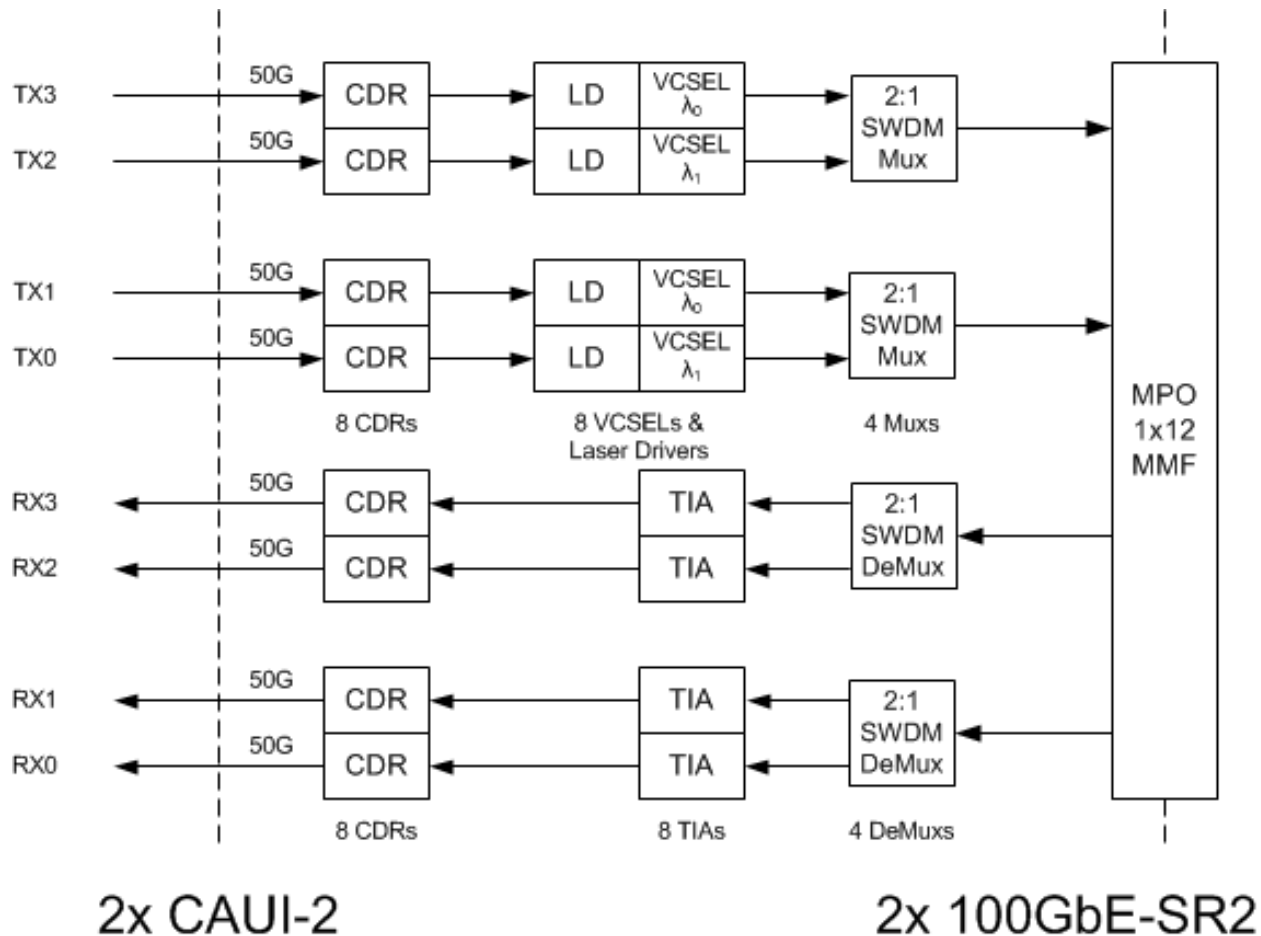
- .bs FEC may be KR4, KP4, or other
- XLAUI-4 I/O module (ex. QSFP) has converter PHY inside

# 160/200G QSFP: Dual 100G duplex SMF



- PAM-4 alternatives shown on pages 5 & 6

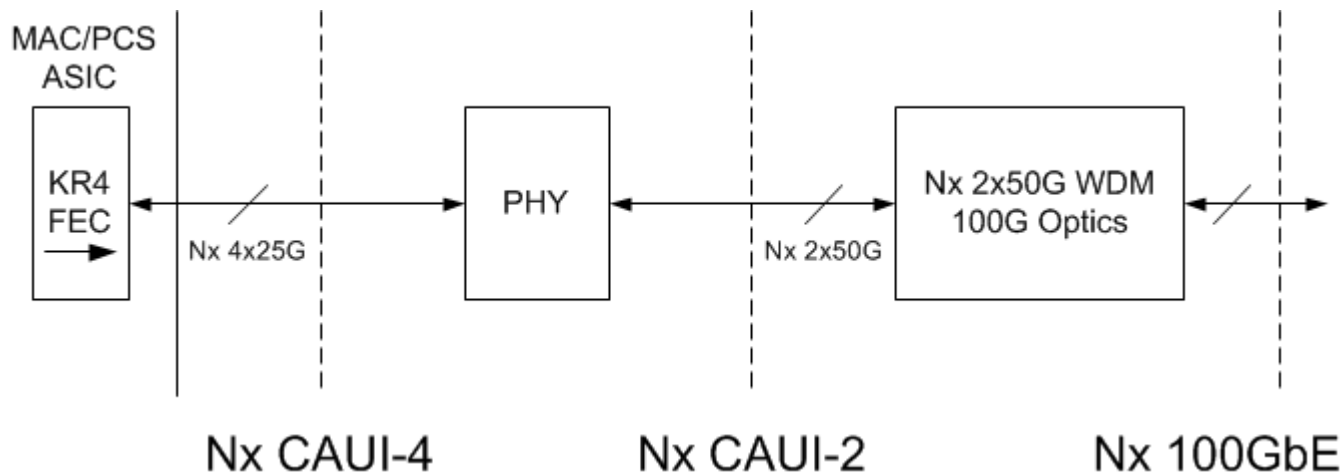
# 160/200G QSFP: Dual 100G duplex MMF



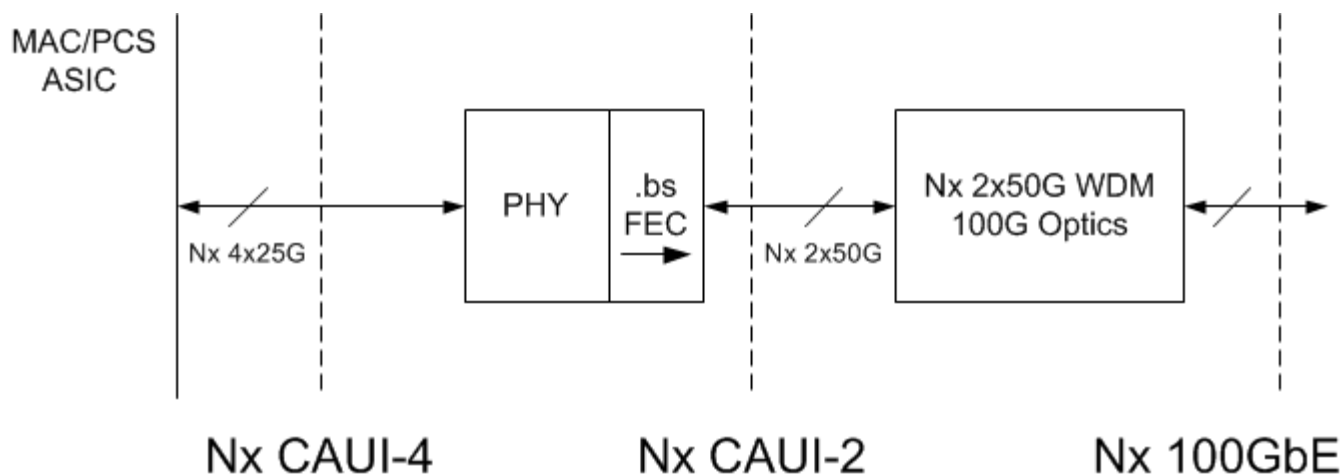
- PAM-4 alternative shown on page 17

# 100G CAUI-4 I/O ASIC Host Architecture

400G KR4  
PMD FEC



400G .bs  
PMD FEC  
other than  
KR4



- CAUI-4 I/O module (ex. QSFP) has converter PHY inside



# 400 & 4x100 Gb/s PMD Alternatives Study

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Thank you