BER-floors in 400Gb/s Ethernet SMF PMDs What are the issues?

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Contents

- Introduction
- Recap of “stassar_01a_0914_smf”, SMF Ad Hoc, 30 September 2014
- What is the potential issue? Why address it?
- Consensus?
- Q&A

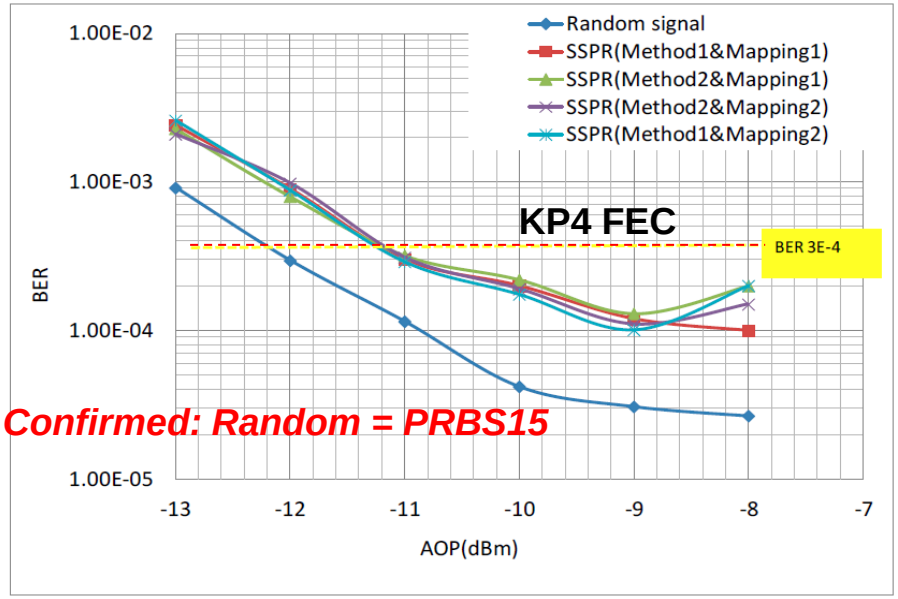
Introduction

- Topic of BER-floors in PAM4 experiments
- First some offline discussions during Ottawa IEEE802.3 meeting
- Presentation of “stassar_01a_0914_smf”, SMF Ad Hoc, 30 Sept 2014
- This presentation adds some further clarification

Recap of “stassar_01a_0914_smf”, SMF Ad Hoc, 30 Sept 2014

“Updated Considerations on 400Gb/s Ethernet SMF PMDs”

- During both San Diego (July 2014) and Ottawa (September 2014) many presentations with test results showing BER curves have been given.
- Some examples for 8x50G PAM4 and 4x100G PAM4



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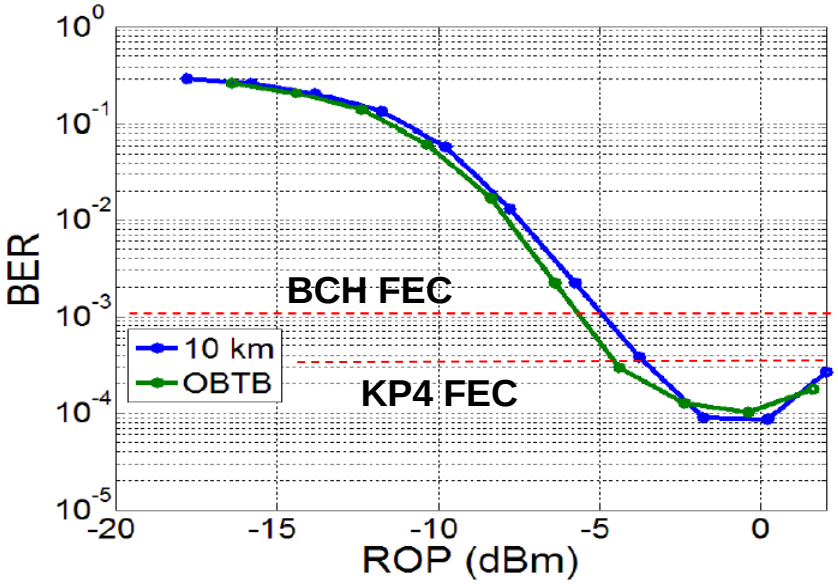

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A BER floor that close to the FEC operation point, even under “ideal” laboratory conditions, will certainly lead to unstable performance in the field under practical field conditions

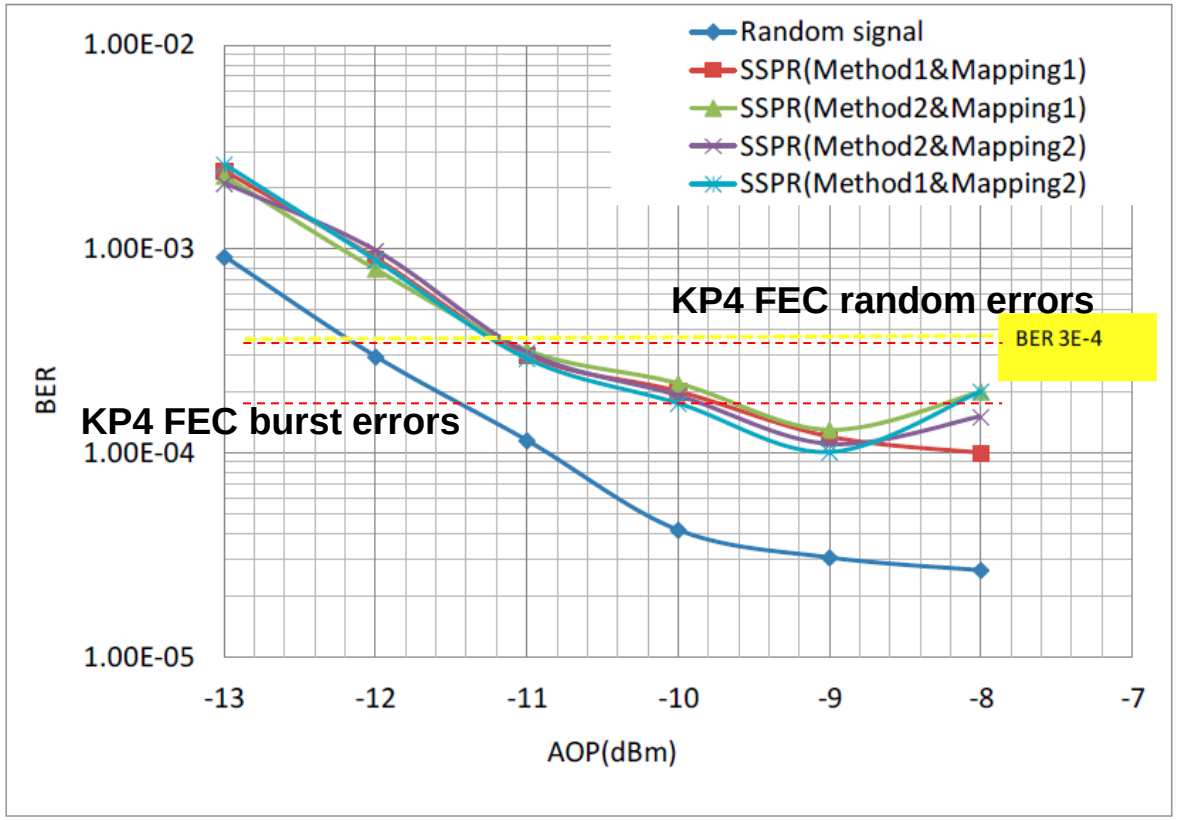
Questions raised at 30 Sept SMF Ad Hoc

- Can we now conclude that PAM4 is not usable?
- ***NO!!!***
- BUT……, it will be critical to identify the reason for these BER-floors and, when identified, show experimental results where the BER-floor is sufficiently below the operation point.
- Questions:
  - Redo both NRZ and PAM4 experiments for SSPR pattern (PRBS 2^{15}-1 is too short) in b2b configuration (to exclude dispersion effects)
  - Is there a difference between 25Gb/s, 50Gb/s and 100Gb/s PAM4?
- Preliminary assessment of PAM4 at Huawei:
  - It seems that the SNR at the receiver is NOT the limiting factor
  - It may be pure ISI from the Tx eye, which cannot be addressed by TDP

Assumptions when generating optical interface specifications

- Specification values are worst case (worst case Tx, path or channel, Rx) to meet the required BER for the specific application.
- So if a spec is defined at BER = $1*10^{-13}$, this does not mean that the link will run at this BER, but that under normal operating conditions, the transmitter AND the receiver AND the channel will never be worst case simultaneously, and the actual BER will be several decades better for an FEC based system.
- But …… to make this a valid assumption BER curves are needed to run down sufficiently far from the FEC operating point so that under practical conditions a link will run without “problems”.

Example 1, 8*50G PAM4 experiment



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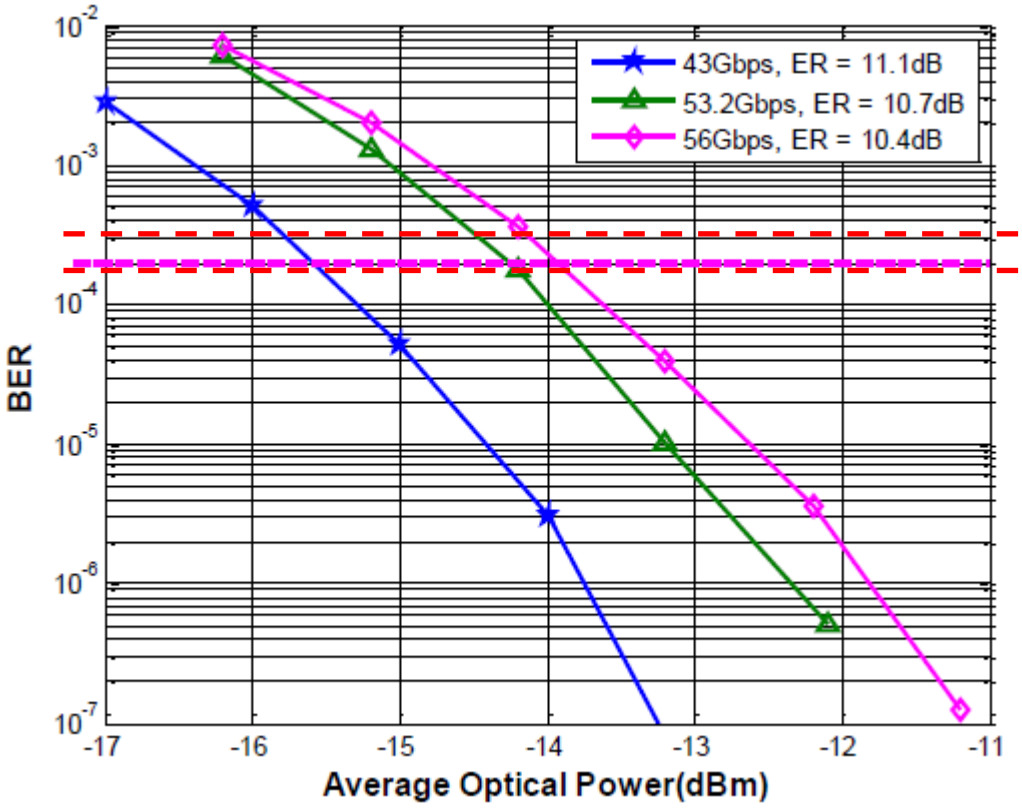
- Penalty Rx sensitivity
- KP4 FEC, random errors to burst errors, 0.6 dB penalty for PRBS15
- KP4 FEC, random errors to burst errors, 1.5 dB penalty for SSPR (red curve)
- Small variations in operating conditions cause big changes in Rx sensitivity

Example 2, 8*50G NRZ experiment



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PRBS31

- Penalty Rx sensitivity
- KP4 FEC, random errors to burst errors, 0.25 dB penalty PRBS31 (purple curve)
- Small variations in operating conditions cause small changes in Rx sensitivity

Issues with BER-floors fairly close to FEC operating point

- When we see BER-floors in experiments, under limited testing conditions like PRBS15, zero dispersion, zero jitter, etcetera,
  - If the floor is a factor of 10 below the KP4 FEC threshold we would expect the output BER to be $7*10^{-29}$
  - However, for normal variations of operational conditions (PRBS length, voltage, temperature, chromatic dispersion, jitter, the exact decision threshold of the CDR, etcetera) the floor may well show more than a factor of 10 variation in level.
  - We should be careful that we will not be bitten by this when we deploy practical systems
  - And that we would not meet market expectations that IEEE802.3 will develop Ethernet specifications that will enable development, manufacturing and deployment of very robust Ethernet technologies.

Confirming the issue

- Do we have consensus that before potentially choosing PAM4 we need to:
  - Get a good understanding that we will be able to design a practical PAM4 system that will have sufficiently robust BER performance under low-cost, high-volume manufacturing conditions
  - Identify that there is an acceptable error floor level (that doesn't move strongly up and down for small system variations) that we don't need to worry about
- Therefore we need to do further testing under varying test conditions and understand also what the difference is in BER-floor level between 50Gb/s and 100Gb/s PAM4

Q & A

Thank you