Further thoughts and inputs on 400Gb/s Ethernet SMF PMDs

Peter Stassar

SMF Ad Hoc, 18 November 2014

HUAWEI TECHNOLOGIES CO., LTD.

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Take-aways from San Antonio meeting BER-floor analyses in PAM4 experiments

- "*Error floor is common in today's coherent systems*"
  - tipper_3bs_01a_1114 and way_3bs_01a_1114
  - Yes, but those are proprietary and not multi-vendor interoperable
- "*We just need to understand and bound the raw error rate*"
  - Yes, so the floor shouldn't move up/down strongly for regular system variations
- Error-floor for 56 Gb/s PAM4 should be around $1x10^{-6}$.
  - way_3bs_01a_1114
  - Yes, even for SSPR testing (see updated test results)
- Error-floor for 112 Gb/s PAM4 should be around $1x10^{-4}$.
  - way_3bs_01a_1114
  - Yes, consistent with all experimental results

Take-aways from San Antonio meeting
BER-floor analyses in PAM4 experiments, continued

- Error-floor for 56 Gb/s PAM4 should be around $1x10^{-6}$.
  - If experimentally confirmed to be stable then ~$3x10^{-4}$ can be appropriate FEC operating point.

- Error-floor for 112 Gb/s PAM4 should be around $1x10^{-4}$.
  - If experimentally not improved appropriate FEC operating point must be above $1x10^{-3}$

Take-aways from San Antonio meeting, FEC performance

- anslow_3bs_02_1114:
  - RS FEC schemes have similar (closely spaced BER curves) FEC performance for random and burst errors.
  - BCH FEC schemes have quite different FEC performance for random and burst errors, with really poor burst performance.
- DMT baseline proposals for 500m, 2km and 10km all claim to need BCH FEC with 3.3×10^{-3} FEC operating point.
- 4x100Gb/s PAM4 baseline proposal for 500m (welch_3bs_01b_1114) claims FEC operating point of 2.1×10^{-5}. How to fit with floor 1×10^{-4}?
- 4x100Gb/s PAM4 baseline proposal for 2km (mason_3bs_01a_1114) claims FEC operating point of 2.1×10^{-4}. How to fit with floor 1×10^{-4}?
- Need further info on FEC complexity, size, power consumption, latency

Take-aways from San Antonio meeting, PAM4 power budget

From: stassar_3bs_01b_1114:

	Realistic specification for 2km duplex SMF	Realistic specification for 500m PSM4 SMF	Unit
Tx average, Before Mux	+6	+4	dBm
Tx OMA (01-00), Before Mux	+4	+2	dBm
Tx OMA (01-00) min	+2	0	dBm
TDP	3	3	dB
Tx OMA (01-00) – TDP min	-1	-3	dBm
Channel insertion loss	4	4	dB
Rx ROP OMA (01-00) with KP4 FEC Specification Value	-5	-7	dBm

Based upon feedback and mason_3bs_01a_1114, needs to be corrected because of non-infinite ER, e.g. 6 dB.

Further considerations on 112Gb/s PAM4 power budget

- Rx sensitivity test value in stassar_3bs_01_0714: -6.4dBm @ $3x10^{-4}$, average power.
- Assume -5dBm (average power) for stable factory spec.
- Translates into -7dBm OMA (01-00) for infinite ER (assuming 5dB modulation penalty) or -9dBm OMA (01-00) for ER = 6dB

Updated considerations for 112Gb/s PAM4

Corrected values for ER = 6 dB.

	Realistic specification for 2km duplex SMF	Realistic specification for 500m PSM4 SMF	Unit
Tx average, Before Mux	+6	+3	dBm
Tx OMA (01-00), Before Mux	+2	-1	dBm
Tx OMA (01-00) min	+0	-3	dBm
TDP	3	3	dB
Tx OMA (01-00) – TDP min	-3	-6	dBm
Channel insertion loss	4	3	dB
Rx ROP OMA (01-00) with KP4 FEC Specification Value	-7	-9	dBm

- For 2km question about feasibility of Tx power of +6 dBm (average) the same
- For 500m question about feasibility of Tx power of +3 dBm (average), 1dB lower

Further test results on error performance of 56Gb/s PAM4

Corrected SSPR testing conditions

Assumptions

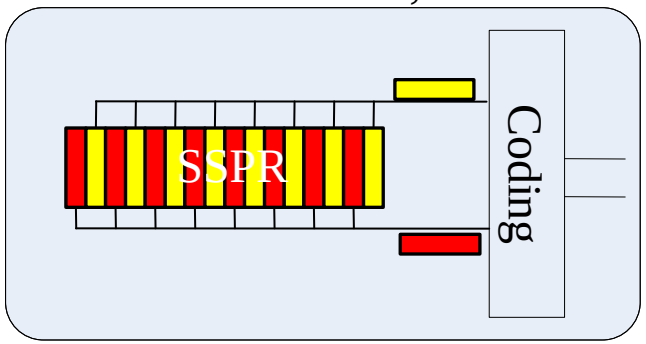
The assumptions used in the PAM4 analysis contained in this presentation were:

- The test pattern bits are divided into two bit symbols xy which is the bit x followed by the bit y
  - E.g. 011011001010 becomes 6 symbols: 01 10 11 00 10 10
- The patterns were also analysed one bit shifted
  - E.g. x011011001010y becomes 7 symbols: x0 11 01 10 01 01 0y
- The two bit symbols were mapped to PAM4 levels as either:
  - {11,10,01,00} map to {+1,+1/3,-1/3,-1}
  - {10,11,01,00} map to {+1,+1/3,-1/3,-1} as for 100GBASE-KP4

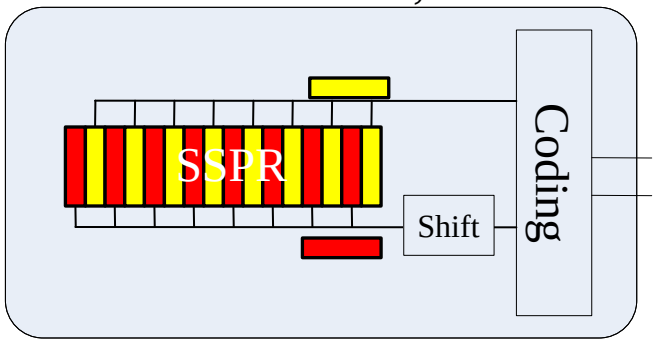
The results for baseline wander are presented first (slides 6 to 8) followed by clock content (slides 9 to 11).

anslow_3bs_03_0714

Method 1, no shift



Method 2, 1 bit shift



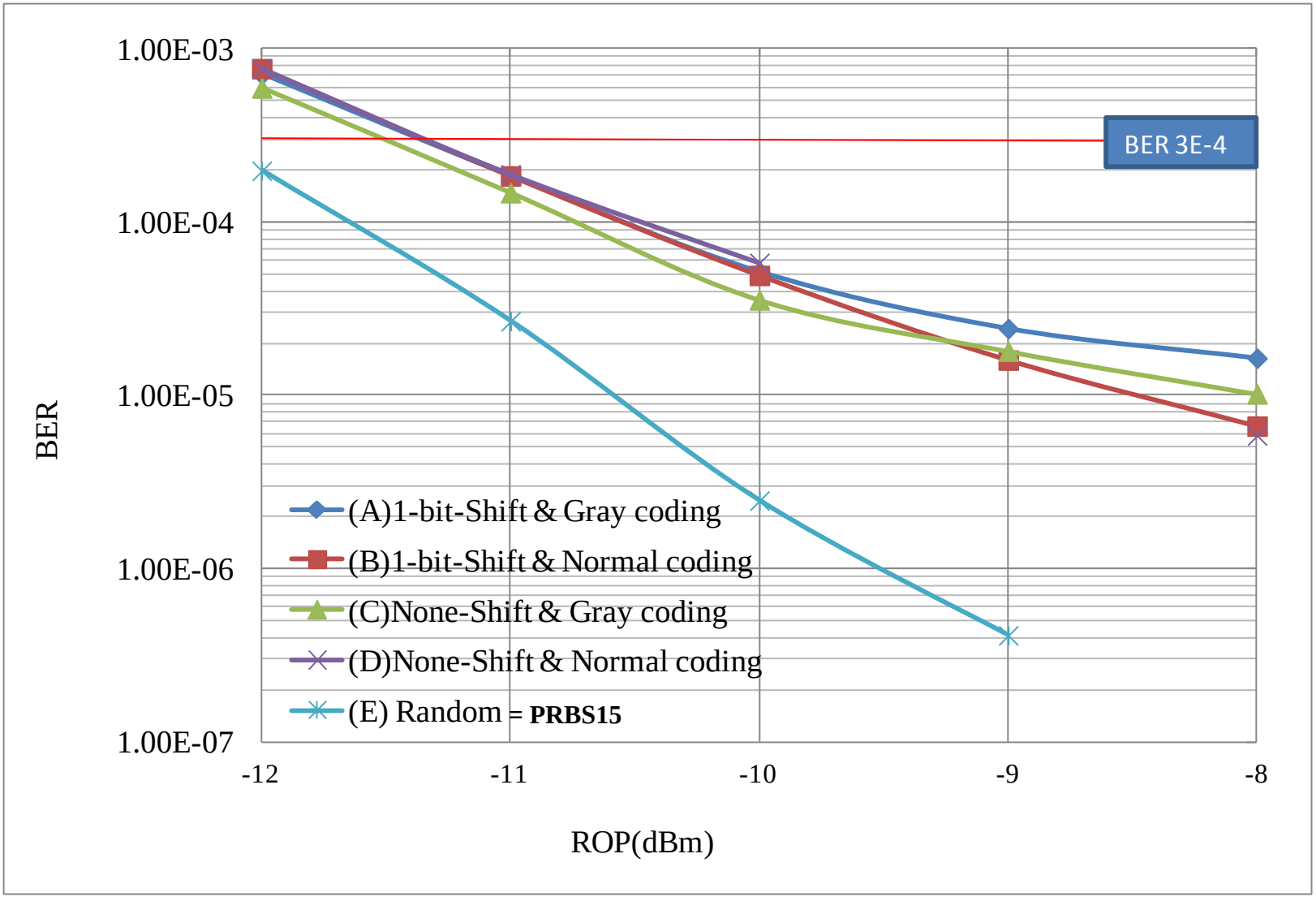
Five scenarios:

(A) 1-bit-Shift & Gray coding
(B) 1-bit-Shift & Normal coding
(C) No Shift & Gray coding
(D) No Shift & Normal coding
(E) PRBS15

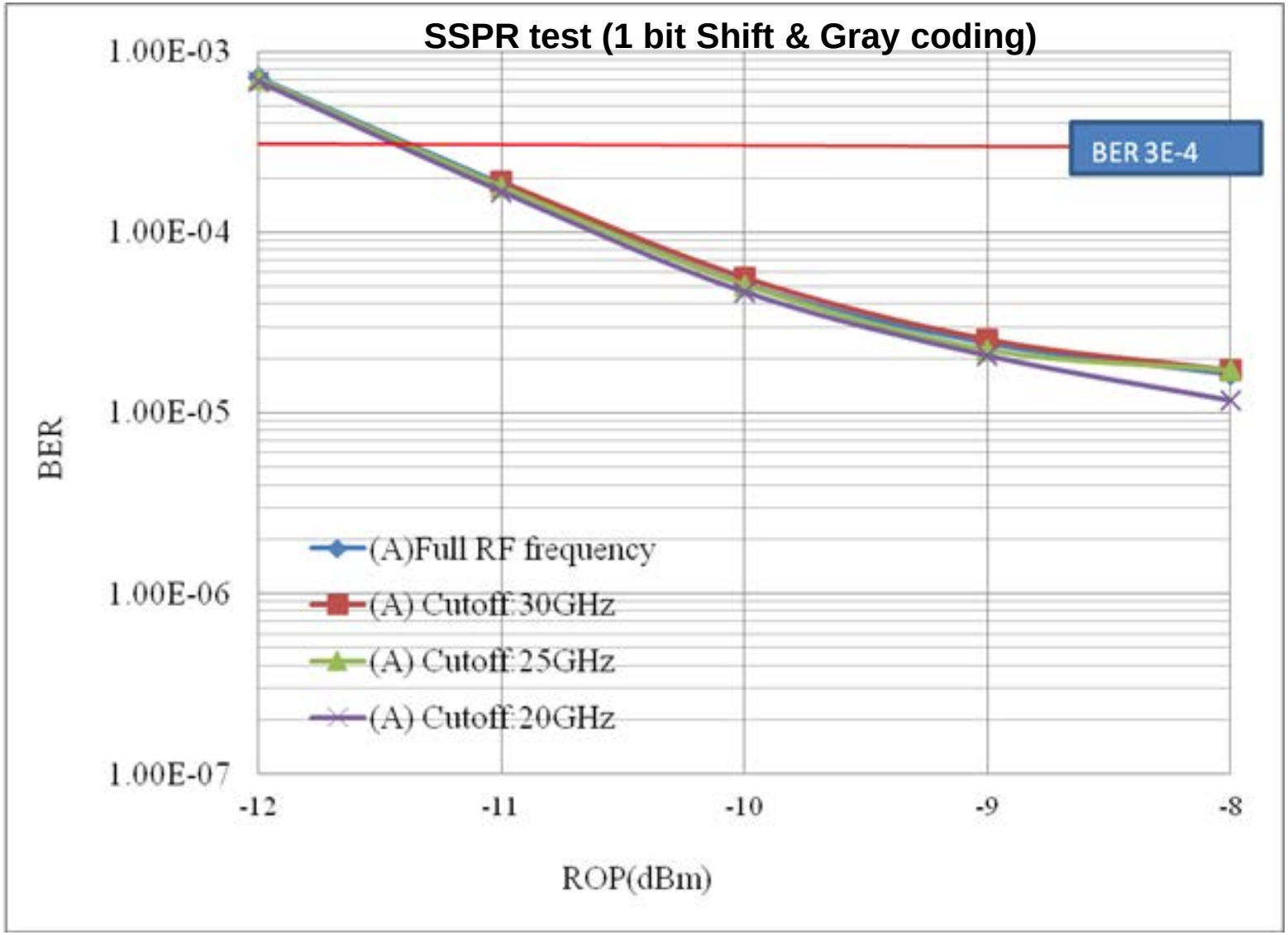
Mapping 1	
00	−3
01	−1
10	+1
11	+3

Mapping 2	
00	−3
01	−1
11	+1
10	+3

Further test results of 56Gb/s PAM4, continued



Further test results of 56Gb/s PAM4, continued 2



Observations from updated 56 Gb/s PAM4 test results

- For PRBS15 error floor < $1x10^{-6}$, consistent with other test results
  - Slope similar to other test results
- For SSPR patterns, error floor higher than for PRBS15, but around $1x10^{-5}$ or lower
  - Slope lower than other test results
- BER curves for ROSA BW between 20 GHz and 30 GHz similar, so no need for high BW ROSA and actually slightly better for 20 GHz.

Follow-up

- FEC experts need to provide information on alternative FEC schemes:
  - Much better performance than KP4 FEC.
  - Similar performance for random and burst errors.
  - Limited complexity and power consumption increase
- Need further test results on BER performance for 56 Gb/s PAM4, 112 Gb/s PAM4 and 56 Gb/s NRZ under SSPR testing
  - Importance of SSPR testing demonstrated in anslow_3bs_03_0714
- Need alternative SSPR test for 112 Gb/s DMT to investigate error resilience

Q & A

Thank you