# Transmitters Compliance and Receivers Stress Sensitivity

**Ali Ghiasi**
**Ghiasi Quantum LLC**

**802.3bs Adhoc Meeting**

**April 19 - 2016**

# Contributors

- **Greg Le Cheminant – Keysight**
- **Pavel Zivny – Tektronix**
- **Marco Mazzini - Cisco**

Updated presentation from http://www.ieee802.org/3/bs/public/15_07/ghiasi_3bs_02a_0715.pdf

# Overview and Challenges

- **Overview of legacy test methods**
  - TDP (CL52, 87, 88)
  - VECP (CL 52, 87, 88)
  - TDEC (CL 95)
- **Possible SMF test method**
  - TDEC like leveraging CDAUI-8 (120D/E)
- **Challenges**
  - As we are struggling to define TDP/TDEC another big issue is lack of agreement on the reference EQ
    - Some believe a simple as CTLE is enough and other view 7+ tap T/2 FFE is necessary
  - Either TDEC or TDP require an agreement of reference receiver
  - A CTLE only reference receiver may allow building a real HW reference receiver for TDP testing and overcome scope limitation to capture noise with FFE EQ for TDEC calculation
  - This is straw proposal with significant amount of work ahead of us to verify correlation and compliance!

# The TDP Test Methodology Components

- **Fast optical transmitter with Tr/Tf ~1/3 Baud period**
- **Hardware CRU with build in reference equalizer “Golden Receiver”**
- **Stress generator + reference transmitter**
- **How DUT transmitter is tested?**
  - Data pattern is PRBS31 or valid Ethernet frame
  - In addition to usual optical parameters device is tested for high probability effect with eye mask at 1E-3
  - Reference transmitter is tested with Golden Receiver to establish TDP baseline
  - Reference transmitter replaced with DUT transmitter to determine its TDP penalty.
- **How DUT receiver is tested?**
  - Data pattern is PRBS31 or valid Ethernet frame
  - The stress generator adjusted to meet condition of stress sensitivity such as VECP, J2, and J9
  - DUT receiver is tested with Stress Generator at specified input power to see if the required BER is met.
- **For SMF getting fast MZM and creating an stress generator should feasible with high quality lab grade components, but HW CRU with reference EQ require custom development that may never see the light!**
- **TDEC for SMF is equivalent of replacing HW CRU+EQ with real time scope or even sampling scope.**

# TDP Test Setup for 100Gbase-LR4

- **TDP is a comprehensive transmitter test method as shown below**
  - The bases for the TDP test is in CL 52.9.10
  - TDP require a reference transmitter to establish reference BER as defined by
    - **Rise/fall times of less than 12 ps at 20% to 80%.**
    - **The output optical eye is symmetric and passes the transmitter optical waveform test of 88.8.8.**
    - **In the center 20% region of the eye, the worst-case vertical eye closure penalty as defined in 57.8.11.2 is less than 0.5 dB.**
    - **Total Jitter less than 0.2 UI peak-to-peak.**
    - **RIN of less than –138 dB/Hz**
  - The drawback of the TDP has been the requirement to have a more strengthen/faster transmitter.

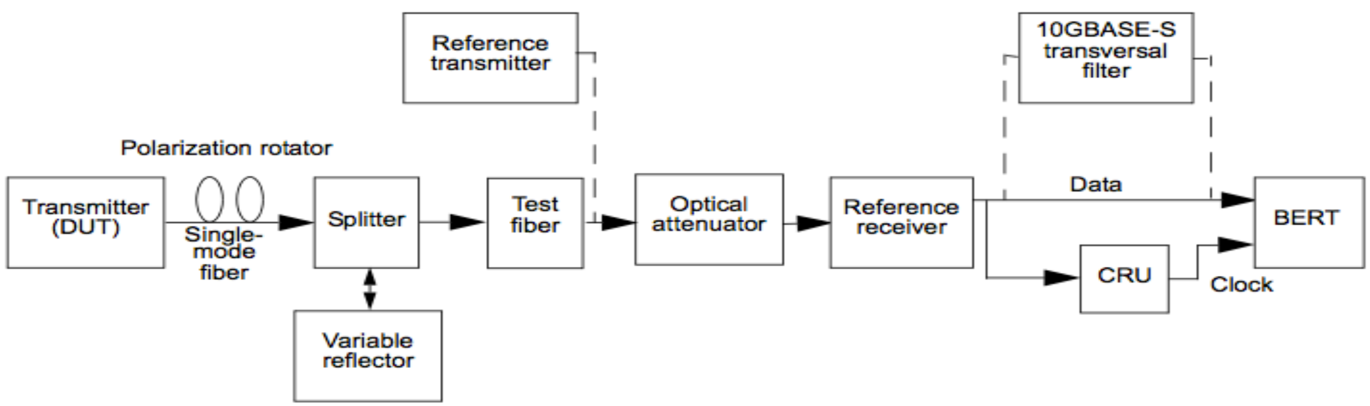



**Figure 52–12—Test setup for measurement of transmitter and dispersion penalty**

# TDP Test Setup for 100Gbase-LR4 Cont.

- **To establish TDP measurement it is tested against a reference receiver with following characteristics:**
  - Reference optical receiver has 4th order BT with 19 GHz BW
  - Sensitivity of reference receiver limited by Gaussian noise
  - Receiver has minimum offset, DJ, hysteresis, deadlock, setup/hold, and other distortions
  - Nominal sensitivity S is measured with the reference transmitter and correct for any reference transmitter impairments
  - Sensitivity S measured at center of eye which is half way between left/right sampling point where BER is 1E-3
  - The Clock recovery unit CRU has corner frequency of 10 MHz with a slope of 20 dB/dec.

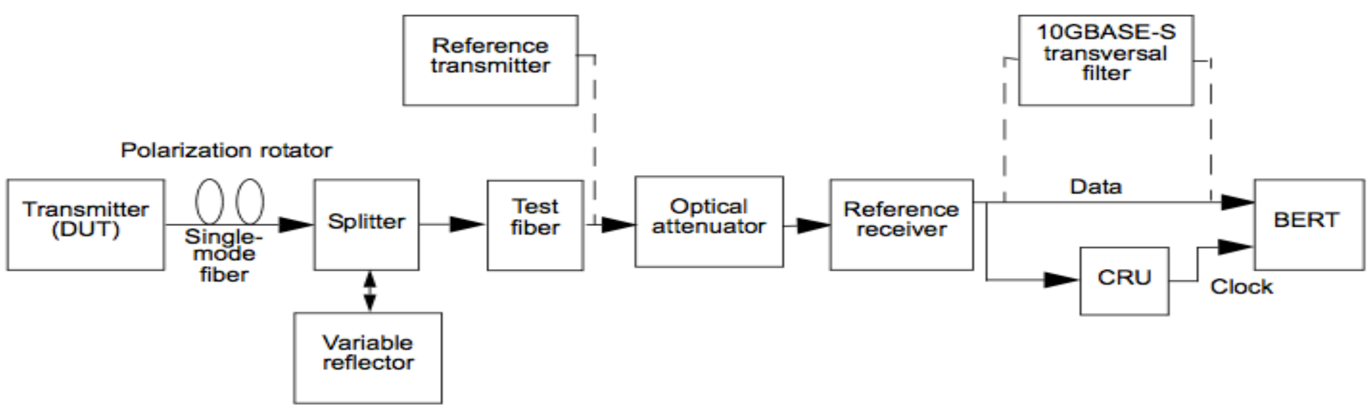



**Figure 52–12—Test setup for measurement of transmitter and dispersion penalty**

# TDP Test Setup for 100Gbase-LR4 Cont.

- **VECP (Vertical Eye Closure Penalty) is a test parameter to calibrate reference TP3 signal for DUT receiver stress sensitivity measurement**

$$VECP = 10 \times \log_{10} \frac{OMA}{A_0} \qquad (dB)$$

A0 is the amplitude of the eye opening from the 99.95$^{th}$% of the lower histogram to 0.05$^{th}$% of the upper histogram.

OMA is the optical modulation amplitude.

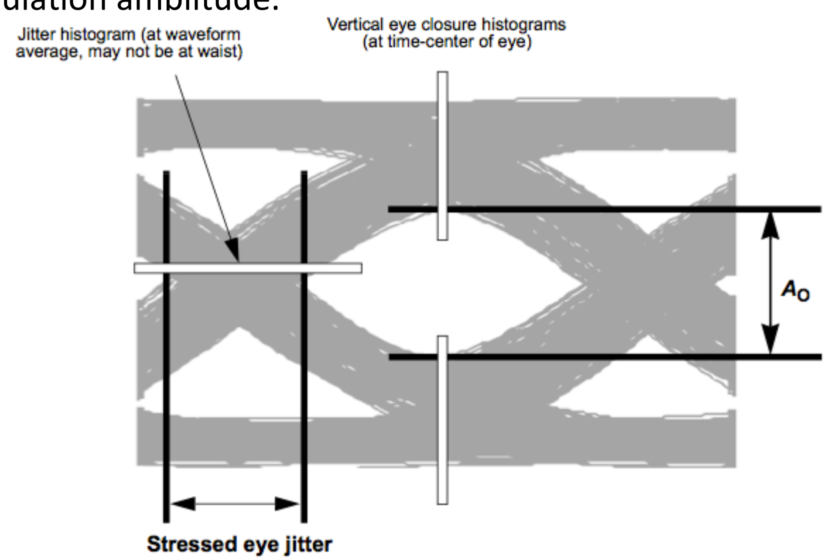



**Figure 87–4—Required characteristics of the conformance test signal at TP3**

# Transmitter and Dispersion Eye Closure (TDEC) CL-95

- **TDEC is a measure of transmitter VEC based on vertical histogram through O/E and worst case optical channel**
  - Extend the VECP test method to include the dispersion and noise penalty
  - TDEC test method is defined in 95.8.5.2
  - TDEC as defined in CL 95 includes penalty associated with modal noise and MPN
  - For SMF link due to complex interaction of chip and dispersion need to include the fiber
  - Even with TDEC still need stress generator and a reference transmitter to test DUT receivers.

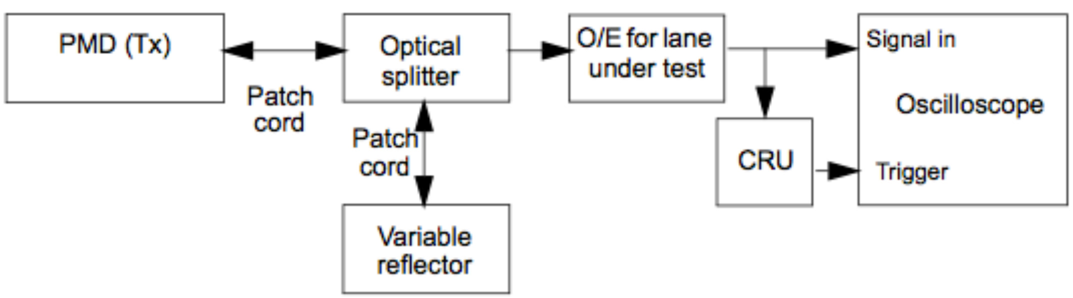



Figure 95–3—TDEC conformance test block diagram

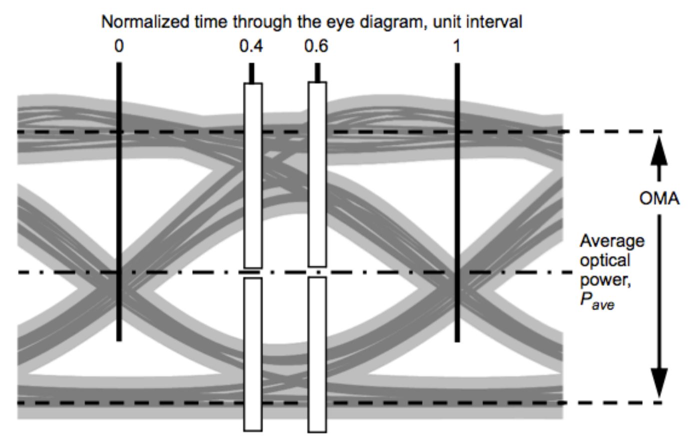
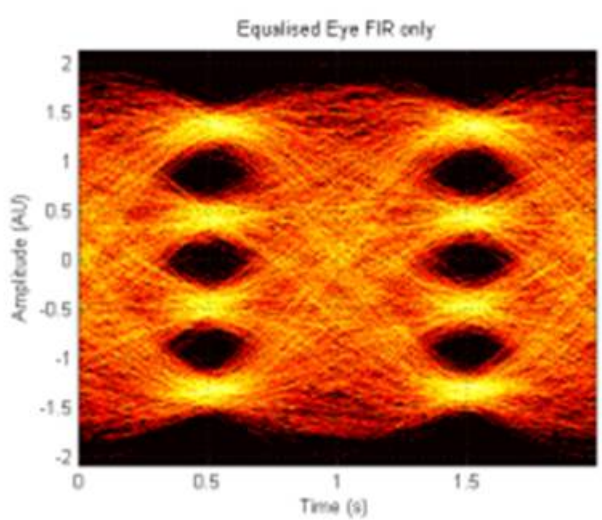



Figure 95–4—Illustration of the TDEC measurement

# Reviewing Previous Work for Potential Reference Equalizer

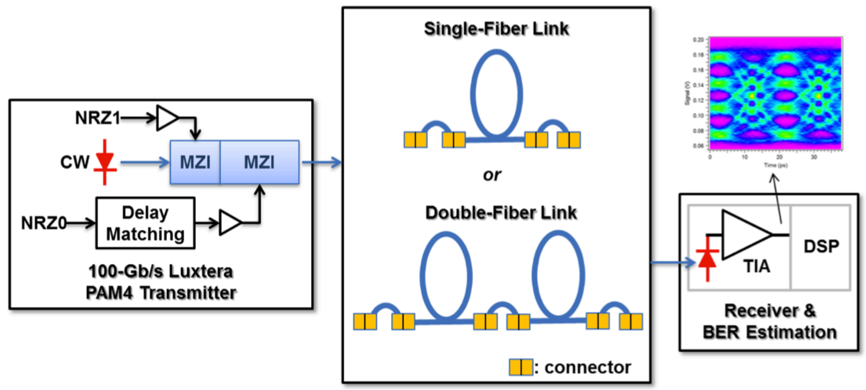
- **Typically a receiver with 4-8 taps T/2 FFE with 1-2 taps of DFE is sufficient to equalize band limited OE and the electrical driver impairments**
  - Uses 21 tap FFE, AWG with 23 GHz limiting the overall BW for 100G PAM
    - http://www.ieee802.org/3/bs/public/14_09/way_3bs_01a_0914.pdf
  - Uses 22 taps T/2 with 35 GHz LiNO3 MZM and 32 GHz receiver
    - http://www.ieee802.org/3/bs/public/14_09/mazzini_3bs_01_0914.pdf
  - Updated result Way/Mazzini showed 14 T/2 FFE having identical performance to 22 T/2 FFE
    - http://www.ieee802.org/3/bs/public/15_01/way_3bs_01a_0115.pdf
  - Even more updated results (below) contributed by Mazzini indicate 7 T/2 FFE is adequate with ~0.4 dBo penalty compare to 22 tap FFE




# Reviewing Previous Work for Potential Reference Equalizer Cont.

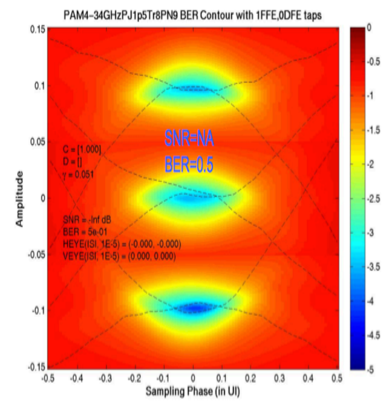
– Luxtera MZM TX with ~32 GHz BW (~7.2 ps Tr/Tf) coupled to 28 GHz PIN/TIA operating at 100 Gb/s PAM4, results published were with 11 tap FFE but the eye after the TIA indicate shorter FEE might have be been adequate

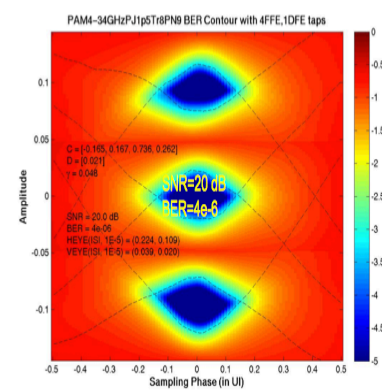
- P. V. Mena, E. Ghillino, Synopsys, Inc., A. Ghiasi, Ghiasi Quantum LLC, B. Welch, Luxtera, Inc., M. S. Khaliq, DET - Politecnico di Torino, and D. Richards, College of Staten Island, 100-Gb/s PAM4 Link Modeling Incorporating MPI, IEEE Optical Interconnect 2015




– Optsim simulation result for 8 ps optical transmitter with 1.5 ps DJ and MPI for 6x30 dB connectors and coupled to 34 GHz PIN/TIA show 4 T/2+ 1DFE perform best but 5-7 T/2 could be reasonable alternative

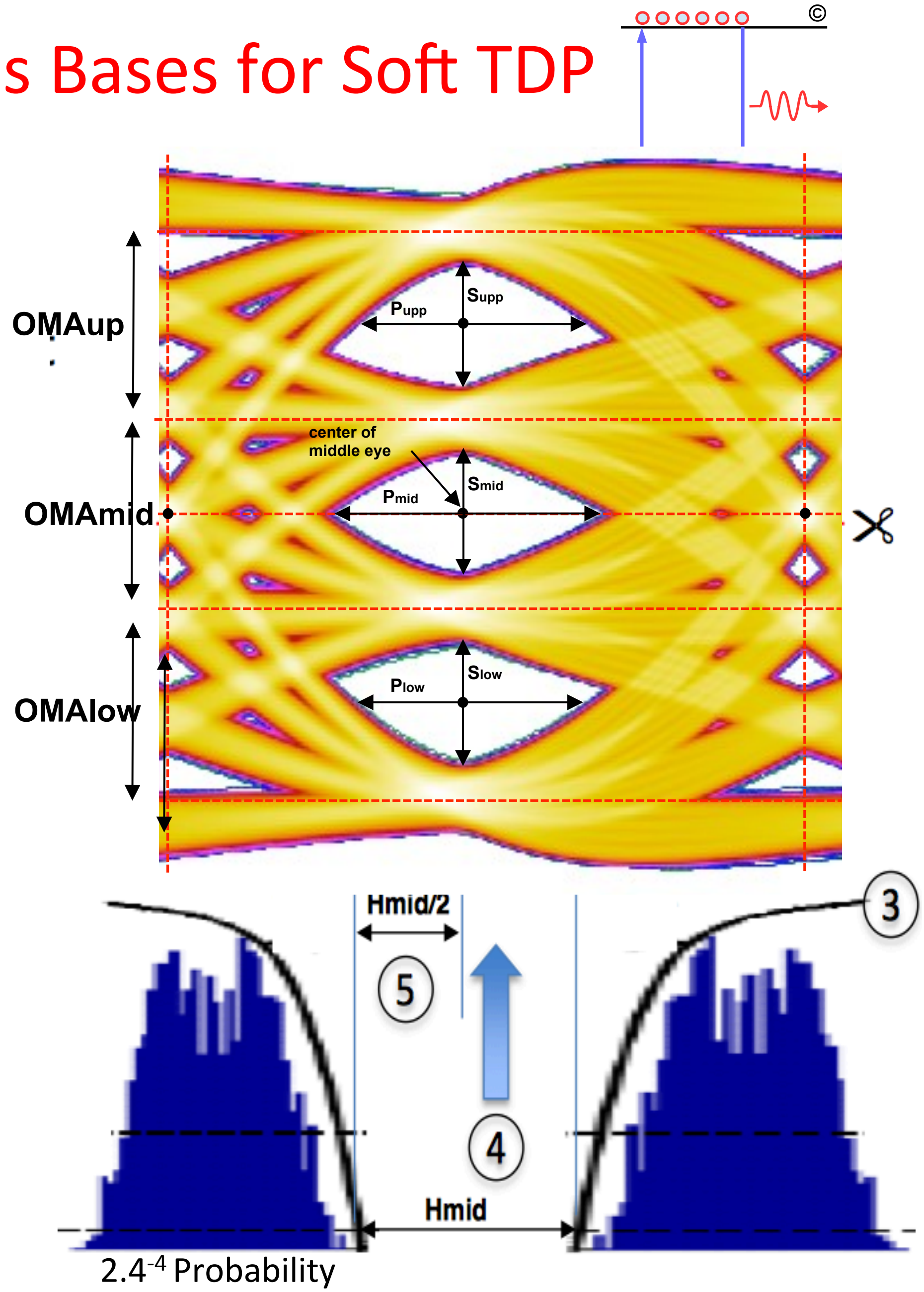
http://www.ieee802.org/3/bm/public/nov12/ghiasi_01a_1112_optx.pdf



# Re-use CDAUI-8 Test Method as Bases for Soft TDP "STDP"

- **Reuse Annex 120E method to:**
  - Capture (> 4 million symbols)
  - Pattern PRBS31Q with real time capture the start capture should be on pattern 23 bits or longer
  - If shorter SSPRQ does not exhibit pattern sensitivity real time scope capture full bit patern, on sampling scope averaging may be an acceptable alternative if non-synchronous noises can be captured
  - Instead of reference CTLE apply 7 tap T/2 FFE
  - Construct CDFs of eye edges at zero crossing
  - Hmid = $1e^{-6}$ inner eye width
  - Locate center of middle eye at Hmid/2
  - Optical link Hmid probability is $2.4e^{-4}$
  - All measurements are performed with max fiber reach at maximum specified fiber dispersion
- **An alternate method is to use TDEC calculation base on CL95**
  - With HOM receiver having linear front end Cu diamond mask looks like reasonable representation of the link.



# STDP (Eye Width and Eye Height Measurement Method)

This subclause describes common measurement tools and methodologies to be used for Clause 121 and 122 measurement.
TDEC eye diagrams are measured using a linear optical-electrical reference receiver. The optical-electrical reference receiver response combined with the scope front end should match a fourth-order Bessel-Thomson low-pass filter response with 3 dB bandwidth of 0.565xBaudrate. The reference equalizer is a 7 taps T/2 FFE either implemented on the scope directly or by hardware implementation, in either case the FFE is optimized with MMSE for maximum eye opening or TDEC. TDEC include dispersion therefore the test include maximum fiber reach at maximum dispersion:

1) Capture SSPRQ using a clock recovery unit with a corner frequency of 4 MHz and slope of 20 dB/decade and a minimum sampling rate of 3 samples per bit. Collect sufficient samples equivalent to at least 4 million PAM4 symbols to allow for construction of a normalized cumulative distribution function (CDF) to a probability of 10-6 without extrapolation. Scope must either operate in real time mode by capturing 4 million PAM4 symbol directly or in sampling mode with persistence to capture the noise.

2) Apply reference to the captured signal or pass the signal through 7 tap T/2 FFE. Optimize the FFE taps for maximum eye opening for all 3 eyes.

3) From the equalized signal from step 2) to construct the CDF of the jitter zero crossing for both the left edge (MIDCDFL) and right edge (MIDCDFR) of the middle eye, as a distance from the center of the eye. Calculate the middle eye width (Hmid) as the difference in time between MIDCDFR and MIDCDFL with a value of 10-6. Calculate the time center of the middle eye width (TCmid) as the mid-point in time between MIDCDFR and MIDCDFL with a value of 10-6. MIDCDFL and MIDCDFR are calculated as the cumulative sum of histograms of the zero crossing samples at the left and right edges of the middle eye normalized by the total number of sampled 2 symbols. The MIDCDFL and MIDCDFR are equivalent to bath tub curves where the BER plotted versus sampling time.

4) Locate the center of the middle eye at TCmid.

5) Use the equalized signal from step 2) to construct the CDF of the optical signal for middle eye within 0.025 UI of time TCmid, for both +1/3 (MIDCDF1) and -1/3 (MIDCDF0), as a distance from the center of the eye. Calculate the eye height (Smid) as the difference in voltage between MIDCDF1 and MIDCDF0 with a value of 10-6. MIDCDF0 and MIDCDF1 are calculated as the cumulative sum of histograms of the optical signal at the top and bottom of the eye normalized by the total number of sampled bits.

6) Using the method in step 5), construct CDFs of optical signal of the upper eye at time TCmid, and calculate the 10-6 upper eye height (Sup). Calculate the optical signal (Sup) for upper eye as the mid-point in optical signal between UPPCDFR and UPPCDFL with a value of 10-6.

7) Using the method in step 5), construct CDFs of optical signal of the lower eye at time TCmid, and calculate the 10-6 lower eye height (Slow). Calculate the optical signal for center (Slow) of the lower eye as the mid-point in voltage between LOWCDFR and LOWCDFL with a value of 10-6.

8) Using the method in step 3), calculate the 10-6 upper eye width (Hup) sliced at Sup.

9) Using the method in step 3), calculate the 10-6 lower eye width (Hlow) sliced at Slow.

10) Check the upper and lower eye alignment to the middle eye. Apply an *ESMW* wide mask centered on TCmid, as illustrated by Figure 2. The 10-6 horizontal openings of the upper eye at Sup, and of the lower eye at Slow must all extend beyond this mask.

# STDP Calculation

- **STDP calculated from the scope measurement at TP3 by measuring:**
  - Equalized optical eye opening Sup, Smid, and are either directly measured on the scope with a 7 taps software FFE or the signal passes through a hardware 7 taps FFE

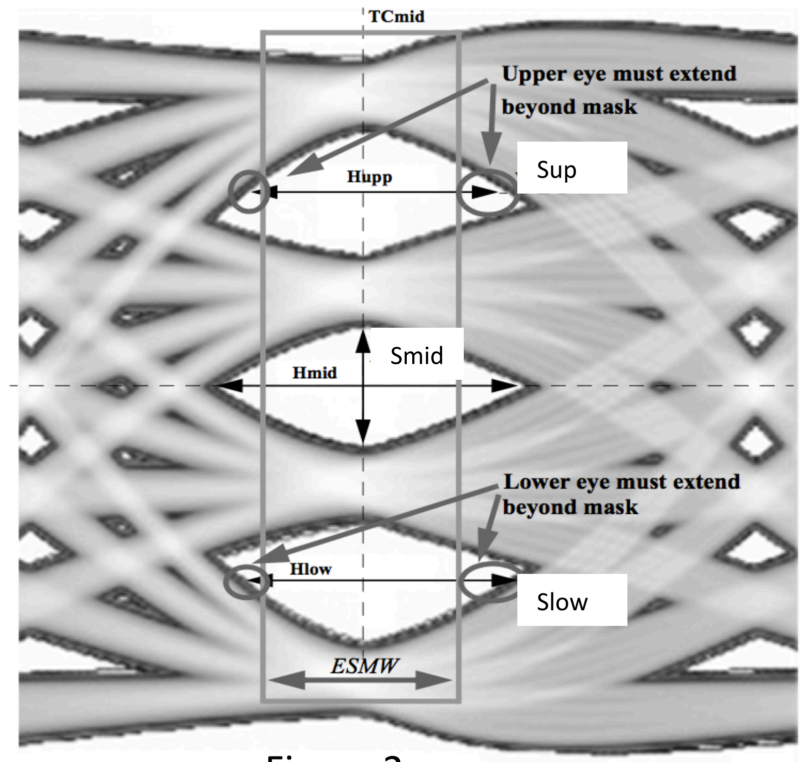
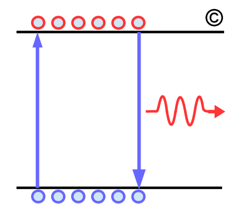



Figure 2

$$STDP = \max\left(10\times\log_{10}\left(\frac{OMAlow}{Slow}\right), 10\times\log_{10}\left(\frac{OMAmid}{Smid}\right), 10\times\log_{10}\left(\frac{OMAhigh}{Sup}\right)\right)$$

# CL 95 TDEC Conformance Test Setup



- **For STDP block diagram is similar to Fig 95-3 with exception max fiber reach is included in the test**
  - Each optical lane is tested at the specified transmitter return loss tolerance
  - The combination of the O/E and the oscilloscope used to measure optical waveform has forth order BT filter response with BW of 0.565*Baudrate
  - The cloak recovery (CRU) has a corner frequency of 4 MHz with slope of 20 dB/decade.

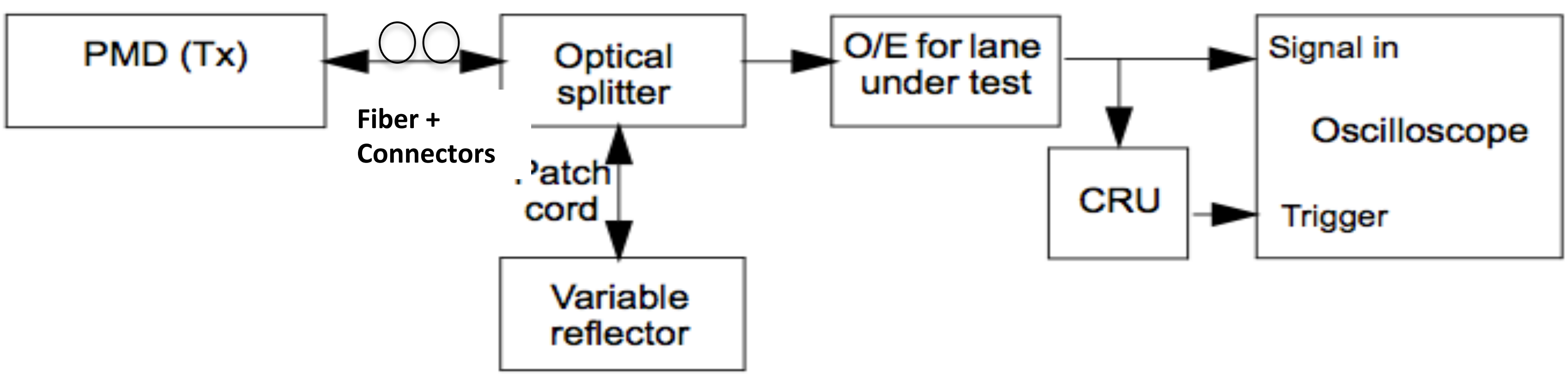



**Figure 95–3—TDEC conformance test block diagram**

# Test Procedure

- **Transmitter compliance**
  - Use STDP to determine if DUT transmitter is compliant at TBD value
  - Test pattern PRBS31Q, SSPRQ is acceptable alternative if the link does not exhibit pattern sensitivity
- **Calibration of the transmitter for stress sensitivity test**
  - Verify transmitter meets TBD STDP and J2/J9 at TBD values
  - Test pattern PRBS31Q, SSPRQ is acceptable alternative if the link does not exhibit pattern sensitivity or by an specific amount (i.e. <0.1 dB)
- **Use the calibrated transmitter to test DUT receiver**
  - Adjust variable reflector and optical power for worst condition
  - Test pattern PRBS31Q, SSPRQ is acceptable alternative if the link does not exhibit pattern sensitivity
  - Measure receiver sensitivity.

# Feedback from Scope Suppliers

- **Supplier I feedback regarding sampling scope**
  - Supports pattern length up to 2^17 bits
  - Supports CTLE, FFE, and DFE
    - CTLE is not adaptive
    - FFE and CTLE will average non-synchronous noises
    - FFE can be T or T/2 spaced
- **Supplier II feedback regarding sampling scope**
  - Supports pattern length up to 2^16 bits
  - Supports CTLE, FFE, and DFE
    - CTLE, FFE, and DFE could be made adaptive
    - Technically can be measured prior to EQ then based on the FFE noise can be shaped prior to display
    - FFE can be T or T/2 spaced
- **Both scope supplier could support PRBS15 or SSPR pattern at expense of test time**
  - The biggest challenge is how to capture non-synchronous noises then accurately included it in the measurement.

# Summary

- The biggest obstacle in defining TDP/TDEC test method is lack of contribution on what is necessary for reference equalizer considering early implementation as well as 2nd generation
  - A fast transmitter based on advance SiP integration having Tr~0.25*Baud period likely can operate with CTLE receiver
  - The standard need to consider broad set of implantations DFB-DML, EA-DFB, and SiP MZM as well as early and 2nd generation implementations

- **The TDP and stress sensitivity methods of CL52, 87, 88 are excellent in identifying potential error floor but the challenge has been lack of available or inconsistent hardware reference receiver**
  - The 400 GbE PMD likely require 5-7 tap HW FFE which no one my ever build!
- **A more viable method is extending TDEC/CDAUI-8 test method using PRBS31Q/SSPRQ measured with a reference software receiver on the scope**
  - To simplify the test method real time scope is assumed
  - If sampling scope evolve such that non-synchronous noise are captured then it is an acceptable alternative
  - The baseline test pattern is PRBS31Q shorter SSPRQ is alternative test pattern if there is no pattern sensitivity
  - Sampling scope could be alternative instrument if the device can capture pre-equalized noise then shape it based on the FFE coefficient then added to the signal
- **This is just a straw proposal where significant amount of work is necessary to verify correlation and compliance!**