Cl **33** *SC* **33.2.7.5** *P* **67** *L* **19** # 1

Bennett, Ken — Sifos Technologies, In

Comment Type **T** *Comment Status* **X** *PSE Power*

There is a recommendation that POWER_UP mode persist for the complete duration of TInrush in section 33.2.7.5 of the existing standard. Commensurately, there is a recommendation against using LEGACY POWER_UP in section 32.2.4.4. This is because legacy power-up can end POWER_UP mode prior to the end of PD Inrush.

The result of an early exit of POWER_UP mode is that current is not limited to the levels in figure 33-13, and inrush current could exceed expected values for a PD, potentially damaging an existing Type 1 or Type 2 PD. Type 3 and Type 4 PSE's could deliver higher currents during PD Inrush in this scenario, increasing the probability of damage to a legacy PD.

The recommendations used in the existing standard have been applied to Type 3 and Type 4 PSE's in the draft. The suggested remedy makes it a requirement for Type 3 and Type 4 PSE's. For reference, the existing text is shown below:

However, for practical implementations, it is recommended that the POWER_UP mode on a pair set persist for the complete duration of TInrush-2P, as the PSE may not be able to correctly ascertain the conclusion of a PD's inrush behavior.

SuggestedRemedy

Change the text to:

However, for practical implementations, it is recommended that POWER_UP mode in Type 1 and Type 2 PSE's persist for the complete duration of TInrush-2P, as the PSE may not be able to correctly ascertain the conclusion of a PD's inrush behavior. Type 3 and Type 4 PSE's shall remain in POWER_UP mode until the Tinrush_2P period in table 33-11 is met.

Proposed Response *Response Status* **W**

Hold open until July.

Yair to present opposition.

Partial OBE by comment # 362.

Cl **33** *SC* **33.2.4.4** *P* **39** *L* **5** # 99

Yseboodt, Lennart — Philips

Comment Type **T** *Comment Status* **X** *PSE Types*

A Type 4 PSE is distinct from a Type 3 PSE in ways other than power (Vpse min, polarity, must implement 4P).
We do not want to prevent Type 4 PSEs from providing also power below class 7.
Currently Table 33-3 requires a Type 4 PSE to have class_num_events = 5, possibly restricting it to Class 7 and 8.

SuggestedRemedy

Add class_num_events 1, 2 and 4 also for Type 4.

Proposed Response *Response Status* **W**

Hold to July for Lennart Presentation.

See Comment # 287.

Cl **33** *SC* **33.3.7** *P* **88** *L* **49** # 271

Dwelley, David — Linear Technology

Comment Type **TR** *Comment Status* **X** *Pres: Table 33-18*

Table 33-18, item 9: Change to "per pair set capacitance" allows 360uF. We changed this to 180uF per Straw Poll 2 in Pittsburgh.

SuggestedRemedy

Change back to "PD capacitance"

Proposed Response *Response Status* **W**

Hold open to July.

Dave Dwelley to present.

Cl **33** *SC* **33.3.7.3** *P* **90** *L* **53** # 334

Darshan, Yair
Microsemi

Comment Type **TR** *Comment Status* **D** *PD Inrush*

We don't want to wait 50- 75msec in Type 3 and 4 systems for Iinrush to be ended if not required due to measuring PD voltage/current/time profile by the PSE and knowing that it was ended earlier.
In some large mutiport systems time for all ports to be ON is affected by Tinrush*N. N number of ports and PSE power supply power capability and its response to dynamic load behavior.

SuggestedRemedy

To add Editor Note at the end of 33.3.7.3.
To address the following issues:
1. Shortening Tinrush if PSE has the knowledge that PD is done with its Inrush.
2. Fastening Tinrush by allowing higher Iinrush_max during Tinrush time frame to shorten Tinrush with big PD capacitors.

Proposed Response *Response Status* **W**

hold open for Yair presentation in July.

This is a brand new topic that has a large techinical impact on the standard. Please give a presentation on such material if you would like it to be included in the standard.

Cl **33** *SC* **33.2.7.5** *P* **67** *L* **36** # 346

Darshan, Yair
Microsemi

Comment Type **TR** *Comment Status* **D** *PSE Power*

It is usefull to allow higher Inrush current than 450mA after TBD time from POWER UP start for the following reasons:
a)Reducing dynamic stress on the MOSFET during POWER UP and
b)Reach faster startup with lower probability for startup oscilations
c) Handle different load behaviour during startup that is time dependent.

SuggestedRemedy

Add the following text after line 36.

The maximum inrush current sourced by the PSE per pair set may exceed the per pair set PSE inrush template in Figure 33–13 only TBD msec after POWER UP has started and shall not excedd ILIM-2P maximum as specified by Table 33-11 item 9.

Proposed Response *Response Status* **W**

Hold open to July.

Yair to present.

Allowing higher current based on time is a brand new topic. Please create a presentation and build consensus for this idea.