

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 33 SC 33.5.1 P 0 L 0 # i-349
 Thompson, Geoffrey Individual

Comment Type ER Comment Status X Management

Cl. 33.5.1, para 1 would seem to be a requirement that applies to cl. 145 devices but I find no clue in 145 to look to cl. 33 for additional requirements.

SuggestedRemedy

Add the requirement to cl. 145 (preferred) or put in some general statement that cl. 145 does not have the complete req'ts for a PSE (and PD?) and you have to read all of cl. 33 to find the rest of them and specify which ones.

Proposed Response Response Status W

TFTD

It is my understanding that we are doing away with all of 33.5. Are we going to do this through maintenance? Or now that the clauses are split, will we just not require this for Type 3 and 4?

TFTD LY

There is no need to remove 33.5 from Clause 33. Our removal of it was undone by the Clause split. We will not define management registers for Clause 145 devices, management of PSEs is possible though Clause 30 objects and the protocols that depend on Clause 30. The rationale not to define this is that the "33.5 style" management has not seen any use in the market.

Cl 1 SC 1.4.254 P 24 L 30 # i-345
 Jones, Chad Cisco Systems, Inc.

Comment Type ER Comment Status D Definitions

Chair notes... before the clause split, we found it necessary to change the definition of link section (and the modifcaiton has evolved). With the clause split, our rationale for the change has disappeared AND I'm not sure it in scope of the PAR (is the definition change required to enable 4P operation or add 10G).

SuggestedRemedy

remove the editorial instructions for 1.4.254

Proposed Response Response Status W

PROPOSED REJECT.

TFTD scope of PAR

I don't think our rationale has disappeared, we still use link section all over the place instead of channel now. Those uses depend on a proper definition.

Cl 1 SC 1.4.313a P 24 L 35 # i-260
 Stewart, Heath Analog Devices Inc.

Comment Type TR Comment Status D Definitions

The existing definition of pairset is PSE centric but is repeatedly referenced by the PD. This definition should be made bi-modal.

Existing definition for pairset:

Either of the two valid 4-conductor connections, Alternative A or Alternative B, as listed in IEEE 802.3, 145.2.4

SuggestedRemedy

Append:

The PSE Alternate A and Alternate B connections are referred to as Mode A and Mode B, respectively, at the PD.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD LY

It needs to be "Alternative" not "Alternate".

Cl 1 SC 1.4.338 P 24 L 39 # i-2
 Anslow, Peter Ciena Corporation

Comment Type E Comment Status D Editorial

IEEE Std 802.3bu-2016 has modified 1.4.338.

SuggestedRemedy

Change the editing instruction to "Change 1.4.338 (as modified by IEEE Std 802.3bu-2016) as follows:"

Change the base text for 1.4.338 to the text as modified by 802.3bu.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD YD

To check this text

TFTD CJ

OBE by 344

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Cl 1 SC 1.4.338 P 24 L 41 # i-344
 Jones, Chad Cisco Systems, Inc.

Comment Type TR Comment Status D Definitions

Chair notes... the definition of PSE needs to include 2.5-10G

SuggestedRemedy

change: intended to provide a single 10BASE-T, 100BASE-TX, or 1000BASE-T device...
 to:
 intended to provide a single 10BASE-T, 100BASE-TX, 1000BASE-T, 2.5GBASE-T,
 5GBASE-T, or 10GBASE-T device...

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by 2

TFTD CJ
 1.4.338 from BU:

1.4.338 Power Sourcing Equipment (PSE): A DTE or midspan device that provides the power to a single link section. PSEs are defined for use with two different types of balanced twisted-pair PHYs. When used with 2 or 4 pair balanced twisted-pair (BASE-T) PHYs, (see IEEE Std 802.3, Clause 33), DTE powering is intended to provide a single 10BASE-T, 100BASE-TX, or 1000BASE-T device with a unified interface for both the data it requires and the power to process these data. When used with single balanced twisted-pair (BASE-T1) PHYs (see IEEE Std 802.3, Clause 104), DTE powering is intended to provide a single 100BASE-T1 or 1000BASE-T1 device with a unified interface for both the data it requires and the power to process these data. A PSE used with balanced single twisted-pair PHYs is also referred to as a PoDL PSE.

Change to:

1.4.338 Power Sourcing Equipment (PSE): A DTE or midspan device that provides the power to a single link section. PSEs are defined for use with two different types of balanced twisted-pair PHYs. When used with 2 or 4 pair balanced twisted-pair (BASE-T) PHYs, (see IEEE Std 802.3, Clause 33 or Clause 145), DTE powering is intended to provide a single 10BASE-T, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, or 10GBASE-T device with a unified interface for both the data it requires and the power to process these data. When used with single balanced twisted-pair (BASE-T1) PHYs (see IEEE Std 802.3, Clause 104), DTE powering is intended to provide a single 100BASE-T1 or 1000BASE-T1 device with a unified interface for both the data it requires and the power to process these data. A PSE used with balanced single twisted-pair PHYs is also referred to as a PoDL PSE.

Cl 25 SC 25.4.5 P 29 L 29 # i-206
 Mcclellan, Brett Marvell Semiconducto

Comment Type ER Comment Status D Editorial

link parameters are specified in 25.4.9 not 25.4.8

SuggestedRemedy

change "25.4.8" to "25.4.9"

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD LY

While the comment seems to be correct, this would be a change to Clause 25 that far outside the scope of our project. It also wasn't an error introduced by our draft, the same possible mistake is present in the base standard. For this a Maintenance Request should be filed.

Cl 30 SC 30.9.1.1 P 35 L 8 # i-350
 Thompson, Geoffrey Individual

Comment Type TR Comment Status X Management

It would appear that all of the strikethrough in this clause is incorrect as it constitutes a change to cl. 33. It is easily possible that the affected text could be improved but it is not proper to remove.

SuggestedRemedy

Restore stricken text in 30.9.1.1. Consider improvements to the text.

Proposed Response Response Status W

TFTD

This is addressed in a bunch of comments from Lennart. Let's revisit and make sure we have satisfied this comment.

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Cl 30 SC 30.9.1.1.1 P 35 L 11 # i-25
 Yseboodt, Lennart Philips Lighting
 Comment Type ER Comment Status D Editorial
 The subclause numbering of aPSEAdminState is wrong. Needs to be 30.9.1.1.2.
 [Note to self: first implement the other Clause 30 comments, this will change all the numbering]
 SuggestedRemedy
 Make aPSEAdminState subclause number 30.9.1.1.2.
 Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 OBE by 3
 TFTD LY
 OBE'ing a comment to itself is not nice. (Comment was marked OBE by 25 in original response).
 TFTD YD
 It is OBE by 3 and not by 25

Cl 30 SC 30.9.1.1.1 P 35 L 21 # i-351
 Thompson, Geoffrey Individual
 Comment Type TR Comment Status D Pres: Yseboodt5
 Reference to control registers in cl. 145 is missing.
 SuggestedRemedy
 Add reference to cl. 145 after the reference to cl. 33.
 Proposed Response Response Status W
 PROPOSED REJECT.
 The reference cannot be added as there are no comment remedies that create a section of clause 145 to point to.
 TFTD

Cl 30 SC 30.9.1.1.4 P 36 L 15 # i-262
 Stewart, Heath Analog Devices Inc.
 Comment Type TR Comment Status X Pres: Darshan5
 It is unclear how the disparate SISM states will be described. For example if the primary is powered and the secondary is searching, what will the returned state value be?
 SuggestedRemedy
 Either remove support for dual-signature PDs or complete their specification throughout the standard.
 Proposed Response Response Status W
 TFTD
 TFTD LY
 The following objects: aPSEPowerDetectionStatus, aPSEPowerClassification, and maybe a few others (30.9.1.1.7, 30.9.1.1.8, 30.9.1.1.11) need to get dual-signature equivalents for each pairset. People who care about dual-signature please to provide baseline at the meeting.
 TFTD YD
 See darshan_05_0917.pdf
 WFP

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CI 30 SC 30.9.1.1.7 P 37 L 25 # i-263
 Stewart, Heath Analog Devices Inc.

Comment Type TR Comment Status X Management

The PSEPowerDeniedCounter is only specified for Type 1 and Type 2 state machine references. It is not clear if this was intention or if references to Type 3 and Type 4 should be added.
 Currently:
 This counter is incremented when the PSE state diagram (Figure 33-9) enters the state POWER_DENIED.

SuggestedRemedy

Option 1 Change
 "(Figure 33-9) enters the state POWER_DENIED"
 to
 "(Figure 33-9, Figure 145-13, Figure 145-15, or Figure 145-16) enters the state POWER_DENIED, POWER_DENIED_PRI, or POWER_DENIED_SEC"
 Option 2 Change
 "when the PSE"
 to
 "when the Type 1 and Type 2 PSE"

Proposed Response Response Status W

TFTD

I somewhat remember a conversation about not supporting this for Type 3/4, am I remembering correctly?

TFTD LY
 That is for the aPSEInvalidSignatureCounter...

CI 30 SC 30.9.1.1.8 P 37 L 35 # i-33
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status D Management

This object was modified to work with Clause 145, but was not updated after the Clause split.
 "This counter is incremented when the PSE state diagram (Figure 145-13, Figure 145-15, and Figure 145-16) enters the state ERROR_DELAY, ERROR_DELAY_PRI, or ERROR_DELAY_SEC."

SuggestedRemedy

Replace by:
 "For Type 1 and Type 2 PSEs, this counter is incremented when the PSE state diagram in Figure 33-9 enters the state ERROR_DELAY.
 For Type 3 and Type 4 PSEs, this counter is incremented when the PSE state diagram in Figure 145-13, Figure 145-15, and Figure 145-16 enters the state ERROR_DELAY, ERROR_DELAY_PRI, or ERROR_DELAY_SEC."

Proposed Response Response Status W

TFTD

You reference the psisms in this remedy, does that make sense?

TFTD DS

I recall agreeing Clause 145 support would not be integrated into Clause 30. Why are we adding references to Type 3 and 4 operation for only this attribute?

CI 30 SC 30.9.1.1.8 P 37 L 41 # i-264
 Stewart, Heath Analog Devices Inc.

Comment Type E Comment Status X Management

The reference to Figure 33-9 has been accidentally deleted.

SuggestedRemedy

Change "(Figure 145-23, " to "(Figure 33-9, Figure 145-13, "

Proposed Response Response Status W

TFTD

see 33

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Cl 30 SC 30.9.1.1.11 P 38 L 2 # i-265
 Stewart, Heath Analog Devices Inc.

Comment Type TR Comment Status X Management

The PSEMPSAbsentCounter is only specified for Type 1 and Type 2 state machine references. It is not clear if this was intention or if references to Type 3 and Type 4 should be added.
 Currently:
 This counter is incremented when the PSE state diagram (Figure 145-13, Figure 145-15, and Figure 145-16) enters the state ERROR_DELAY, ERROR_DELAY_PRI, or ERROR_DELAY_SEC.

SuggestedRemedy

Option 1 Change
 "transitions directly from the state POWER_ON to the state IDLE due to tmpdo_timer_done being asserted"
 to
 "transitions directly from the state POWER_ON, SEMI_PWR_PRI, SEMI_PWR_SEC, POWER_ON_PRI, or POWER_ON_SEC to the state IDLE due to tmpdo_timer_done, tmpdo_timer_done_pri or tmpdo_timer_done_sec being asserted"
 Option 2 Change
 "when the PSE"
 to
 "when the Type 1 and Type 2 PSE"

Proposed Response Response Status W
 TFTD

Cl 30 SC 30.9.2 P 38 L 19 # i-352
 Thompson, Geoffrey Individual

Comment Type TR Comment Status X Management

Comment is out of the scope of the project.

SuggestedRemedy

Delete this line in the draft

Proposed Response Response Status W
 TFTD

TFTD LY
 The referenced line is an editing instruction to delete subclause 30.9.2. Not sure why this is out of scope: there are no PD managed objects, hence this subclause has no merit.

Cl 30 SC 30.12.2.1.9 P 38 L 53 # i-353
 Thompson, Geoffrey Individual

Comment Type TR Comment Status X Management

Missing a syntax value for "Both"

SuggestedRemedy

Add enumeration for "Both" plus appropriate expansion of the "BEHAVIOUR".

Proposed Response Response Status W
 TFTD

(How) do we handle Type 3/4. I know we created PowerPairsX in clause 79.

Cl 30 SC 30.12.2.1... P 40 L # i-355
 Thompson, Geoffrey Individual

Comment Type E Comment Status X Management

I don't understand why each attribute has a "regular" version and a local LLDP version

SuggestedRemedy

Please explain.

Proposed Response Response Status W
 TFTD

Someone with management expertise, please provide a response.

Cl 30 SC 30.12.2.1.18 P 40 L 18 # i-354
 Thompson, Geoffrey Individual

Comment Type TR Comment Status X Management

There is no enumeration defined for "unknown" or "not supported".

SuggestedRemedy

Define the value -1 as indicating "unknown" or "not supported".

Proposed Response Response Status W
 TFTD

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Cl 30 SC 30.12.2.1.18i P 42 L # i-319
 Law, David Hewlett Packard Enter

Comment Type TR Comment Status X Pres: Yseboodt4

The aLldpXdot3LocPowerClassxA, aLldpXdot3LocPowerClassxB, aLldpXdot3RemPowerClassxA and aLldpXdot3RemPowerClassxB attributes don't seem to map to any of the TLV fields defined in subclause 79.3.2 or its subclauses.

SuggestedRemedy

Suggest that:

[1] Delete attributes aLldpXdot3LocPowerClassxA (subclause 30.12.2.1.18i , page 42, line 22), aLldpXdot3LocPowerClassxB (subclause 30.12.2.1.18j, page 42, line 33), aLldpXdot3RemPowerClassxA (subclause 30.12.3.1.18g, page 51, line 29) and aLldpXdot3RemPowerClassxB (subclause 30.12.3.1.18h, page 51, line 41).

[2] Remove entries for aLldpXdot3LocPowerClassxA, aLldpXdot3LocPowerClassxB, aLldpXdot3RemPowerClassxA and aLldpXdot3RemPowerClassxB from Table 30-7 'LLDP capabilities' (page 32, line 38).

Proposed Response Response Status W

TFTD

I assume these were added for DS...

TFTD LY

Should be addressed by yseboodt 04

Cl 30 SC 30.12.2.1.18k P 42 L 3 # i-322
 Law, David Hewlett Packard Enter

Comment Type TR Comment Status X Management

There are no attributes provided in the subclause 30.12.2 'LLDP Local System Group managed object class' or subclause 30.12.3 'LLDP Remote System Group managed object class' for the TLV fields 'Dual-signature power Classx Mode A' and 'Dual-signature power Classx Mode B'.

SuggestedRemedy

Suggest that:

[1] The following new attributes are added in the LLDP local (aLldpXdot3LocDualSigPowerClassxModeA and aLldpXdot3LocDualSigPowerClassxModeB) and remote (aLldpXdot3RemDualSigPowerClassxModeA and aLldpXdot3RemDualSigPowerClassxModeB) managed object class to support the TLV fields 'Dual-signature power Classx Mode A' and 'Dual-signature power Classx Mode B'.

aLldpXdot3LocDualSigPowerClassxModeA

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

singleSignature Single-signature PD

class5 Class 5

class4 Class 4

class3 Class 3

class2 Class 2

class1 Class 1

BEHAVIOUR DEFINED AS:

If the local system is a PD, a read-only value that indicates if it is a single-signature PD, or for a dual-signature PD, the requested Class for Mode A during Physical Layer Classification (see 145.3.6). If the local system is a PSE, a read-only value that indicates if it has detected a single-signature PD, or if it has detected a dual-signature PD, the assigned Class for Alternative A (see 145.2.7).

aLldpXdot3LocDualSigPowerClassxModeB

ATTRIBUTE

APPROPRIATE SYNTAX:

The same as used for aLldpXdot3LocDualSigPowerClassxModeA.

BEHAVIOUR DEFINED AS:

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If the local system is a PD, a read-only value that indicates if it is a single-signature PD, or for a dual-signature PD, the requested Class for Mode B during Physical Layer Classification (see 145.3.6). If the local system is a PSE, a read-only value that indicates if it has detected a single-signature PD, or if it has detected a dual-signature PD, the assigned Class for Alternative B (see 145.2.7).

aLldpXdot3RemDualSigPowerClassxModeA

ATTRIBUTE

APPROPRIATE SYNTAX:

The same as used for aLldpXdot3LocDualSigPowerClassxModeA.

BEHAVIOUR DEFINED AS:

If the remote system is a PD, a read-only value that indicates if it is a single-signature PD, or if it is a dual-signature PD, its requested Class for Mode A during Physical Layer Classification (see 145.3.6). If the remote system is a PSE, a read-only value that indicates if it has detected a single-signature PD, or if it has detected a dual-signature PD, its assigned Class for Alternative A (see 145.2.7).

aLldpXdot3RemDualSigPowerClassxModeB

ATTRIBUTE

APPROPRIATE SYNTAX:

The same as used for aLldpXdot3LocDualSigPowerClassxModeA.

BEHAVIOUR DEFINED AS:

If the remote system is a PD, a read-only value that indicates if it is a single-signature PD, or if it is a dual-signature PD, its requested Class for Mode B during Physical Layer Classification (see 145.3.6). If the remote system is a PSE, a read-only value that indicates if it has detected a single-signature PD, or if it has detected a dual-signature PD, its assigned Class for Alternative B (see 145.2.7).

[2] Mappings for two of the new attributes are added in Table 79-9 'IEEE 802.3 Organizationally Specific TLV/LLDP Local System Group managed object class cross references'. Suggest that the following two new entries are inserted between the row 'PSE power pairx' 'aLldpXdot3LocPowerPairsx' and the row 'Power classx' 'aLldpXdot3LocPowerClassx'.

'Dual-signature power Classx Mode A' 'aLldpXdot3LocDualSigPowerClassxModeA'
'Dual-signature power Classx Mode B' 'aLldpXdot3LocDualSigPowerClassxModeB'

[3] Mappings for two of the new attributes are added in Table 79-10 'IEEE 802.3 Organizationally Specific TLV/LLDP Remote System Group managed object class cross references'. Suggest that the following two new entries are inserted between the row 'PSE

power pairx' 'aLldpXdot3RemPowerPairsx' and the row 'Power classx' 'aLldpXdot3RemPowerClassx' in both tables.

'Dual-signature power Classx Mode A' 'aLldpXdot3RemDualSigPowerClassxModeA'
'Dual-signature power Classx Mode B' 'aLldpXdot3RemDualSigPowerClassxModeB'

Proposed Response *Response Status* **W**
TFTD

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CI 30 SC 30.12.2.1.18i P 43 L 6 # i-320
 Law, David Hewlett Packard Enter

Comment Type TR Comment Status X Management

The behaviour defined for the attributes aLldpXdot3LocPowerTypex and aLldpXdot3RemPowerTypex doesn't see to match the 'Power typex' TLV field that these attributes map to (see Table 79-9 and 79-10). Specifically, the behaviour doesn't include any reference to the single-signature and dual-signature values that Table 79-6d 'System setup field' defines for the 'Power typex' field. Rather than try to further expand the behaviour text to decode bits it would seem a better approach, since these are new attributes being added by IEEE P802.3bt, to change their syntax from 'BIT STRING [SIZE (4)]' to 'ENUMERATED value list'.

SuggestedRemedy

Suggest that:

[1] The 'APPROPRIATE SYNTAX:' text for the attributes aLldpXdot3LocPowerTypex and aLldpXdot3RemPowerTypex should be changed to read:

An ENUMERATED value list that has the following entries:

- type4dualPD Type 4 dual-signature PD
- type4singlePD Type 4 single-signature PD
- type3dualPD Type 3 dual-signature PD
- type3singlePD Type 3 single-signature PD
- type2PD Type 2 PD
- type1PD Type 1 PD
- type4PSE Type 4 PSE
- type3PSE Type 3 PSE
- type2PSE Type 2 PSE
- type1PSE Type 1 PSE

[2] The 'BEHAVIOUR DEFINED AS:' text for the attribute aLldpXdot3LocPowerTypex should be changed to read:

A read-only attribute that returns a value to indicate if the local system is a Type 1, Type 2, Type 3, or Type 4 PSE or PD, and in the case of a Type 3 or Type 4 PD, if it is single-signature or dual-signature.;

[3] The 'BEHAVIOUR DEFINED AS:' text for the attribute aLldpXdot3RemPowerTypex (subclause 30.12.3.1.18j, page 52, line 16) should be changed to read:

A read-only attribute that returns a value to indicate if the remote system is a Type 1, Type 2, Type 3, or Type 4 PSE or PD, and in the case of a Type 3 or Type 4 PD, if it is a single-signature or dual-signature.;

Proposed Response Response Status W

TFTD

CI 30 SC 30.12.3.1.18e P 51 L 17 # i-356
 Thompson, Geoffrey Individual

Comment Type TR Comment Status D Management

"Value"? What value?

SuggestedRemedy

Fully expand the term "value" to "value in units of term, see: 33.n or 145.n."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

TFTD

CI 30 SC 30.12.3.1.18f P 51 L 20 # i-357
 Thompson, Geoffrey Individual

Comment Type TR Comment Status X Management

I have no idea of what a "load configuration" is, much less how it can be described by a BOOLEAN.

SuggestedRemedy

Expand BEHAVIOUR description so what it references is clear and fully explain (repair?) the syntax.

Proposed Response Response Status W

TFTD

CI 30 SC 30.12.3.1.18j P 52 L 20 # i-359
 Thompson, Geoffrey Individual

Comment Type E Comment Status X Management

Requires a slightly different software module to do interpretation for PSE vs. PD for no good reason.

SuggestedRemedy

Make syntax the same for PSE and PD.

Proposed Response Response Status W

TFTD

I don't understand the comment? The syntax is the same, right?

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Cl 33 SC 33.2.1 P 61 L 25 # i-36
 Yseboodt, Lennart Philips Lighting

Comment Type ER Comment Status D Editorial

TOPIC: and/or
 The Chicago Manual of Style says the following about the use of 'and/or':
 "Avoid this Janus-faced term. It can often be replaced by 'and' or 'or' with no loss in meaning.
 Where it seems needed, try 'or ... or both'. But also think of other possibilities."

"PSEs can be compatible with 10BASE-T, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, and/or 10GBASE-T."

SuggestedRemedy

"PSEs can be compatible with 10BASE-T, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, or 10GBASE-T."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

"PSEs can be compatible with 10BASE-T, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, 10GBASE-T, or any combination there of."

TFTD LY

"PSEs can be compatible with any combination of 10BASE-T, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, or 10GBASE-T."

TFTD HS

thereof is one word

Response DNA: I learned that after I gave Chad my responses...who knew? You did.

Cl 33 SC 33.3.1 P 62 L 8 # i-258
 Lukacs, Miklos Silicon Laboratories

Comment Type G Comment Status D General

This is confusing because Clause 145 is also part of THIS standard. Type 1 and Type 2 qualifiers should be added.

SuggestedRemedy

PDs that implement only Mode A or Mode B are specifically not allowed by this standard for Type 1 and Type 2 PDs. PDs that simultaneously require power from both Mode A and Mode B are specifically not allowed by this standard for Type 1 and Type 2 PDs.

Proposed Response Response Status W

PROPOSED REJECT.

We have introduced the following sentence at the beginning of the Clause 33 to point out this exact thing...

References to PSEs and PDs without a Type qualifier refer to Type 1 and Type 2 devices.

TFTD HS

I agree with Miklos. We could easily substitute the word "clause"

PDs that implement only Mode A or Mode B are specifically not allowed by this clause for Type 1 and Type 2 PDs. PDs that simultaneously require power from both Mode A and Mode B are specifically not allowed by this clause for Type 1 and Type 2 PDs.

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Cl 33 SC 33.4.6 P 64 L 34 # i-227
 Mcclellan, Brett Marvell Semiconducto

Comment Type TR Comment Status D AES

E_d_out is a time domain peak to peak voltage but the formula defines E_d_out as varying across frequency. E_d_out isn't measured at individual frequencies.

SuggestedRemedy

delete formula (33-17a) and the text defining f and fmax
 change text on line 31 from:
 "shall not exceed the requirements Equation (33-17a)" (note the missing 'of')
 to "shall not exceed 10 mV peak-to-peak when measured in the band from 1 MHz to 10 MHz and shall not exceed 1mV peak-to-peak when measured in the band from 10 MHz to 100 MHz for 2.5GBASE-T, 10 MHz to 250 MHz for 5GBASE-T, and 10 MHz to 500 MHz for 10GBASE-T"

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD GZ

Reason: i-219 is already TFTD and these are the same comment/issue. We are double checking on the level and test method as to whether we can just do an accept on both of these.

Cl 33 SC 33.4.9.1.1 P 65 L 33 # i-208
 Mcclellan, Brett Marvell Semiconducto

Comment Type TR Comment Status D AES

NEXT loss in 33-18 for PSE midspan is 40dB at 100MHz, however 2.5/5GBASE-T budgets 43dB for connectors. 2.5G and higher needs a separate equation.

SuggestedRemedy

line 25 change "2.5GBASE-T" to "1000BASE-T"
 line 27 delete "For 5GBASE-T, NEXT loss for Midspan PSE devices shall meet the values determined by Equation (145-32) when measured for the transmit and receive pairs from 1 MHz to 250 MHz."
 line 29 change "5GBASE-T" to "1000BASE-T"
 line 39 insert new paragraph "For 5GBASE-T, NEXT loss for Midspan PSE devices shall meet the values determined by Equation (33-18aa) when measured for the transmit and receive pairs from 1 MHz to 100 MHz. For 5GBASE-T, NEXT loss for Midspan PSE devices shall meet the values determined by Equation (33-18aa) when measured for the transmit and receive pairs from 1 MHz to 250 MHz. For operation with 2.5GBASE-T and 5GBASE-T, for frequencies that correspond to calculated values greater than 65 dB, the requirement reverts to the minimum requirement of 65 dB."
 insert a new equation,(33-18aa), copied from (33-18) with accompanied 'NEXTconn' and 'f' definitions, except that "40" is changed to "43"

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

TFTD GZ

Still need to fix equation number on line 27 delete???

Line 25 change "2.5GBASE-T" to "1000BASE-T"
 line 27 delete "For 5GBASE-T, NEXT loss for Midspan PSE devices shall meet the values determined by Equation (145-32) when measured for the transmit and receive pairs from 1 MHz to 250 MHz."
 line 29 change "5GBASE-T" to "1000BASE-T"
 line 39 insert new paragraph "For 2.5GBASE-T, NEXT loss for Midspan PSE devices shall meet the values determined by Equation (33-18aa) when measured for the transmit and receive pairs from 1 MHz to 100 MHz. For 5GBASE-T, NEXT loss for Midspan PSE devices shall meet the values determined by Equation (33-18aa) when measured for the transmit and receive pairs from 1 MHz to 250 MHz. For operation with 2.5GBASE-T and 5GBASE-T, for frequencies that correspond to calculated values greater than 65 dB, the requirement reverts to the minimum requirement of 65 dB."
 insert a new equation,(33-18aa), copied from (33-18) with accompanied 'NEXTconn' and 'f' definitions, except that "40" is changed to "43"

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 33 SC 33.4.9.1.2 P 66 L 10 # i-238
 Zimmerman, George Aquantia, ADI, Comm

Comment Type TR Comment Status D AES

Missing requirement for 10GBASE-T in clause 33 (this one is OK in clause 145, just missed in clause 33)

SuggestedRemedy

Insert new equation 33-19a identical to 33-19 except 0.040 is changed to 0.020. Add text "For 10GBASE-T capable midspans, insertion loss for Midspan PSE devices shall meet the values determined by Equation (33-19) when measured for the transmit and receive pairs from 1 MHz to 500 MHz."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by 209

TFTD YD
 Need to check

Cl 33 SC 33.4.9.1.2 P 66 L 10 # i-209
 McClellan, Brett Marvell Semiconducto

Comment Type TR Comment Status D AES

missing a requirement for 10GBASE-T

SuggestedRemedy

insert new equation 33-19 identical to 33-19 except 0.040 is changed to 0.020. Add text " For 10GBASE-T capable midspans, insertion loss for Midspan PSE devices shall meet the values determined by Equation (33-19) when measured for the transmit and receive pairs from 1 MHz to 500 MHz."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

TFTD GZ

insert new equation 33-19a identical to 33-19 except 0.040 is changed to 0.020. Add text " For 10GBASE-T capable midspans, insertion loss for Midspan PSE devices shall meet the values determined by Equation (33-19a) when measured for the transmit and receive pairs from 1 MHz to 500 MHz."

TFTD YD

Too tight. Channel has sufficient margin. No need to tighten Midspan connector.

Cl 33 SC 33.4.9.1.3 P 66 L 35 # i-210
 McClellan, Brett Marvell Semiconducto

Comment Type TR Comment Status D AES

The return loss limit at 20MHz violates the RL spec in 126.7.2.3 for 2.5G and 5G (17dB).

SuggestedRemedy

create a separate table entry for 2.5GBASE-T with the following limits based on Cat5E:
 1 MHz<f<=31.5 MHz 30 dB
 31.5 MHz<f<=100 MHz 20-20log10(f/100)

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD GZ

Reason: These are the same issue as i-210/i-239 except for 5GBASE-T instead of 2.5GBASE-T. We expect the resolution here will be to adopt the equation of i-239 for 5GBASE-T (Using Cat5e connector requirements frequency extended for a 5G midspan rather than Cat 6), but use the separate-entry structure in the i-211 comment, so the resolution is a bit of a mixture.

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 33 SC 33.4.9.1.3 P 66 L 35 # i-239
 Zimmerman, George Aquantia, ADI, Comm

Comment Type T Comment Status D AES

Return loss on PSE midspan for 2.5G/5GBASE-T should be based on Cat 5e not on clause 40 requirements predating cat 5e. line 35 return loss limit at 20MHz violates the RL spec in 126.7.2.3 for 2.5G and 5G (17dB). Make consistent with Cat 5e connector return loss specifications

SuggestedRemedy

Delete "or 2.5G/5GBASE-T" from 2nd row of 1st column of Table 33-20.
 Insert new row "2.5G/5GBASE-T" between 10/100/1000BASE-T row and 5GBASE-T row, with frequency ranges of:
 1<f<= 31.5 MHz at a return loss value of 30 dB, and
 31.5 MHz<f<=100MHz at a return loss value of 20 - 20log10(f/100) dB
 Change 5GBASE-T row return loss value (100 MHz<= f<= 250 MHz) from 14 dB to 20 dB

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by 210

TFTD GZ
 Reason: These are the same issue as i-210/i-239 except for 5GBASE-T instead of 2.5GBASE-T. We expect the resolution here will be to adopt the equation of i-239 for 5GBASE-T (Using Cat5e connector requirements frequency extended for a 5G midspan rather than Cat 6), but use the separate-entry structure in the i-211 comment, so the resolution is a bit of a mixture.

Cl 33 SC 33.4.9.1.3 P 66 L 37 # i-211
 McClellan, Brett Marvell Semiconducto

Comment Type TR Comment Status X AES

at 100MHz the limit of 14dB is only 4dB margin vs the 2.5/5G spec

SuggestedRemedy

create a separate table entry for 5GBASE-T with the following limits based on Cat6:
 1 MHz<f<=50 MHz 30 dB
 50 MHz<f<=250 MHz 24-20log10(f/100)

Proposed Response Response Status W

TFTD

George, why didn't you comment on this (You and Brett agreed on all the others)?

TFTD GZ

Reason: These are the same issue as i-210/i-239 except for 5GBASE-T instead of 2.5GBASE-T. We expect the resolution here will be to adopt the equation of i-239 for 5GBASE-T (Using Cat5e connector requirements frequency extended for a 5G midspan rather than Cat 6), but use the separate-entry structure in the i-211 comment, so the resolution is a bit of a mixture.

TFTD YD

Go with CAT5E spec to have some margins to MIDSPAN. Not see a reason why to tighten the spec and give the link section the margin. From "channel/link section point of view" it should be OK. Base on 10G experience.
 Same for i-222.

Cl 79 SC 79 P 73 L 1 # i-38
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status X Pres: Yseboodt4

Dual-signature LLDP is incompletely and incorrectly defined.

SuggestedRemedy

Adopt yseboodt_04_0917_LLDP.pdf

Proposed Response Response Status W

TFTD

WFP

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 79 **SC 79.3** **P 73** **L 36** # **i-215**
 McClellan, Brett Marvell Semiconducto
Comment Type ER **Comment Status D** **LLDP**
 can't have a TBD.
SuggestedRemedy
 Change TBD on line 36 to "8"
 Change TBD on line 37 to "9"
Proposed Response **Response Status W**
 PROPOSED ACCEPT.

TFTD LY
 The TBD was put there at the request of Mr. Law to prevent premature software implementations. To check if we are at the stage where we get a subtype assigned and make sure it is aligned with other projects in 802.3.

Cl 79 **SC 79.3.2.1** **P 75** **L 13** # **i-217**
 McClellan, Brett Marvell Semiconducto
Comment Type ER **Comment Status D** **Editorial**
 Note 2 was deleted, but "Note 3" was not renumbered.
SuggestedRemedy
 change "Note 2" to "Note 3" on lines 13 and 23
Proposed Response **Response Status W**
 PROPOSED ACCEPT IN PRINCIPLE.

 change "Note 2" to "Note 3" on lines 13 and 23 on page 75 (comment originally quoted page 15).

TFTD LY
 The comment got it backwards: NOTE 3 needs to become NOTE 2. Check with Pete Anslow what the editorially correct thing to do is and implement that.

TFTD DS
 Comment i-324 (proposed accept) deletes, among other things, the referenced note. If we decide to keep this note, modify proposed remedy to change "Note 3" to "Note 2" and not the other way around.

Cl 79 **SC 79.3.2** **P 81** **L 33** # **i-395**
 Darshan, Yair
Comment Type T **Comment Status X** **Pres: Yseboodt4**
 The 4PID bit need to move to legacy TLV field in order to support legacy PDs.
 This will resolve also comment #130 from D2.4.
SuggestedRemedy
 In Table 79-6d PD 4PID bit: Move this bit to Table 79-4 to bit 3:2 instead of the reserve bits. Make the PD 4PID bit as the reserved bits.
Proposed Response **Response Status W**
TFTD

 Can we add to the legacy fields? I thought a Type 1/2 PD can use the fields of the new TLVs as long as some fields were 0.

TFTD LY
 OBE to yseboodt 04

TFTD YD
 See yseboodt_04_0917.pdf for LLDP adhoc proposed baseline

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Cl 79 SC 79.3.2.6f P 82 L 21 # i-460

Darshan, Yair

Comment Type T Comment Status X Pres: Yseboodt7

Table 79-6f describes autotclass field. Per the draft, autotclass can be requested any time including after the physical layer autotclass after transitioning to POWER_ON.

The are some issues that appear to be not closed.

In the case PD is and PSE supporting LLDP: Why PD will ask for autotclass through LLDP if he can do similar task by LLDP? I am asking this question since if PD eventually do this, it add a level of complexity (that can be resolved) that yet is not addressed in the standard. for example:

- a) There is no syncing or handshake mechanism defined to verify that the PD won't start to consume more power than the PSE allows it to draw, before the PSE is ready for it
- b) It is also not covered in the state machine diagram at page 131 line 43, when moving from IDLE_ACS to MEASURE_ACS.

To resolve this, we need at least to add new variable "dll_autotclass_pd_pse_ready". This variable will indicate that PD has set it's requested power level for the PSE to be measure and the PSE has the available power to measure the PD requested power without going to overload/Ilim 2p condition.

SuggestedRemedy

1. add new variable "dll_autotclass_pd_pse_ready" to the variable list in 145.2.5.4 with the following definition:

"dll_autotclass_pd_pse_ready

This variable indicates that PD has set it's requested power level for the PSE to be measure and the PSE has the available power in order to stay powered and to measure the PD requested power without going to overload/Ilim 2p condition."

2. In the state machine in page 131 line 43 in the exit from IDLE_ACS to MEASURE_ACS, change from:

"MirroredPDAutotclassRequest"

To: "MirroredPDAutotclassRequest*dll_autotclass_pd_pse_ready"

Proposed Response Response Status W

TFTD

I thought Lennart added (or was planning to add LLDP support for Autotclass)...

TFTD DS

WFP yseboodt_07_0917_pdautotclassfix.pdf

Cl 79 SC 79.3.8 P 83 L 36 # i-218

Mcclellan, Brett

Marvell Semiconducto

Comment Type TR Comment Status D LLDP

"subtype=2" is NOT defined for Power Via MDI Measurements
The subtype for Power Via MDI Measurements was left TBD (see other comment)

SuggestedRemedy

change "subtype=2" to "subtype=8"

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD LY

Based on the outcome of i-215 this needs to become subtype=TBD or subtype=<number>. Wait for i-215.

Cl 145 SC 145.1 P 95 L 7 # i-364

Thompson, Geoffrey

Individual

Comment Type ER Comment Status X Pres: Thompson??

There is no clear statement of the top level model of a PoE system in clause 145.1. such a statement is essential for someone reading the standard for the first time in order for the reader to figure out how to structure his thinking and to parse the problem.

SuggestedRemedy

See proposed text in submitted file GOT - Proposed text.txt. Pick existing text back up at the start of the list at line 27.

Proposed Response Response Status W

TFTD

WFP

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.1 P 95 L 9 # i-43
 Yseboodt, Lennart Philips Lighting

Comment Type E Comment Status X Editorial

"This clause defines the functional and electrical characteristics for providing an enhancement of the Power over Ethernet (PoE) system defined in Clause 33 for deployment over balanced twisted-pair cabling."

Makes it seem that Clause 145 is an 'add-on' to Clause 33. It isn't, it is a complete, standalone PoE Clause.

SuggestedRemedy

"This clause defines the functional and electrical characteristics of an enhanced Power over Ethernet (PoE) system originally defined in Clause 33 for deployment over balanced twisted-pair cabling."

Proposed Response Response Status W

TFTD

This new text makes it seem that an "enhanced PoE system" was defined in Clause 33.

TFTD LY

True... Maybe split up: "This clause defines the functional and electrical characteristics of an enhanced Power over Ethernet (PoE) system for deployment over balanced twisted-pair cabling. The original PoE system is defined in Clause 33".

TFTD CJ

Surprised you just didn't suggest this as the remedy: "This clause defines the functional and electrical characteristics of a Power over Ethernet (PoE) system originally defined in Clause 33 for deployment over balanced twisted-pair cabling."

Cl 145 SC 145.1 P 95 L 21 # i-365
 Thompson, Geoffrey Individual

Comment Type ER Comment Status X Editorial

Clause 1.4 is the definitions clause for the entire standard. If this line is necessary it would appear in each clause.

SuggestedRemedy

Delete line 21

Proposed Response Response Status W

TFTD

We added this line specifically because most of the readers we deal with don't know that 1.4 has the definitions.

Cl 145 SC 145.1 P 95 L 25 # i-366
 Thompson, Geoffrey Individual

Comment Type ER Comment Status D Editorial

The phrase "with a single interface to both the data it requires and the power to process this data" implies that the power provided is adequate to do data processing on 10GBASE-T. The TF has done no investigation to establish whether such is the case or is factual. Further, there are broader valid uses for PoE than is implied in the text.

SuggestedRemedy

Change text to read: "...with a single cabling interface for both the data and power."

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD CJ

proposed reject.

1.I recall Mr. Thompson being intimately involved in crafting this language to AF. Change of heart on having this informative text about THE INTENT of PoE?

2.I have personally seen 10G systems that work under AT power, let alone the 71.3W we will provide a PD for BT. Conversely, I can devise many systems that could have only a 10Mb link but need more than 13W, 25.5W or even 90W. Neither of those facts change the fact that PoE is INTENDED to provide a single connection for power and data – for products that can squeeze their power consumption under the limits set forth in the standard.

3.The remedy simply adds 'cabling' to the sentence. This does nothing to resolve the so-called issues laid out in the comment. I disagree that 'cabling' needs added to the sentence and the comment made zero case for this inclusion.

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.1e P 95 L 32 # i-367
 Thompson, Geoffrey Individual

Comment Type ER Comment Status D Editorial

The PSE and PD are mentioned in the plural. The "method" referred to is only between one PSE and PD. Dynamic negotiation between PSEs, while possible, is outside the scope of this standard.

SuggestedRemedy

Change text to read: "A method for a PSE and the PD to which it is paired to dynamically negotiate and allocate power"

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Change text to read: "A method for a PSE and the PD to which it is paired to dynamically negotiate and allocate power"

Also, change item d) to "Methods to classify a PD based on its power needs.

TFTD LY

Change "paired" to "connected".

Cl 145 SC 145.2 P 97 L 1 # i-369
 Thompson, Geoffrey Individual

Comment Type ER Comment Status X PI

This paragraph is a problem. Regarding the first sentence, I don't believe we specify, or should specify a PSE at the MDI, we specify at the PI. After all, that is why we created the PI. Thus, I don't think there are any statements that express PSE specs in terms of the MDI (though I confess I did not search). If there are they should be re-expressed in terms of the PI. Regarding the second sentence, this is a HUGE escape clause which allows ANY mid-span to claim compliance to the standard

SuggestedRemedy

Replace with: "In the case of a Midspan PSE PI, the interface specification point is physically separate from the MDI and is contained within the cabling portion of the data transmission system."

Proposed Response Response Status W

TFTD

Cl 145 SC 145.1.3 P 97 L 21 # i-370
 Thompson, Geoffrey Individual

Comment Type ER Comment Status D Systems

We have proved in TF discussions that there can be multiple PSEs in a valid system but only one of them can be active for there not to be a fault.

SuggestedRemedy

Change wording to read: A valid power system consists only of a single active PSE, a single PD, and the link section connecting them. If needed, we could say: "A valid active power system consists only of a single active PSE, a single PD, and the link section connecting them."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Change wording to read: "A valid power system consists only of a single active PSE, a single PD, and the link section connecting them."

TFTD DS

Per i-382 response, we don't specify a PoE system--we specify components individually so that they interoperate. In this case, "active" is an undefined term; this will lead to interpretations and likely to interoperability issues.

Propose we maintain the existing text and furthermore remove the informative text in 145.2.5.1 beginning with "It is possible that two separate PSEs...may be attached to the same link segment". This removes the implication that Clause 145 provisions for specific system configurations.

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Cl 145 SC 145.1.3 P 97 L 37 # i-44
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status D Systems

Table 145-1, Type 4 entry lists 0.96A as the nominal current and number of powered pairs as "2 or 4".

We only allow >0.6A when in 4-pair mode though (with the exception of dual-signature fault conditions).

SuggestedRemedy

Split Type 4 line in two:

Type 4	0.6	2	12.5	(cable spec)
Type 4	0.96	4	12.5	(cable spec)

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD YD

"I don't think this is correct to do.-Technically it is incorrect.-We are talking about current capability of the wires per type. It cant be that if over 4-pairs we allowed to supply 0.96A over each pairset and over only 2-pair you can only deliver 0.6A. The math is not correct.-The limitations for 0.6A over 2-pair is not technical limitation. It is other (political limitation) and it is sufficiently defined in the spec. To limit it in the table is a mistake."

Cl 145 SC 145.1.3 P 97 L 38 # i-394
 Diminico, Christopher

Comment Type TR Comment Status X Pres: Diminico

For a constant power load and a worse case PSE the current per pair (ICable, A) is dependent on the loop resistance (equation 145-2). The current per pair/conductor is a parameter used to limit the number of 4-pair cables in a cable bundle. The 802.3bt nominal highest current per pair (ICable, A) derived by assuming the worse case DC loop restistance (RCh), associated with 100 meters of cabling, is being used to limit the number of 4-pair cables in a bundle for all cabling lengths (DCR). Assuming the worse case DCR (length) for all cabling topologies leads to overly pessimistic limits on the number of 4-pair cables in a cable bundle.

SuggestedRemedy

Develop informative Annex to characterize the current as a function of DCR (length) for constant power loads and worse case PSEs (equation 145-2). Presentation of proposed Annex to be provided.

Proposed Response Response Status W

TFTD

WFP

Cl 145 SC 145.1.3 P 98 L 2 # i-334
 Abramson, David Texas Instruments Inc

Comment Type E Comment Status D Editorial

Inconsistent language: This clause uses "pairset DC loop resistance"... However, a few lines below (lines 10 and 15) we use "DC pairset loop resistance".

SuggestedRemedy

Editor to change line 2 to "DC pairset loop resistance" and confirm all other uses in claus 145 are aligned.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD LY

I would rather change line 10 to "RCh is the maximum pairset DC loop resistance, as defined ...".

Cl 145 SC 145.1.3 P 98 L 6 # i-372
 Thompson, Geoffrey Individual

Comment Type E Comment Status X

It is a fine point but lport is defined on the basis of the cabling, but a "port" is a feature of equipment, not cabling. Therefore the definition should be "lport is the total current sourced by a PSE or sunk by a PD."

SuggestedRemedy

Change text per comment.

Proposed Response Response Status W

TFTD

While Geoffrey has a point, I think his suggested definition obscures the point we are trying to make (lport is the total current).

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.1.3.1 P 98 L 28 # i-379
 Thompson, Geoffrey Individual

Comment Type ER Comment Status D Editorial

The placement of the cabling specifications in 145.1.3 System Parameters is wrong. Cabling is not a "system parameter". Placement there is organizationally confusing. Cabling is a full element of the the specified 3 element system. The cabling should have its own sub-clause at a peer level with 145.2 PSE and 145.3 PD.

SuggestedRemedy

Move the specification (whether it be by reference or local) for cabling to its own higher level clause, presumably cl. 145.4 which would bump the rest of the clause further out.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Move clause 145.1.3.1 (which now has what used to be 145.1.3.2 in it) to new clause 145.4 and increment all further clauses.

TFTD just to check

TFTD LY

I assume you meant to make it 145.1.4... ?

Response DNA: nope, Geoff wants it as 145.4

Cl 145 SC 145.1.3.1 P 98 L 28 # i-378
 Thompson, Geoffrey Individual

Comment Type ER Comment Status D Editorial

There is no reason for 145.1.3.1 Cabling requirements and 145.3.2 Link section requirements to be separate peer clauses. There is no difference between the two so there is no reason to have separate clauses.

SuggestedRemedy

Consolidate the text of the two sub-clauses into a single clause or consolidate the text into any new form of the specification.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Consolidate the text of the two sub-clauses into a single clause

TFTD DS

Comment references section "145.3.2"; should reference "145.1.3.2".

Cl 145 SC 145.2 P 99 L 1 # i-347
 Jones, Chad Cisco Systems, Inc.

Comment Type TR Comment Status X PSE Power

Chair notes... Confirm that it is not possible that a Type 3, 4 PSE DOES NOT present 4 or 5 event class and only uses L1 to get to >30W. I know this is a bad format comment and breaks all my rules. I ran out of time to research. I will withdraw if I can find the answer after the ballot closes.

SuggestedRemedy

Make the change to prevent a Type 3 or 4 PSE from only using LLDP to get to >30W

Proposed Response Response Status W

TFTD

TFTD LY

Page 148, line 28 says: "A PSE shall be capable of assigning the highest Class it can support by means of Multiple-Event Physical Layer Classification." This should prevent the behavior stated in your comment.

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.1 P 99 L 25 # i-346
 Jones, Chad Cisco Systems, Inc.

Comment Type E Comment Status D PSE Power

Chair notes... We are missing the statement that a PSE does not change Type once it is powering a PD.

SuggestedRemedy

On page 99, line 25, add the sentence:
 Once a PSE is reached POWER_ON, PSE Type does not change.

Proposed Response Response Status W

PROPOSED REJECT.

Type is immutable in Clause 145.

TFTD YD

Response "Type is immutable in Clause 145." is not clear

TFTD DS

While I agree with the editor's sentiment, I cannot find a statement in Clause 145 reinforcing the immutability of PSE Type. Let's add a statement to this effect.

TFTD CJ

'type is immutable'. Where is this statement? I couldn't find it. Reminder: when the comment says Chair notes... this means it came up in conversation in the room and I took the AI to follow up.

A Type 4 pse is free to use system parameters of the PD type if attached to a lower type PD. Is it then free to switch back to Type 4 settings while the PD is powered?

Cl 145 SC 145.2.2 P 99 L 53 # i-47
 Yseboodt, Lennart Philips Lighting

Comment Type ER Comment Status D Editorial

TOPIC: and/or
 The Chicago Manual of Style says the following about the use of 'and/or':
 "Avoid this Janus-faced term. It can often be replaced by 'and' or 'or' with no loss in meaning.
 Where it seems needed, try 'or ... or both'. But also think of other possibilities."

"PSEs can be compatible with 10BASE-T, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, and/or 10GBASE-T."

SuggestedRemedy

"PSEs can be compatible with 10BASE-T, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, or 10GBASE-T."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

"PSEs can be compatible with 10BASE-T, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, 10GBASE-T, or any combination thereof."

TFTD LY

"PSEs can be compatible with any combination of 10BASE-T, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, or 10GBASE-T."

Cl 145 SC 145.1.3.1 P 102 L 30 # i-48
 Yseboodt, Lennart Philips Lighting

Comment Type ER Comment Status D Cabling

"Type 3 and Type 4 operation requires Class D or better cabling as specified in ISO/IEC 11801:2002."

Redundant reference to Type. Also, not completely true, a Type 3 system operating at Class 3 will still work over 20 ohm cable.
 Trying to explain that nuance in this sentence seems unnecessary.

SuggestedRemedy

"Class D or better cabling as specified in ISO/IEC 11801:2002 is required to support operation as specified in this Clause."

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD CJ

the comment says: Also, not completely true, a Type 3 system operating at Class 3 will still work over 20 ohm cable.
 but the suggested remedy makes no effort to fix?

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

CI 145 SC 145.2.4 P 107 L 40 # i-49
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status X Pres: Darshan12

A PD's diode bridge is the dominant, and most unpredicable, contributor to pair-to-pair current unbalance.

Diode specifications generally do not include information or guarantees about the maximum spread in forward voltage between samples.

This makes it hard to get to a provable correct design that will always meet the current unbalance spec.

It is however not impossible, analysis over the course of this project has shown that diode forward voltage differences of more than 60mV are extremely rare. This number has been used to calculate the unbalance budget for the PD.

What isn't taken into account is diode aging. As diodes are exposed to current and temperature, their forward voltage will begin to drift.

A pair of parallel diodes exposed to roughly the same current may be expected to age in the same way (this is uncertain, but let's accept it for the moment).

If 4-pair PSEs are allowed to provide power in polarity configurations that can result in ONE pairset having the other polarity between two PSEs, this would mean that a PD that has been exposed to a certain current configuration, would find itself powered in a way that has one 'aged' diode conduct, and another 'new' diode in parallel. By 'new' I refer to a diode that has not seen any significant current over it's lifetime.

At the moment of writing this comment, it is unknown what the magnitude of this issue is. Test to determine this are planned.

SuggestedRemedy

1. Quantify this issue for the November meeting
2. Appropriate solution, if needed to be presented then

Proposed Response Response Status W

TFTD

TFTD YD

See darshan_12_0917.pdf

WFP

TFTD DS

The PD designer has multiple options to circumvent this issue: Request greater Class, utilize less of P_Class_PD, or take active control of PD contribution to system unbalance. The TF have specified unbalance numbers that compromise between substantial PD unbalance contributions and burden on other system objects to 'ballast' PD contributions. PD designers with marginal designs and high P_Class_PD utilization should be cautioned to consider unbalance effects (perhaps a note in PD unbalance section).

TFTD CJ

Proposed reject. The comment has served its purpose. We reject, he says unsatisfied, it remains in scope for November. Incidentally, I did some measurements of 'used' diodes versus unused and found indistinguishable difference in Vf.

CI 145 SC 145.2.5 P 108 L 6 # i-50
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status X Pres: Yseboodt5

Clause 33 in the base standard, subclause 33.5 says:

"If the PSE is implemented with a management interface described in 22.2.4 or 45.2 (MDIO), then the management access shall use the PSE register definitions shown in 33.5.1. Where no physical embodiment of the Clause 22 or Clause 45 management is supported, equivalent management capability shall be provided. Managed objects corresponding to PSE and PD control parameters and states are described in Clause 30."

Clause 145 will not define these specific registers, as implementors choose to use a different interface than MDIO to configure the PSE.

We should however maintain the requirement that certain basic parameters in the state diagram must be configurable by the implementor of the PSE.

SuggestedRemedy

Adopt yseboodt_05_0917_management.pdf

Proposed Response Response Status W

TFTD

WFP

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.5.3 P 109 L 42 # i-253
 Pekar, Arkadiy Microsemi Corporation

Comment Type TR Comment Status X PSE SD

This comment is an update to the comment that requires to delete Figure 145B-3:
 Per the definition of CC_DET_SEQ=0 for dual-signature, the detection need to be parallel and not staggered and this contradicts figure 145B-3 that is shown as one of the staggered detection versions. So we have two options to resolve this:
 a) To delete figure 145B-3 to sync with CC_DET_SEQ=0 definition for dual-signature PDs and also update state machine which will be complicated task at this point of time. OR,
 b) (Preferred) Keep Figure 145B-3, and change the ""CC_DET_SEQ=0 definition that to allow staggered detection in addition to parallel detection which currently is supported by the state machine."

SuggestedRemedy

Change "Connection Check is followed by staggered detection for a single-signature PD and parallel detection for a dual-signature PD."
 To: Connection Check is followed by staggered detection for a single-signature PD and parallel or staggered detection for a dual-signature PD."

Proposed Response Response Status W

TFTD

These variables do something in the state diagram (control which branches to take), so I don't think we can just change the definition of option "0" unless "0" really has both staggered and parallel. Does it?

TFTD DS

To answer the editor's question: it does. Sequence 0 runs dual-signature staggered/"parallel" using the same variables and logic as Sequence 1. To the commentor, I would ask if we are adding clarity by trying to summarize the entire behavior of each sequence in these descriptions? We've already pointed the reader to Annex 145B, which does a fine job showcasing the intended behavior.

Cl 145 SC 145.2.5.4 P 110 L 27 # i-52
 Yseboodt, Lennart Philips Lighting

Comment Type ER Comment Status D PSE SD

For variable alt_pwr_d_pri, the values are described:
 "FALSE: The PSE is not to apply power to the Primary Alternative.
 TRUE: The PSE has detected, classified, and will power a PD on the Primary Alternative; or power is being forced on the Primary Alternative in TEST_MODE."

Why are we describing half of the state machine for the 'TRUE' value ?

SuggestedRemedy

Replace TRUE by:
 TRUE: The PSE is to apply power to the Primary Alternative.

Same change for _sec.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD YD

It is clearer that way that this is the intent. Verify precedence in other similar variables

TFTD DS

'is to apply power'? When?
 Propose instead, "The PSE is (not) applying power to the Primary Alternative".

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.5.4 P 111 L 36 # i-457
 Darshan, Yair

Comment Type E Comment Status D PSE SD

In the variable description dll_4PID "dll_4PID A variable that indicates whether the PSE and PD have negotiated 2-pair or 4-pair power." it doesn't say with what they were negotiate etc.

SuggestedRemedy

Change from "dll_4PID
 A variable that indicates whether the PSE and PD have negotiated 2-pair or 4-pair power."
 To: "dll_4PID
 A variable that indicates whether the PSE and PD have negotiated 2-pair or 4-pair power capability via the Data Link Layer."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Change to: "dll_4PID
 A variable that indicates whether the PSE and PD have negotiated 2-pair or 4-pair power capability via the Data Link Layer."

Also change the descriptions of values "0" and "1" from "...power negotiated" to "...power capability negotiated"

TFTD DS

It seems more appropriate to directly reference the field, rather than hunt thru TLVs to find what this variable hooks on to.

Change to "dll_4PID: A variable indicating the state of the PD 4PID bit in the System startup field"

Cl 145 SC 145.2.5.4 P 113 L 24 # i-269
 Stewart, Heath Analog Devices Inc.

Comment Type T Comment Status X PSE SD

option_class_probe can be utilized to both reduce dissipated heat during classification and increase classification flexibility.
 See stewart_0917_01.

SuggestedRemedy

Adopt stewart_0917_01.

Proposed Response Response Status W

TFTD

WFP

TFTD YD

See also darshan_04_0917.pdf

Cl 145 SC 145.2.5.4 P 113 L 40 # i-249
 Peker, Arkadiy Microsemi Corporation

Comment Type TR Comment Status X

In the variable option_probe_alt_sec definition:
 "option_probe_alt_sec
 This variable indicates if the PSE will continue to detect and conditionally class on the Secondary Alternative in the event an invalid detect or class result is found on the Primary Alternative. This variable applies to CC_DET_SEQ = 3.

Values:

FALSE: PSE does not probe the Secondary Alternative if an invalid signature is found on the Primary Alternative.

TRUE: PSE does probe the Secondary Alternative if an invalid signature is found on the Primary Alternative." we have few issues:

1) The definition text says "in the event an invalid detect or class result is found" is not reflected in the text that defines the TRUE and FALSE. Only the "invalid detection" is addressed.

2) The text " if an invalid signature is found" in the TRUE and FALSE definition is not logically accurate and can lead to wrong interpretation. It should be " if an invalid signature will be found" since this variable can be set in system config phase or on the fly, but the current definition may be interpreted as this parameter can be configured only on the fly as function of the result of primary detection signature result if valid or not."

SuggestedRemedy

Change the TRUE and FALSE definition from:

"FALSE: PSE does not probe the Secondary Alternative if an invalid signature is found on the Primary Alternative.

TRUE: PSE does probe the Secondary Alternative if an invalid signature is found on the Primary Alternative."

To:

"FALSE: PSE does not probe the Secondary Alternative if an invalid detection signature or classification will be found on the Primary Alternative.

TRUE: PSE does probe the Secondary Alternative if an invalid detection signature or classification will be found on the Primary Alternative"

Proposed Response Response Status W

TFTD to your first point about class. Does the SD show the option of probing alt_sec if class is invalid? Or just detect?

TFTD DS

The original text states 'if an invalid signature is found', where 'invalid signature' may refer to 'detection signature' or 'classification signature'.

To address the editor's question, the SD does allow SEC to probe in the general case that PRI has failed to power on. The agreed intention of probe_alt_sec is that SEC is prohibited from powering on, in this specific case (see page 3, stover_01_0116_rev01.pdf)

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.5.4 P 114 L 32 # i-270
 Stewart, Heath Analog Devices Inc.

Comment Type T Comment Status D PSE SD

Existing definition of pd_4pair_cand is out of sync with 145.2.6.7, which describes 4 possible procedures. The Physical Classification procedure is missing.
 pd_4pair_cand
 This variable is used by the PSE to indicate that a connected PD is a candidate to receive power on both Modes. This variable is a function of the results of Detection, Connection Check, and PD 4PID; see 145.2.6.7.

SuggestedRemedy

Change "Connection Check, " to "Connection Check, Physical Classification, "

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD LY
 Needs to be "Physical Layer Classification"

Cl 145 SC 145.2.5.4 P 114 L 37 # i-60
 Yseboodt, Lennart Philips Lighting

Comment Type E Comment Status D PSE SD

"This variable indicates 4PID and Type 3 or Type 4 dual-signature PD has been established by using the method to generate 3 class events on the Primary Alternative."

The PD has been established ?

SuggestedRemedy

Replace by:
 "This variable indicates that 4PID has been established on the Primary Alternative by using the method to generate 3 class events to determine the PD's Type."

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD DS
 Actually, this method may use 3 or 4 class events to determine 4PID (inexplicably, Class 5 PDs require 4 class events to establish 4PID). Also, I see no reason to redundantly state this in the variable definition.
 Change to: "This variable indicates dual-signature PD Type has been established on the Primary Alternative by Physical Classification."

Cl 145 SC 145.2.5.5 P 119 L 10 # i-271
 Stewart, Heath Analog Devices Inc.

Comment Type E Comment Status D Editorial

There are two differing spelling of t_class_acs vs t_classacs. Note the _ after the t denotes subscript.

SuggestedRemedy

Globally change t_classacs_timer to t_class_acs. Note the _ after the t denotes subscript.
 Page 119, line 10
 Page 128, lines 17 and 21

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD LY

Since it is a state diagram timer, it needs to end with "timer". So, global replace of "tclassacs timer" with "tclass acs timer". The note about subscript doesn't make sense, and indicates that the timer and the timing parameter have been conflated since timers do not use subscript.

TFTD DS

Minor fix to suggested remedy: Globally change "tclassacs_timer" to "tclass_acs_timer"

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.5.6 P 122 L 13 # i-274
 Stewart, Heath Analog Devices Inc.

Comment Type E Comment Status D PSE SD

The do_classification_[pri|sec] function is unique in that it remembers previous calls and builds return variable responses based on the preceding collection of calls.

SuggestedRemedy

Append after "variables for the Primary Alternative."
 Return values are based on all do_classification_pri events until a detection or class reset clears the memory.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

TFTD

I think including this text in the description of pse_allocated_pwr_pri and pd_req_pwr_pri is better. The value of pd_class_sig_pri is not dependent on previous function calls.

Append the following to the end of the pse_allocated_pwr_pri and pd_req_pwr_pri descriptions.

The returned value is based on all previous do_classification_pri function calls since the last time in DETECT_EVAL_PRI or CLASS_RESET_PRI.

Make similar change for _sec.

TFTD LY

Also append: "See Table 145-11 for a correct determination of the PSE assigned Class".

Cl 145 SC 145.2.5.7 P 125 L 1 # i-348
 Jones, Chad Cisco Systems, Inc.

Comment Type TR Comment Status X

Chair notes... PSE State Diagram. I cannot find a path to power up with pse_ss_mode=0. There is the ELSE statement in POWER_ON, where alt_pwrd_pri gets set true and alt_pwrd_sec gets set false. This seems to allow a Type 3 PSE to power up a class 1-4 in 2P mode, (which my Chair note indicated I needed to confirm) but then it implies that there is no path to 4P power for Class 1-4. Will withdraw when I am educated on how to get to each operating point.

SuggestedRemedy

Change figure 145-13 to enable Class 1-4 operation on either 2P or 4P.

Proposed Response Response Status W

TFTD

I believe it is done through the use of pse_ss_mode_update which transitions immediately back to POWER_ON.

TFTD DS

Proposed response addresses variable assignment after POWER_ON; does not address question related to how this variable is initialized.

Add pse_ss_mode assignment logic to IDLE state logic as follows, to indicate to the user how this variable may be initialized:

```
IF (pse_alternative != both) THEN
    pse_ss_mode <= 0
ELSE
    pse_ss_mode <= user defined
END
```

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.5.7 P 125 L 1 # i-66
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status X Pres: Yseboodt6

The PSE state diagram currently requires a PSE to either turn on, or go back to IDLE within Tpon referenced at the end of detection. Another option is to 'renew' Tpon by checking is the PD is drawing a correct mark current. This flexibility has a number of use cases as explained in http://www.ieee802.org/3/bt/public/may17/lukacs_01_0517_Mark&Hold_rev1.0.pdf

SuggestedRemedy

Adopt yseboodt_06_0917_markhold.pdf

Proposed Response Response Status W

TFTD

WFP

TFTD LY

Also see lukacs 01 on reliability testing.

Cl 145 SC 145.2.5.7 P 127 L 33 # i-288
 Stover, David Analog Devices Inc.

Comment Type ER Comment Status D PSE SD

Missing parenthesis in PSE SD (shown in proposed change as a right square bracket; should be inserted as a right parenthesis).

SuggestedRemedy

Change to "(pse_alternative = both) * ((det_temp = only_one) * (sig_pri != valid) + (det_temp = both_neither) * (sig_sec != valid) + (((CC_DET_SEQ = 0) + (CC_DET_SEQ = 3)) * (det_temp = only_one) * tdet2det_timer_done))] + (pse_alternative = a) * (sig_pri != valid) + (pse_alternative = b) * (sig_pri = open_circuit)" replacing right square bracket with right parenthesis.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD, can someone confirm this?

TFTD LY

Nope... that arc contains 15 open parens and 15 closing parens.

TFTD YD

Need to confirm

TFTD DS

Confirmed.

Cl 145 SC 145.2.5.7 P 128 L 6 # i-398
 Darshan, Yair

Comment Type T Comment Status D PSE SD

In CLASSIFICATION state, the assignment pse_allocated_power = 0 is not possible per the pse_allocated_power variable definition that starts from 1 and not from 0.

SuggestedRemedy

Change from: pse_allocated_power <= 0
 To: pse_allocated_power <= 1

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Change from: pse_allocated_pwr <= 0

To: pse_allocated_pwr <= 1

TFTD LY

A better solution is to define what '0' means. Add value 0 to the variable description of pse allocated power, with text "No power is assigned to the PD". That way the value of pse allocated power always reflects the truth, no matter where we are in the state diagram.

TFTD YD

"Instead of the proposed remedy, it will be better to:-add value 0 to pse_allocated_pwr with meaning ""no power allocated"". -also add pse_allocated_pwr = 0 to POWER_DENIED."

TFTD DS

Reject. Pse_allocated_pwr = 0 is used to trigger computation of pse_allocated_pwr in MARK_EV_LAST (must transition thru this state and cannot leave assigned to 0).

Cl 145 SC 145.2.5.7 P 128 L 46 # i-458
 Darshan, Yair

Comment Type T Comment Status X PSE SD

In the exit from CLASS_EV3 MARK_EV3 "tcle3_timer_done * (pse_alternative = both) * (pd_class_sig ? 4) * ((pse_avail_pwr ? pd_class_sig+5) + (pse_avail_pwr > 5))", missing parenthesis in pd_class_sig+5.

SuggestedRemedy

Change from: " tcle3_timer_done * (pse_alternative = both) * (pd_class_sig ? 4) * ((pse_avail_pwr ? pd_class_sig+5) + (pse_avail_pwr > 5))"
 To: "tcle3_timer_done * (pse_alternative = both) * (pd_class_sig ? 4) * ((pse_avail_pwr ? (pd_class_sig+5) + (pse_avail_pwr > 5))"

Proposed Response Response Status W

TFTD

Wait for outcome of 459

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.5.7 P 128 L 46 # i-459

Darshan, Yair

Comment Type T Comment Status X PSE SD

In the exit from CLASS_EV3 MARK_EV3 "tcle3_timer_done * (pse_alternative = both) *(pd_class_sig ? 4) *((pse_avail_pwr ? pd_class_sig+5) +(pse_avail_pwr > 5))", the "+" in pd_class_sig+5 is (according to page 109 line 22) "a Boolean OR" while in the intent here is to be used as mathematical sum. There is a need to either update the '+' definition or add another symbol for mathematical summation.

SuggestedRemedy

1. add '++' symbol to table in page 109 and define this symbol as mathematical summation.
2. Change from "pd_class_sig+5)" to "pd_class_sig++5)"
3. Fix the same problem in P128, l46 in MARK_EV3 state.

Proposed Response Response Status W

TFTD

What is this line supposed to be? It wouldn't make sense for ((pse_avail_pwr >= pd_class_sig+5) +(pse_avail_pwr > 5)) to exist.

That would simply reduce to (pse_avail_pwr > 5), right?

TFTD LY

This is really a problem. The "+" operator is use for logical OR, and in these statements for addition as well.

Remedy:

- replace "pd req pwr = pd class sig+5" by "pd req pwr = sum(pd class sig, 5)" in MARK EV3
- replace "((pse avail pwr >= pd class sig+5) +)" by "((pse avail pwr >= sum(pd class sig, 5)) +)" in the arc from CLASS EV3 to MARK EV3

Response DNA:

I still don't see how ((pse_avail_pwr >= sum(pd_class_sig, 5)) +(pse_avail_pwr > 5)) does not reduce to (pse_avail_pwr > 5)...please explain.

TFTD DS

The term in question is trying to allow PSE w/ Class 5 power available, to negotiate w/ Class 5 PD.

This revision to transition logic does not make use of math operations:

CLASS_EV3 -> MARK_EV3

tcle3_timer_done * (pse_alternative = both) * (pd_class_sig != 4) * (pse_avail_pwr > 4) * ((pd_class_sig = 0) + (pse_avail_pwr > 5))

CLASS_EV3 -> MARK_EV_LAST

tcle3_timer_done * ((pse_alternative != both) + (pd_class_sig = 4) + (pse_avail_pwr <= 4) + ((pd_class_sig != 0) * (pse_avail_pwr <= 5)))

Cl 145 SC 145.2.5.8 P 130 L 34 # i-474

Darshan, Yair

Comment Type T Comment Status D PSE SD

In the POWER_ON state we are addressing two use cases:

- a) The PSE is working over 4-pairs
- b) The PSE is working over 2-pairs for class <5

If we work over 4-pairs and we had error on the pri for example, we are allowing the sec keep working until the sec will have error (in this case we go to IDLE) or the sec will continue to work.

In the case that the sec is continued to work, we need to move to SEMI_PWR_SEC state in page 131 which is done by the exit from POWER_ON to SEMI_PWR_SEC which is:

semi_pwr_en * !error_sec * error_pri.

Now we are in SEMI_PWR_SEC and our options to exit from SEMI_PWR_SEC is when we have erro_sec (going to IDLE) or not sufficient power (going to POWER_DENIDE and then to IDLE) or tmpdo_timer_done (going to IDLE)

So far all is good.

Now if the use case is that the port is working with single-signature PD over 2-pairs, class <5. This will cause issue in the state machine. Why?

1. The above use case means per the POWER_ON state alt_pwrd_pri=TRUE and alt_pwrd_pri=FALSE i.e. only the pri is ON.

2. Now something happened and I have error event on the pri.

3. When I have error event on the primary, the condition from POWER_ON to SEMI_POWER_ON_SEC became true: semi_pwr_en * !error_sec * error_pri and we move to SEMI_POWER_ON_SEC which is a problem...THE SEC was OFF already...so I can't be in SEMI_POWER_ON_SEC. So the question is, what we have to do to exit from SEMI_POWER_ON_SEC back to IDLE or block us from going to SEMI_POWER_ON_SEC?

The simplest way is: to prevent going to SEMI_POWER_ON_SEC in this case and allow going to IDLE through the ERROR_DELAY state.

SuggestedRemedy

1. Make the following changes in the exit from POWER_ON to SEMI_PWRON_SEC:

Change from: "semi_pwr_en * !error_sec * error_pri"

To: "semi_pwr_en * !error_sec * error_pri*alt_pwrd_sec"

2. Make the following changes in the exit from POWER_ON to ERROR_DELAY:

Change from:"(!semi_pwr_en*(error_pri+ error_sec))+ (semi_pwr_en*error_pri* error_sec)"

To:"(!semi_pwr_en*(error_pri+error_sec))+ (semi_pwr_en*error_pri*error_sec)+ (semi_pwr_en*error_pri*!alt_pwrd_sec)"

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

TFTD

Can someone more familiar with the SD check this logic.

TFTD LY

This indeed can get a state diagram stuck in one of the SEMI PWRON states.

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Fix as follows:

– Arc from POWER ON to SEMI PWRON SEC:

semi pwr en * alt pwr sec * !error sec * error pri

– Arc from POWER ON to ERROR DELAY:

(!semi pwr en * (error pri + error sec)) +

(semi pwr en * error pri * (error sec + !alt pwr sec))

I come to the same logic as Yair (though slightly shorter).

TFTD DS

This fix works, but we can reduce the 2nd and 3rd terms of in (2) with no effect to function:

(!semi_pwr_en * (error_pri + error_sec)) + (semi_pwr_en * error_pri * (error_sec + !alt_pwr_sec))

Cl 145 SC 145.2.5.7 P 131 L 6 # i-400

Darshan, Yair

Comment Type T Comment Status D PSE SD

In the exit from SEMI_PWRON_PRI to POWER_DENIED need to be !power_available_pri and not !power_available

SuggestedRemedy

Change from "!power_available" to "!power_available_pri"

Proposed Response Response Status W

PROPOSED REJECT.

Power_available_pri is only used in the SISMs, not in the top-level SD.

TFTD YD

"AIP: Add explanation to variable description that power_available is for SS and the _pri and _sec are for DS.Rename SEMI_PWRON_PRI to PRI_SEMI_PWRON (same for SEC)"

Cl 145 SC 145.2.5.7 P 131 L 7 # i-401

Darshan, Yair

Comment Type T Comment Status D PSE SD

In the exit from SEMI_PWRON_PRI to IDLE need to be power_available_pri and not power_available

SuggestedRemedy

Change from "power_available" to "power_available_pri"

Proposed Response Response Status W

PROPOSED REJECT.

Power_available_pri is only used in the SISMs, not in the top-level SD.

TFTD YD

See 400

Cl 145 SC 145.2.5.7 P 131 L 21 # i-402

Darshan, Yair

Comment Type T Comment Status D PSE SD

In the exit from SEMI_PWRON_SEC to POWER_DENIED need to be !power_available_sec and not !power_available

SuggestedRemedy

Change from "!power_available" to "!power_available_sec"

Proposed Response Response Status W

PROPOSED REJECT.

Power_available_sec is only used in the SISMs, not in the top-level SD.

TFTD YD

See 400

Cl 145 SC 145.2.5.7 P 131 L 25 # i-403

Darshan, Yair

Comment Type T Comment Status D PSE SD

In the exit from SEMI_PWRON_SEC to IDLE need to be power_available_sec and not power_available

SuggestedRemedy

Change from "power_available" to "power_available_sec"

Proposed Response Response Status W

PROPOSED REJECT.

Power_available_sec is only used in the SISMs, not in the top-level SD.

TFTD YD

See 400

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

CI 145 SC 145.2.5.7 P 131 L 39 # i-404
 Darshan, Yair

Comment Type T Comment Status X Pres: Yseboodt7

In the Exit from IDLE_ACS to WAIT_ACS we have the following conditions:
 pd_autoclass * !tpon_timer_done * tinrush_timer_pri_done * pwr_app_pri * (!alt_pwr_sec + tinrush_timer_sec_done * pwr_app_sec)

It looks that we have two issues here:

1) redundancy in the term " tinrush_timer_pri_done * pwr_app_pri. If pwr_app_pri is true, it means that tinrush_timer_pri_done is TRUE as well.

2) the term (!alt_pwr_sec + (tinrush_timer_sec_done * pwr_app_sec)) is always TRUE.

- alt_pwr_sec in false meaning that "The PSE is not to apply power to the Primary Alternative. "

- tinrush_timer_sec_done * pwr_app_pri indicates that we POWER up secondary pair and inrush is done in the secondary.

So, we have a condition that if we power up/or not power up.

It's like doing (X or not X) that is always true, which requires to remove this term completely...

In order to find what we really need here, let's expand the whole original term. It is equivalent to the following two parts:

a) pd_autoclass * !tpon_timer_done * tinrush_timer_pri_done * pwr_app_pri * !alt_pwr_sec +

b) pd_autoclass * !tpon_timer_done * tinrush_timer_pri_done * pwr_app_pri

*tinrush_timer_sec_done * pwr_app_sec

I believe that our intent is to allow Autoclass for Type 3 and 4 PSEs supporting single-signature PDs over 4-pairs or Type 3 PSE supporting SS-PD over 2-pairs.

There are few issues:

In part (a), redundancy in the term " tinrush_timer_pri_done * pwr_app_pri ".

If pwr_app_pri is true, it means that tinrush_timer_pri_done is TRUE as well.

As a result, it is sufficient to reduce this term from " tinrush_timer_pri_done * pwr_app_pri " to "pwr_app_pri", resulting with term (a):

"pd_autoclass * !tpon_timer_done * pwr_app_pri * !alt_pwr_sec"

In part (b), the same concept as in part (a) applies to tinrush_timer_sec_done *

pwr_app_sec i.e. If pwr_app_sec is true, it means that tinrush_timer_sec_done is TRUE as well.

As a result, we can reduce term (b) to:

"pd_autoclass * !tpon_timer_done * pwr_app_pri * pwr_app_sec"

The net result is:

pd_autoclass * !tpon_timer_done * pwr_app_pri * !alt_pwr_sec + pd_autoclass *

!tpon_timer_done * pwr_app_pri * pwr_app_sec =

pd_autoclass * !tpon_timer_done * pwr_app_pri * (!alt_pwr_sec + pwr_app_sec)

SuggestedRemedy

Change from:

"pd_autoclass * !tpon_timer_done * tinrush_timer_pri_done * pwr_app_pri * (!alt_pwr_sec + tinrush_timer_sec_done * pwr_app_sec)"

To:

"pd_autoclass * !tpon_timer_done * pwr_app_pri * (!alt_pwr_sec + pwr_app_sec)"

Proposed Response Response Status W

TFTD

Can someone confirm this logic?

TFTD LY

It is not fully equivalent and introduces a difference in timing. Probably OBE by yseboodt 07

WFP

TFTD DS

Reject.

Addressing the commentor's points:

1) This is a straight copy-paste of transition logic from POWER_UP to POWER_ON, as intended. The timer check should remain in both locations, as pwr_app_x does not evaluate inrush timer.

2) Disagree. If the PSE is applying power on alt_sec and inrush is not completed on alt_sec, this argument is false. I assume you ultimately came to agree on this point, as the suggested remedy maintains the logic "!alt_pwr_sec + pwr_app_sec".

CI 145 SC 145.2.5.7 P 132 L 4 # i-195

Peker, Arkadiy Microsemi Corporation

Comment Type TR Comment Status X PSE SD

Missing error_condition_pri at the input to the state IDLE_PRI at the condition iclass_lim_det_pri.

SuggestedRemedy

1. Change from: "iclass_lim_det_pri" to "iclass_lim_det_pri + error_condition_pri"

2. Add new variable to 145.2.5.4:

"error_condition_pri

A variable indicating the status of implementation-specific fault conditions or optionally other system faults that prevent the PSE from meeting the specifications in Table 145-16 and that require the PSE not to source power over the Primary Alternative.

Values:

FALSE: No fault indication.

TRUE: A fault indication exists.

Proposed Response Response Status W

TFTD

Do we want to create pri and sec versions of error_condition?

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.5.7 P 133 L 5 # i-198
 Peker, Arkadiy Microsemi Corporation

Comment Type TR Comment Status X PSE SD

Figure 145-15 doesn't have the option of using short class event when doing "class probe" functionality as we have in single-signature class probe case. This cost with more time to complete process and more power dissipation. The same applies to the secondary part in page 137. It is suggested to replicate CLASSIFICATION pre-state and CLASS_PROBE from page Figure 145-13 page 128 in primary and secondary state machines with the relevant modifications.

SuggestedRemedy

Adopt darshan_04_0917.pdf

Proposed Response Response Status W

TFTD

WFP

Cl 145 SC 145.2.5.7 P 133 L 13 # i-229
 Peker, Arkadiy Microsemi Corporation

Comment Type TR Comment Status D PSE SD

"In the exit from CLASS_EV2_PRI to MARK_EV2_PRI, the variable option_2ev is missing in the condition:
 tcle2_timer_pri_done *(pd_class_sig_pri = temp_var_pri) * (class_4PID_mult_events_pri +(pse_avail_pwr_pri > 4)).
 It needs to be the same concept as in the single-signature case."

SuggestedRemedy

Change from:

"tcle2_timer_pri_done *(pd_class_sig_pri = temp_var_pri) * (class_4PID_mult_events_pri +(pse_avail_pwr_pri > 4))"

To:

"tcle2_timer_pri_done * (pd_class_sig_pri = temp_var_pri) * ((class_4PID_mult_events_pri * !option_2ev)+(pse_avail_pwr_pri > 4)) "

Proposed Response Response Status W

TFTD

Do we want to use the same variable for SS and DS?

TFTD LY

This logic is wrong. To make sure we adopt the corrected version (Yair has it).

TFTD YD

"1. There is an error in the proposed remedy: It should be:""tcle2_timer_pri_done * (pd_class_sig_pri = temp_var_pri) * ((class_4PID_mult_events_pri + !option_2ev + (pse_avail_pwr_pri > 4)) ""2. And the answer for comment editor question ""Do we want to use the same variable for both SS and DS"" is YES since not need to seperate within a port the option for primary and secondary."

TFTD DS

Setting class_4PID_mult_events_x FALSE already enables PSE to limit to 2 class events. We do not need an option_ev2 for dual-signature diagrams.

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.5.8 P 133 L 18 # i-469
 Darshan, Yair

Comment Type E Comment Status D PSE SD

In the exit from CLASS_EV2_SEC to MARK_EV_LAST_SEC, the condition:
 "tcle2_timer_sec_done * (pd_class_sig_sec = temp_var_sec) *
 !class_4PID_mult_events_sec * pse_avail_pwr_sec = 4" is missing parenthesis in
 "pse_avail_pwr_sec = 4".

SuggestedRemedy

Change from:
 "tcle2_timer_sec_done * (pd_class_sig_sec = temp_var_sec) *
 !class_4PID_mult_events_sec * pse_avail_pwr_sec = 4"
 To:
 "tcle2_timer_sec_done * (pd_class_sig_sec = temp_var_sec) *
 !class_4PID_mult_events_sec * (pse_avail_pwr_sec = 4)"

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Change from:
 "tcle2_timer_sec_done * (pd_class_sig_sec = temp_var_sec) *
 !class_4PID_mult_events_sec * pse_avail_pwr_sec = 4"
 To:
 "tcle2_timer_sec_done * (pd_class_sig_sec = temp_var_sec) *
 !class_4PID_mult_events_sec * (pse_avail_pwr_sec = 4)"

on page 137 (comment says page 133 by mistake).

TFTD YD

"The comment editor is correct it is page 137 for the secondary. However the same problem apply for page 133 on the primary. So the same fix apply to the primary on page 133."

Cl 145 SC 145.2.5.8 P 133 L 18 # i-230
 Peker, Arkadiy Microsemi Corporation

Comment Type TR Comment Status X PSE SD

"In the exit from CLASS_EV2_PRI to MARK_EV_LAST_PRI, the variable option_2ev is missing in the condition:
 "tcle2_timer_pri_done * (pd_class_sig_pri = temp_var_pri) * !class_4PID_mult_events_pri *
 pse_avail_pwr_pri = 4".
 It needs to be the same concept as in the single-signature case."

SuggestedRemedy

"Change from:
 "tcle2_timer_pri_done * (pd_class_sig_pri = temp_var_pri) * !class_4PID_mult_events_pri *
 pse_avail_pwr_pri = 4"
 To:
 "tcle2_timer_pri_done * option_2ev * (pd_class_sig_pri = temp_var_pri) *
 !class_4PID_mult_events_pri * pse_avail_pwr_pri = 4"

Proposed Response Response Status W

TFTD

Do we want to use same variable for SS and DS?

TFTD LY

This logic is wrong. To make sure we adopt the corrected version (Yair has it).

TFTD DS

Setting class_4PID_mult_events_x FALSE already enables PSE to limit to 2 class events. We do not need an option_ev2 for dual-signature diagrams.

Cl 145 SC 145.2.5.7 P 135 L 37 # i-410
 Darshan, Yair

Comment Type T Comment Status X PSE SD

In the exit from ERROR_DELAY_PRI to IDLE we have the following condition:
 "ted_timer_pri_done + option_detect_ted_pri".
 A) The variable option_detect_ted_pri is missing from the variable list.
 B) in addition I believe it is not required since if you have the option to do detection during Ted time interval or you dont have the option, you are going to IDLE_PRI and in IDLE_PRI you don't do detection.

SuggestedRemedy

Change from: " "ted_timer_pri_done + option_detect_ted_pri"
 To: "ted_timer_pri_done "

Proposed Response Response Status W

TFTD

What was the intent of this variable?

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.5.7 P 136 L 4 # i-199
 Pekar, Arkadiy Microsemi Corporation

Comment Type TR Comment Status X PSE SD

Missing error_condition_sec at the input to the state IDLE_SEC at the condition iclass_lim_det_sec.

SuggestedRemedy

1. Change from: ""iclass_lim_det_sec"" to ""iclass_lim_det_sec + error_condition_sec""
2. Add new variable to 145.2.5.4:

""error_condition_sec

A variable indicating the status of implementation-specific fault conditions or optionally other system faults that prevent the PSE from meeting the specifications in Table 145-16 and that require the PSE not to source power over the Secondary Alternative.

Values:

FALSE: No fault indication.

TRUE: A fault indication exists."

Proposed Response Response Status W

TFTD

Do we want pri and sec versions of error_condition?

Cl 145 SC 145.2.5.7 P 136 L 11 # i-254
 Pekar, Arkadiy Microsemi Corporation

Comment Type TR Comment Status X Pres: Darshan13

In the exit from IDLE_SEC to START_DETECT_SEC we have the following condition:
 "(!pwr_app_sec * pwr_app_pri) + ((CC_DET_SEQ=3) * option_probe_alt_sec * !det_start_pri * !det_once_sec)"

Based on the description in page 109 lines 37-38 for CC_DET_SEQ and specifically, CC_DET_SEQ=3 for dual-signature means: Connection check is followed by staggered detection

(The analysis and simulations results for other sequences 0, 1 and 2 are covered by other comments and most of them are OK).

The staggered detection range may occur with starting the secondary detection after doing the primary detection (option 1) up to doing the secondary detection only if the primary is on (option 2). This covers the full range of possibilities.

Option 1 is normally used when class_4PID_mult_events_sec=TRUE. This currently is not covered by the state machine.

Option 2 is normally used when class_4PID_mult_events_sec=FALSE and it is covered in the 1st part of the condition: (!pwr_app_sec * pwr_app_pri).

Option 3 is covers the case that the primary return to IDLE_PRI due to various reasons and the secondary didn't detect even once: ((CC_DET_SEQ=3) * option_probe_alt_sec * !det_start_pri * !det_once_sec).

The current state diagram covers option 2 and 3, and does not cover option 1!

The state diagram should allow staggered detection before Primary power up, after primary power up, and during power up in case that class_4PID_mult_events_sec is set to FALSE. The proposed changes in the state diagram will allow staggered detection after Primary finished its 1st detection without affecting the previous functionality and flow, by oring the additional missing possibility (option 1).

The proposed changes do not affect:

- a) The behavior of other "CC_DET_SEQ NE 3" flows.
- b) Previous state diagram possibilities.

In addition, the proposed changes also required to cover multiple cycles of detection+classification until host decides to power on the port (which is covered by darshan_04_0917.pdf).

The additional missing possibility is covered by adding the following part:

+ (class_4PID_mult_events_sec*(CC_DET_SEQ=3) * !det_once_sec * det_once_pri)

In order to implement the addition, we need to add the following variable for the primary side (similar variable is already exist for the secondary):

"det_once_pri

This variable indicates if the PSE has probed the Primary Alternative at least once, when entering to DETECT_EVAL_PRI.

Values:

FALSE: The PSE has not probed on the Primary Alternative since entering the Primary Alternative state diagram.

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

TRUE: The PSE has probed the Primary Alternative at least once since entering the Primary Alternative state diagram."

In the above proposed change, det_once_pri is used as a condition for starting detection in the secondary any time until power up, after primary was detected at least once. det_once_pri is set to FALSE when sism = FALSE at ENTRY_PRI. det_once_pri is set to TRUE when Primary state diagram reaches to "DETECT_EVAL_PRI", to clearly indicate that detection on primary has ended before tdet_timer_pri expired."

SuggestedRemedy

1. Change from:
 "(!pwr_app_sec * pwr_app_pri) + ((CC_DET_SEQ=3) * option_probe_alt_sec * !det_start_pri * !det_once_sec)"
 To:
 "(!pwr_app_sec * pwr_app_pri) + ((CC_DET_SEQ=3) * option_probe_alt_sec * !det_start_pri * !det_once_sec) + (class_4PID_mult_events_sec*(CC_DET_SEQ=3) * !det_once_sec * det_once_pri)"
 2. Add the following variable to the variable list:
 det_once_pri
 This variable indicates if the PSE has probed the Primary Alternative at least once, when entering to DETECT_EVAL_PRI. Values:
 FALSE: The PSE has not probed on the Primary Alternative since entering the Primary Alternative state diagram.
 TRUE: The PSE has probed the Primary Alternative at least once since entering the Primary Alternative state diagram.
 "

<i>Proposed Response</i>	<i>Response Status</i>	W
TFTD		
WFP		

<i>Cl</i> 145	<i>SC</i> 145.2.5.7	<i>P</i> 136	<i>L</i> 20	<i>#</i> i-251
Peker, Arkadiy		Microsemi Corporation		

<i>Comment Type</i>	TR	<i>Comment Status</i>	X	<i>Pres:</i> Darshan13
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In Figure 145-16, in the exit from ENTRY_SEC to START_DET_SEC, when selecting CC_DET_SEQ 0 or 1, and class_4PID_multi_event_sec = FALSE, the secondary state machine allows to move from ENTRY_SEC state to START_DETECT_SEC only if pwr_app_pri = TRUE per the existing condition:
 sism * ((!class_4PID_mult_events_sec * pwr_app_pri) + class_4PID_mult_events_sec) * (CC_DET_SEQ=0 + CC_DET_SEQ=1)

If Primary fails to powerup, the Primary state machine returns back to IDLE_PRI. As a result, pwr_app_pri variable will remain in FALSE, and the secondary state machine won't be able to exit from ENTRY_SEC i.e. will be stuck there.
 The easy way to handle this problem is to enable moving to START_DETECT_SEC from ENTRY_SEC, also if primary performed detection at least once and is now in IDLE_PRI state which prevents stuck at ENTRY_SEC. This solution requires the addition of new variable det_once_pri (the current draft has only det_once_sec) which is required also by other comments that all related to each other and can be see in darshan_04_0917.pdf. "

SuggestedRemedy

See darshan_04_0917.pdf for how the following change is also addresses other issues including the possibility to do cycles of detection + class_probe events on primary and secondary with the option to go to IDLE_PRI/SEC and WAIT_PRI/SEC.

 1) Add the following variable:
 det_once_pri
 This variable indicates if the PSE has probed the Primary Alternative at least once, when entering to DETECT_EVAL_PRI. Values:
 FALSE: The PSE has not probed on the Primary Alternative since entering the Primary Alternative state diagram.
 TRUE: The PSE has probed the Primary Alternative at least once since entering the Primary Alternative state diagram.
 2) Change from:
 "sism * ((!class_4PID_mult_events_sec * pwr_app_pri) + class_4PID_mult_events_sec) * (CC_DET_SEQ=0 + CC_DET_SEQ=1)"
 To:
 sism * ((!class_4PID_mult_events_sec * (pwr_app_pri + det_once_pri * !det_start_pri)) + class_4PID_mult_events_sec) * (CC_DET_SEQ=0 + CC_DET_SEQ=1)."

<i>Proposed Response</i>	<i>Response Status</i>	W
TFTD		
WFP		

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.5.7 P 136 L 20 # i-250
Peker, Arkadiy Microsemi Corporation

Comment Type ER Comment Status X Pres: Darshan4

There is redundant parenthesis in the exit from ENTRY_SEC to START_DETECT_SEC:
"sism *((!class_4PID_mult_events_sec * pwr_app_pri) + class_4PID_mult_events_sec) *
(CC_DET_SEQ=0 + CC_DET_SEQ=1)"
in the part: (!class_4PID_mult_events_sec * pwr_app_pri). "

SuggestedRemedy

Change from:
"sism *((!class_4PID_mult_events_sec * pwr_app_pri) + class_4PID_mult_events_sec) *
(CC_DET_SEQ=0 + CC_DET_SEQ=1)"
To:
"sism *((!class_4PID_mult_events_sec * pwr_app_pri + class_4PID_mult_events_sec) *
(CC_DET_SEQ=0 + CC_DET_SEQ=1)"

See darshan_04_0917.pdf for additional changes proposed to this condition due to other comments."

Proposed Response Response Status W

TFTD

WFP

TFTD LY

By removing these parens we both reduce clarity, and we now depend on operator precedence and-before-or. Something we said we would avoid.

TFTD YD

"This is no longer in darshan_04 and the proposed remedy is complete without the need for presentation. Deletete the text ""See darshan_04_0917.pdf for additional changes proposed to this condition due to othercomments."""

Cl 145 SC 145.2.5.7 P 136 L 21 # i-252
Peker, Arkadiy Microsemi Corporation

Comment Type TR Comment Status X Pres: Darshan13

In the transition between ENTRY_SEC to START_DET_SEC we have the following condition:

"sism *((!class_4PID_mult_events_sec * pwr_app_pri) + class_4PID_mult_events_sec) *
(CC_DET_SEQ=0 + CC_DET_SEQ=1)"

In this condition, when class_4PID_mult_events_sec=FALSE, and CC_DET_SEQ=0 OR 1, If START_DET_PRI exit to IDLE_PRI due to tdet_timer_pri_done, the pwr_app_pri will remain in FALSE which won't allow exiting from ENTRY_SEC to START_DETECT_SEC and the secondary state machine remain stuck in ENTRY_SEC.

The proposed solution for this problem is:

- 1) To add stop_tdet_timer_pri in the DETECT_EVAL_PRI state. This action ensures that tdet_timer_pri_done will remain FALSE when moving from START_DETECT_PRI to DETECT_EVAL_PRI. This modification is required since even if we did detection before tdet_timer_pri is expired, we will get tdet_timer_pri_done anyway. This action will enables the usage of tdet_timer_pri_done in the secondary state machine at the exit from ENTRY_SEC to START_DETECT_SEC when we will add this variable in (2).
2. To add ""tdet_timer_pri_done to the condition of the exit from ENTRY_SEC to START_DETECT_SEC as follows:
"sism *((!class_4PID_mult_events_sec * (pwr_app_pri + tdet_timer_pri_done)) +
class_4PID_mult_events_sec) * (CC_DET_SEQ=0 + CC_DET_SEQ=1)"" . This change will allow to move to START_DETECT_SEC in case that we move from START_DETECT_PRI to IDLE_PRI due to tdet_timer_pri expiration."

SuggestedRemedy

1. Add "stop_tdet_timer_pri" to the DETECT_EVAL_PRI state.
2. Add "tdet_timer_pri_done to the condition of the exit from ENTRY_SEC to START_DETECT_SEC by performing the following change:

Change from:
"sism *((!class_4PID_mult_events_sec * pwr_app_pri) + class_4PID_mult_events_sec) *
(CC_DET_SEQ=0 + CC_DET_SEQ=1)"

To:
"sism *((!class_4PID_mult_events_sec * (pwr_app_pri + tdet_timer_pri_done)) +
class_4PID_mult_events_sec) * (CC_DET_SEQ=0 + CC_DET_SEQ=1)"

Due to the fact that item 2 need additional changes due to other comments, and in order to meet the requirement that we need single independent comment for each issue which I did here but may cause editor confusion of how to apply the remedies of other comments, See darshan_04_0917.pdf for how the above change is combined with other changes i.e. the possibility to do cycles of detection + class_probe events on primary and secondary with the option to go to IDLE_PRI/SEC and WAIT_PRI/SEC."

Proposed Response Response Status W

TFTD

WFP

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

CI 145 SC 145.2.5.8 P 137 L 13 # i-231
 Pekar, Arkadiy Microsemi Corporation

Comment Type TR Comment Status X PSE SD

In the exit from CLASS_EV2_SEC to MARK_EV2_SEC, the variable option_2ev is missing in the condition:
 ""tcle2_timer_sec_done *(pd_class_sig_sec = temp_var_sec) * (class_4PID_mult_events_sec +(pse_avail_pwr_sec > 4))".
 It needs to be the same concept as in the single-signature case."

SuggestedRemedy

Change from:"tcle2_timer_sec_done *(pd_class_sig_sec = temp_var_sec) * (class_4PID_mult_events_sec +(pse_avail_pwr_sec > 4))"
 To: "tcle2_timer_sec_done *(pd_class_sig_sec = temp_var_sec) * ((class_4PID_mult_events_sec * !option_2ev) + (pse_avail_pwr_sec > 4))"

Proposed Response Response Status W

TFTD

Do we want to use the same variable for both SS and DS?

TFTD LY

This logic is wrong. To make sure we adopt the corrected version (Yair has it).

TFTD YD

"1. There is an error in the proposed remedy: It should be:"tcle2_timer_sec_done *(pd_class_sig_sec = temp_var_sec) * ((class_4PID_mult_events_sec + !option_2ev + (pse_avail_pwr_sec > 4))". 2. And the answer for comment editor question ""Do we want to use the same variable for both SS and DS"" is YES since not need to separate within a port the option for primary and secondary."

TFTD DS

Setting class_4PID_mult_events_x FALSE already enables PSE to limit to 2 class events. We do not need an option_ev2 for dual-signature diagrams.

CI 145 SC 145.2.5.8 P 137 L 18 # i-232
 Pekar, Arkadiy Microsemi Corporation

Comment Type TR Comment Status X PSE SD

In the exit from CLASS_EV2_SEC to MARK_EV_LAST_SEC, the variable option_2ev is missing in the condition:
 "tcle2_timer_sec_done * (pd_class_sig_sec = temp_var_sec) * !class_4PID_mult_events_sec * pse_avail_pwr_sec = 4".
 It needs to be the same concept as in the single-signature case."

SuggestedRemedy

Change from:
 "tcle2_timer_sec_done * (pd_class_sig_sec = temp_var_sec) * !class_4PID_mult_events_sec * pse_avail_pwr_sec = 4"
 To:
 "tcle2_timer_sec_done * option_2ev* (pd_class_sig_sec = temp_var_sec) * !class_4PID_mult_events_sec * pse_avail_pwr_sec = 4"

Proposed Response Response Status W

TFTD

Do we want to use the same variable for both SS and DS?

TFTD LY

This logic is wrong. To make sure we adopt the corrected version (Yair has it).

TFTD DS

Setting class_4PID_mult_events_x FALSE already enables PSE to limit to 2 class events. We do not need an option_ev2 for dual-signature diagrams.

CI 145 SC 145.2.5.7 P 139 L 37 # i-416
 Darshan, Yair

Comment Type T Comment Status X PSE SD

In the exit from ERROR_DELAY_SEC to IDLE we have the following condition:
 "ted_timer_sec_done + option_detect_ted_sec".
 A) The variable option_detect_ted_sec is missing from the variable list.
 B) in addition I believe it is not required since if you have the option to do detection during Ted time interval or you dont have the option, you are going to IDLE_SEC and in IDLE_SEC you dont do detection.

SuggestedRemedy

Change from: " "ted_timer_sec_done + option_detect_ted_sec"
 To: "ted_timer_sec_done "

Proposed Response Response Status W

TFTD

What was the purpose of this variable?

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Cl 145 SC 145.2.6 P 141 L 20 # i-73
 Yseboodt, Lennart Philips Lighting

Comment Type T Comment Status D PSE Detection

"In any operational state, the PSE shall not apply operating power to a pairset until the PSE has successfully detected a valid signature over that pairset."

A PSE does not apply power, it applies voltage and the PD draws current, causing power to be sourced.

The term 'operating power' is not defined either.

"In any operation state" are 4 redundant words.

SuggestedRemedy

"The PSE shall not apply operating voltage to a pairset until the PSE has successfully detected a valid signature over that pairset."

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD YD

"Change to: ""The PSE shall not apply operating voltage to a pairset until the PSE has

successfully detected a valid signature over that pairset, with the exception of operating in test mode.""

TFTD DS

The state diagram and the other normative statements in the PSE detection section make this a redundant requirement. Repairing this statement would require a lot of nuance (considerations for TEST_MODE states, "greater than v_valid" vs "operating voltage"). Delete redundant requirement.

Cl 145 SC 145.2.6 P 141 L 29 # i-203
 Peker, Arkadiy Microsemi Corporation

Comment Type TR Comment Status X PSE Detection

We have the following text: "Also, a PSE may successfully detect a PD but then opt not to power the detected PD.". We need similar text for the classification i.e. "A PSE may successfully detect and classify a PD but then opt not to power that PD. " to be added at the end of clause 145.2.7 page 148 after line 38.

SuggestedRemedy

Add the following text in 145.2.7 page 148 after line 38: "A PSE may successfully detect and classify a PD but then opt not to power that PD. "

Proposed Response Response Status W

TFTD

I don't see the need for this statement as it is a subset of the sentence you point out in the comment.

TFTD YD

"Yair: It is not subset. It doesnt say that I can detect and classify and then opt not power. See Lennart and my proposal to merge it all to one sentence instead of the proposed remedy:""Also, a PSE may successfully detect a PD or detect and classify a PD, but then opt not to power the detected PD.""

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

CI 145 SC 145 P 142 L 10 # i-1
 Anslow, Peter Ciena Corporation

Comment Type TR Comment Status X Editorial

The IEEE-SA Standards Style Manual 13.3.2 says "An em dash (--) should be used to indicate the lack of data for a particular cell in a table."
 Comment #29 against P802.3bt D2.4 was: "Several tables in Clause 145 have blank cells in the min or max columns, which should contain an em-dash", but this was rejected with the rebuttal:
 "The lack of em-dashes is intentional. The em-dash would convey that there is no relevant information, while the lack of the em-dash conveys that there is no specific number."
 This makes no sense.
 The first example of this issue is in Table 145-7. "Connection check to detection time" Tcc2det has a maximum value of 0.4 s, but the min column is blank. According to the IEEE style manual the cell should contain an em dash, which would indicate that there is no minimum requirement for this time. If there is some requirement on the minimum (not just a number) then an indication of this should be made via an entry in the cell such as "See 145.x.x". If this is not the case, then the cell should contain an em dash.

SuggestedRemedy

Make sure all tables have an entry of em-dash or pointer to the requirement in currently blank min or max columns.
 In particular, Tables 145-7, 145-8, 145-9, 145-10, 145-14, 145-16, 145-20, 145-27, 145-28, 145-30, 145-31, 145-32.

Proposed Response Response Status W

TFTD

TFTD LY

There is a distinction between an em-dash, which indicates 'a lack of data', and leaving a cell blank. Eg. for parameters that convey a range, having a blank 'Min' cell, does NOT indicate there is lack of data, rather that the minimum value is open-ended. An em-dash would convey an incorrect message. Em-dashes have been put in all cells where it is appropriate. This seems consistent with other Clauses, I found many tables with empty cells: Table 78-4, 80-2, 80-3, 80-4, 82-1, 85-1, 85-5, 85-7, 86-2, 86-6, 86-7, 88-9, 89-6, 91-1, 92-8, 94-16, 94-17, 95-6, 95-7.

CI 145 SC 145.2.6.3 P 143 L 34 # i-76
 Yseboodt, Lennart Philips Lighting

Comment Type E Comment Status X Editorial

In Table 145-8 is written; "In detection state or connection check state".
 Detection and connection check happen in multiple states.

SuggestedRemedy

Change to:
 "In detection states or connection check states" (two occurrences in Table 145-8)

Proposed Response Response Status W

TFTD

Why do we need this text at all? This whole table is about detection. Should it say "Also applies to connection check"? Also, why doesn't Vvalid have this note since it also applies to connection check.

CI 145 SC 145.2.7 P 146 L 41 # i-79
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status X PSE Power

Topic: SLIDING
 "Measurements should be averaged using any sliding window with a width of 1 s."

This sentence follows after the definition of PClass and PClass-2P. That whole section is informative in nature.

- Why is this a should ?
- Measurements of what ? PClass is a capability.
- The actual power requirement of a PSE is encoded in ICon-2P.

SuggestedRemedy

Remove quoted sentence.

Proposed Response Response Status W

TFTD

I believe this is the only mention of the window for Pclass. Is it ok to remove it?

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Cl 145 SC 145.2.7 P 148 L 36 # i-81
 Yseboodt, Lennart Philips Lighting

Comment Type **TR** Comment Status **X** PSE Class

"When connected to a dual-signature PD, a PSE operating over 4 pairs shall treat the requested power over each pairset independently."

Redundant and untestable. The requirement on ICon-2P clearly states that power is independently handled for each pairset.

A PSE is also allowed to allocate the greater of the pairset power to each pairset.

Classification must be performed on both pairsets of a dual-signature PD per line 25.

SuggestedRemedy

Remove quoted text.

Proposed Response Response Status **W**

TFTD

I believe this text was included to try to spike out one of the key points of the new clause.

How about: "When connected to a dual-signature PD, a PSE operating over 4 pairs treats the requested power over each pairset independently."

and how about moving it to the beginning of the paragraph on page 146, line 25.

TFTD YD

"The intent was to also to get rid of addressing unbalance in dual-sig so, don't remove the text and the ""shall"". And Lennart assumption that it is not testable is wrong. It is easy to to test. "

Cl 145 SC 145.2.7.1 P 149 L 36 # i-281
 Stewart, Heath Analog Devices Inc.

Comment Type **TR** Comment Status **D** Editorial

Typo.

SuggestedRemedy

Change T_CLE to T_LCE. _ indicates subscript.

Proposed Response Response Status **W**

PROPOSED ACCEPT.

TFTD YD

"This is correct for most states in Line 36. This may affect comments that are trying to not force using twice long class event timing in CLASS_EV1_LCE_4PID_PRI, or CLASS_EV1_LCE_4PID_SEC "

Cl 145 SC 145.2.7.1 P 149 L 40 # i-282
 Stewart, Heath Analog Devices Inc.

Comment Type **E** Comment Status **D** Editorial

Text is redundant to state machine. Because the PSE is in the CLASS_EV1_AUTO state is has already met the "PSE in the state CLASS_EV1_LCE does not measure I_Class in the range of class signature 0 and the " clause.

SuggestedRemedy

Change

If the Autoclass enabled PSE in the state CLASS_EV1_LCE does not measure IClass in the range of class signature 0 and the PSE in the state CLASS_EV1_AUTO does measure IClass in the range of class signature 0 this indicates the PD will perform Autoclass; see 145.2.7.2 and 145.3.6.2.

to

If the Autoclass enabled PSE in the state CLASS_EV1_AUTO does measure IClass in the range of class signature 0 this indicates the PD will perform Autoclass; see 145.2.7.2 and 145.3.6.2.

Proposed Response Response Status **W**

PROPOSED ACCEPT.

TFTD LY

Change to: If the Autoclass enabled PSE in the state CLASS EV1 AUTO measures IClass in the range of class signature 0 this indicates the PD will perform Autoclass; see 145.2.7.2 and 145.3.6.2.

TFTD YD

Need to check

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.7.1 P 151 L 11 # i-84
 Yseboodt, Lennart Philips Lighting

Comment Type T Comment Status D PSE Class

Table 145-14:

T_CLE2 has value 6ms to 30ms.
 T_CLE3 has value 6ms to 20ms.

Post clause split, there is no longer a reason to keep T_CLE2.

SuggestedRemedy

- Remove T_CLE2 from Table 145-14
- Rename T_CLE3 to T_CLE
- Change any mention of T_CLE2 and T_CLE3 in the draft to T_CLE:
 - * Remove tcle2 timers
 - * Rename tcle3 timers to tcle timers
 - * Update usage in the state diagram
 - * Update text in draft (Change T_CLE2 or T_CLE3 to T_CLE)

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD DS

This is a great comment. Since we're globally changing T_CLE, can we select a different name, to easily distinguish this variable from the similarly-named T_LCE? At a glance, they are very easy to mix up. Propose "T_CLS_EV".

Cl 145 SC 145.2.7.1 P 151 L 27 # i-86
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status D PSE SD

"If the PSE returns to IDLE, it shall maintain the PI voltage in the range of V Reset for a period of at least T Reset min before starting a new detection cycle."

Is contradicted by the state diagram, which does not have this requirement, invalidating this 'shall'.

SuggestedRemedy

- Add to IDLE state (Figure 145-13): "start tclass_reset_timer"
- Prepend "tclass_reset_timer_done * " to the logic from IDLE to START_CXN_CHK, START_DETECT, and START_CXN_CHK_DETECT.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD YD

To the same for dual-signature.

TFTD DS

The proposed remedy places a minimum 15ms startup delay on all PSEs, regardless of past state (for example, the PSE could be exiting a reset state). Perhaps we can capture transitions back to IDLE (but not from the OFFLINE state) through an arc that waits tclass_reset time?

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.7.2 P 151 L 44 # i-283
 Stewart, Heath Analog Devices Inc.

Comment Type E Comment Status D Autoclass

The preceding paragraph and the note do not match. The preceding paragraph hooks the start of the T_AUTO_PSEx timers to a specific arc entering the POWER_ON state. The table row incorrectly hooks the timer start to _any_ entry into the POWER_ON state.

SuggestedRemedy

Change
 Measured from the transition to state POWER_ON
 to
 Measured from the transition of the POWER_UP state to the POWER_ON state.
 Also change line 44 same page

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD LY
 Merge the two affected cells, only have text once.

TFTD YD
 Need to check

Cl 145 SC 145.2.8 P 152 L 29 # i-89
 Yseboodt, Lennart Philips Lighting

Comment Type E Comment Status D Editorial

Table 145-16, Item 1, Parameter = "Output voltage per pairset in the POWER_ON state".

SuggestedRemedy

Replace by: "Output voltage per pairset in POWER_ON"

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD DS
 OBE this by 289, which presents an alternate solution that includes all power on states (_pri, _sec as well).

Cl 145 SC 145.2.8 P 152 L 30 # i-289
 Stover, David Analog Devices Inc.

Comment Type TR Comment Status D PSE Power

Vport_PSE_diff and Vport_PSE-2P both apply to either pairset of the PSE when that pairset is in a power on state (POWER_ON, POWER_ON_PRI, POWER_ON_SEC). These items are are not labeled consistently in the table.

SuggestedRemedy

Change "Output voltage pair-to-pair difference" to "Output voltage pair-to-pair difference with both pairsets in a power on state"; Change "Output voltage per pairset in the POWER_ON state" to "Output voltage per pairset in a power on state".

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD LY
 Agree with changing item 1 Item 2 is well explained in 145.2.8.2. Do not explain things in parameter names, there is no horizontal room for that. Change item 2 parameter name to "Pair-to-pair voltage difference".

Cl 145 SC 145.2.8 P 152 L 38 # i-90
 Yseboodt, Lennart Philips Lighting

Comment Type E Comment Status D PSE Power

Table 145-16, item 10: T_CUT-2P.
 For parameters that deal with time and are not exclusive to dual-signature, the "-2P" suffix doesn't make too much sense.

SuggestedRemedy

Rename T_CUT-2P to T_CUT throughout Clause 145.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD YD
 Reject: The issue is not that it is exclusive for dual-sig. These parameters are part of a group that ensures that each pairset can be protected individually for single-signature and dual-signature. Using -2P add clarity for the intent and prevent intrpretations that the control on each pairset must be doe simultaneously.

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.8 P 152 L 46 # i-419

Darshan, Yair

Comment Type T Comment Status X Pres: Darshan3

Icon-2P_unb in Table 145-16 item 5 needs some updates to sync with latest changes and to fit the test verification models accuracy.

SuggestedRemedy

Adopt the changes proposed in darshan_03_0917.pdf

Proposed Response Response Status W

TFTD

WFP

Cl 145 SC 145.2.8 P 152 L 46 # i-463

Darshan, Yair

Comment Type T Comment Status X Pres: Darshan12

The following question has been asked regarding diode aging and its affect on PD_Vdiff that affect unbalance.

Background:

Our spec defines unbalance requirements for the PSE in terms of VPort_PSE-2P, Icon-2P_unb and for the PD in terms of Icon-2P_unb and inexplicit design requirement to keep PD_Vdiff=60mV max measured at 1-10mA range. The PD_Vdiff has the highest effect on the system current/resistance unbalance.

The following use case has been investigated:

A PD is connected to a PSE over 4-pairs. The PSE is using Alt A (MDI) and Alt B (X) resulting with 1,2 and 7,8 are positive and 3,6 and 4,5 are negative. It runs this way for MANY years. The PD front end is not an active bridge, it is a diode bridge. The PSE has been replaced and it uses Alt A (MDI) and Alt B (S). Now, 1,2 and 4,5 are positive and 3,6 and 7,8 are negative. Now we have diodes that have been aged (1,2 and 3,6) in parallel with diodes that have never have current through them (the ones in 4,5 and 7,8). This is not simply switching from the old diodes to the new ones, its mixing old with new. The questions are:

1. If the aging has an effect on Vf, then we may have higher mismatch between the diodes in parallel leading to higher unbalance.
2. In an extreme case, we may have a runaway situation as the aged diode drops more power and heats more than the 'new' diode.

Answers:

1. All diodes in the diode bridge has to have 60mV maximum Vdiff between any permutations of each two diodes.
2. Silicon doesn't have a memory. The performance characteristics change may changed after diode end of life time period due to mechanical construction and other issues that are function of current conduction.
3. Diodes that are at their end of life will introduce higher leakage current, higher VF, and other parameters will exceed the spec.
4. As long as the diode is kept with their allowed operating conditions, VF will not change significantly during the diode defined life time with or without current conduction.
5. Life time of a diode of reliable vendor can be 20 years. The lowest life time value of reliable vendors is 10 years. The typical is somewhere between these ranges.
6. As a result of the above, any component in the PD or PSE need to be selected with life time which exceed the product life time like any other designs.
7. If vendor follow the above rules, the effect of aging should not be a problem for VF (or other parameter).

SuggestedRemedy

See darshan_12_0917.pdf for details

Proposed Response Response Status W

TFTD

WFP

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.8 P 153 L 16 # i-290
 Stover, David Analog Devices Inc.

Comment Type T Comment Status X PSE Inrush

Item 6 specifies "Total output current...in the POWER_UP state per the assigned Class", but includes rows for "Type 3" and "Type 4" dual-signature PDs.

SuggestedRemedy

Change from "Type 3 dual-signature PD" to "Dual-signature PD, Class 1 to 4"; Change from "Type 4 dual-signature PD" to "Dual-signature PD, Class 5".

Proposed Response Response Status W

TFTD

Wait for outcome of 92

Cl 145 SC 145.2.8 P 153 L 16 # i-92
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status X PSE Inrush

Table 145-16, linrush (item 6) lists minimum values for dual-signature PDs. Dual-signature PDs may be started up in a staggered fashion, making this parameter meaningless. In general, dual-sig PDs are specified exclusively on a per pairset basis only, this needs to be the same here.

SuggestedRemedy

- Remove the two rows for dual-signature PDs in Item 6 of Table 145-16
- Remove the two rows for dual-signature PDs in Item 4 of Table 145-28

Proposed Response Response Status W

TFTD

TFTD YD

"DO NOT REMOVE.We need a limit to the total maximum.If you delete, the total max will be 1.2A! That is why we have these rows. The minimum total value may be deleted."

Cl 145 SC 145.2.8 P 153 L 16 # i-291
 Stover, David Analog Devices Inc.

Comment Type TR Comment Status X PSE Inrush

The PSE inrush requirements "I_Inrush" and "I_Inrush-2P" always apply. However, dual-signature PDs may be powered over one or both pairs. For this reason, specifying total output current (I_Inrush) for dual-signature PDs is problematic. For example: When a single pairset of a Type 4/Class 5 dual-signature PD is inrushed, the PSE shall provide an I_Inrush of at least 0.65A and shall not provide an I_Inrush-2P of more than 0.6A. For dual-signature PDs, output current during inrush should only be specified per-pairset.

SuggestedRemedy

Remove I_Inrush entries for dual-signature PDs.

Proposed Response Response Status W

TFTD

TFTD YD

"-The remedy doesnt make sense with the comment..which rows to remove? we can't remove any row..-You may want to remove only the minimum value of the total current for dual-sig row in item 6."

TFTD DS

Comment i-92 presents a superior remedy.

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.8 P 153 L 31 # i-485

Johnson, Peter

Comment Type T Comment Status X PSE Inrush

Dual Signature Class 5 Minimum I_Inrush-2P is specified as 325 mA. Class 5 Dual Signature PD's are specified in 145.3.8.3 as allowing up to 180uF for C_Port-2P without PD current limiting. Is there a rationale why 325mA current limiting meets the needs of a Class 5 Dual Signature but we require 400mA for all other cases where C_Port or C_Port-2P can go up to 180uF ?

SuggestedRemedy

Unless there is a justifiable reason, I_Inrush should be 800mA and I_Inrush-2P 400mA for the Type-4 Dual Signature case.

Proposed Response Response Status W

TFTD

That is a very good question Pete.

TFTD YD

"1. The rational was to allow foldback current limit that will start with 325mA.

2. To account for unbalance at the pair with the minimum current i.e. to ensure the the minimum current will be 325mA minimum after unbalance effect. This was proven by calculations made by me Yair and David Stover. I agree that it is better to set it to 0.4A as the rest."

Cl 145 SC 145.2.8 P 153 L 33 # i-205

Peker, Arkadiy

Microsemi Corporation

Comment Type TR Comment Status X Tpon

"Table 145-16, item 8, Tinrush: It is clear from the state machine that Tpon includes Tinrush. It means that effective Tpon is (400-50) msec=350ms or (400-75) ms=325msec which needs to cover long 1st class events, + 4 class events + design margin. group to discuss if it sufficient for their designs and applications in both single and dual-signatures. To consider if Tpon need to be increased by approximately 50msec to compensate for the increase in the 1st long class events to keep our margins as in 802.3af/at. It doesn't affect reliability etc. since we had so far 200msec margin from the 600msec value from the 802.3af experiments and the actual spec numbers."

SuggestedRemedy

Increase Tpon from 400msec to 450msec or to what ever the group decides.

Proposed Response Response Status W

TFTD

Adding up the class events you get:

95ms + 4*12ms + 5*9ms

(1st finger, 4 short class events, 5 mark events)

= 188ms

There seems to be plenty of margin.

TFTD YD

Response to David's calculations: If we want to power on at the same time it is marginal with typical numbers. If we power_on in staggered manar, then there is no issue.

TFTD CJ

I think worst case numbers are 105+4*20+5*12.

Response DNA: The PSE can choose not use worst case numbers...

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.8 P 153 L 33 # i-93

Yseboodt, Lennart

Philips Lighting

Comment Type E Comment Status D PSE Power

Table 145-16, item 8: T_Inrush-2P.
For parameters that deal with time and are not exclusive to dual-signature, the "-2P" suffix doesn't make too much sense.
On the PD side we call it T_Inrush_PD.

SuggestedRemedy

Rename T_Inrush-2P to T_Inrush in Clause 145.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD YD

Reject: The issue is not that it is exclusive for dual-sig. These parameters are part of a group that ensures that each pairset can be protected individually for single-signature and dual-signature. Using -2P add clarity for the intent and prevent interpretations that the control on each pairset must be done simultaneously.

Cl 145 SC 145.2.8 P 154 L 16 # i-421

Darshan, Yair

Comment Type T Comment Status X PSE Power

Resolve first comment marked CLASS8_PPD. Table 145-16 item 11, ILIM-2P. ILIM_2P is derived from Ipeak-2P_unb. The value of 0.99 was simulated when PClass_PD was 71W and as a result, Ppeak_PD was 1.05*71W. Now it is 71.3W and Ppeak_PD was already updated in all Tables and equation but not in related parameters in Table 145-16.
If Ppeak_PD for class 8 is 74.8W then ILIM-2P need to be 0.995A.
If Ppeak_PD for class 8 is 74.9W then ILIM-2P need to be 0.996A.

SuggestedRemedy

After resolving the comment marked CLASS8_PPD. Adopt the following options accordingly:

Option 1:

If Ppeak_PD for class 8 is 74.8W then ILIM-2P need to be 0.995A.

Option 2:

If Ppeak_PD for class 8 is 74.9W then ILIM-2P need to be 0.996A.

Proposed Response Response Status W

TFTD

See 437

Cl 145 SC 145.3.1 P 154 L 19 # i-285

Stewart, Heath

Analog Devices Inc.

Comment Type TR Comment Status X DLL

Data Link Layer Classification is deemed optional in Table 145-18. However, because a PSE is _allowed_ to select any one of 4 4PID inspection techniques (see 145.2.6.7), it logically follows that the PD _must_ exhibit all 4 of the 4PID characteristics.
Notably, the 1st characteristic (single-signature) is enough to prove a PD is 4PID compatible, thus a single-signature PD need not comply with the remaining 3 attributes. However, a dual-signature PD has little choice but to comply with all 3 attributes (2-4). Because the PD does not know which of the aforementioned tests will be performed it must have all 2-4 attributes in order to receive 4P power.

SuggestedRemedy

Change

Table 145-18, Type 3, Dual, 1 to 3 row :: Data Link Layer Classification column :: from "Optional" to "Mandatory"

Delete Table 145-18, Note 2

Page 184, Line 3 Change

Single-signature PDs that request Class 4 or higher and dual-signature PDs that request Class 4 or higher on at least one of its Modes shall provide DLL classification.

to

Single-signature PDs that request Class 4 or higher and dual-signature PDs shall provide DLL classification.

Proposed Response Response Status W

TFTD

Was the intention to let the PSE choose any of the methods?

TFTD YD

"YES. PSE can choose one of the methods. Practically PSE will use physical layer 4PID in dual-sig due to the fact that: (a) not all PDs using DLL. (2) Midspans can't use DLL. As a result LLDp in <Class 4 should stay optional."

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.8 P 154 L 23 # i-94
 Yseboodt, Lennart Philips Lighting

Comment Type E Comment Status D Editorial

Table 145-16, parameter 12: T_LIM-2P.
 For parameters that deal with time and are not exclusive to dual-signature, the "-2P" suffix doesn't make too much sense.

SuggestedRemedy

Rename T_LIM-2P to T_LIM throughout Clause 145.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD YD

Reject: The issue is not that it is exclusive for dual-sig. These parameters are part of a group that ensures that each pairset can be protected individually for single-signature and dual-signature. Using -2P add clarity for the intent and prevent interpretations that the control on each pairset must be done simultaneously.

Cl 145 SC 145.2.8 P 154 L 27 # i-95
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status X PSE Power

While this is not entirely unambiguous, the spec today requires a PSE to support at least Class 3, due to the PType(min) parameter having a value of 15.4W. The historic reason for this is that classification was optional and not well understood. By requiring at least support for Class 3, the situation was avoided that a PD was plugged in a nothing ever happened (eg. because it is a Class 1 only PSE).

The situation has now changed:

- Classification is mandatory
- The concept of Classes is much more prevalent in the standard
- The Ethernet Alliance logo program uses Class in the logo to make it clear what kind of PSE is needed to power a particular PD

There are valid use-cases for Class 1 and Class 2 only PSE ports, for which it is currently unclear if these are compliant or not.

Per the same logic, Type 4 PSEs should then be allowed to support only Class 7.

SuggestedRemedy

Change Table 145-16, Item 13:

- minimum value of Type 3 from 15.4 to 4
- minimum value of Type 4 from 90 to 75

Proposed Response Response Status W

TFTD

Cl 145 SC 145.2.8.1 P 155 L 37 # i-294
 Stover, David Analog Devices Inc.

Comment Type T Comment Status D PSE Power

"The voltage transients as a result of load changes up to 35mA/us shall be limited to 3.5V/us". This PSE requirement seems to be the dual of the PD transient behavior requirement (145.2.8.1). In another comment, I show that slew rate (TR3, Source dv/dt) should be 3500 V/s. This PSE requirement should likely reflect that change.

SuggestedRemedy

Replace "3.5 V/us" with "3500 V/s".

Proposed Response Response Status Z

PROPOSED REJECT.

This comment was WITHDRAWN by the commenter.

TFTD

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.8.3 P 156 L 3 # i-99
 Yseboodt, Lennart Philips Lighting

Comment Type T Comment Status X PSE Power

KTran_lo, the minimum peak PSE voltages for Type 3, Class 6 and Type 4, Class 8 are 46.2 V and 48.05 V respectively.
 If these values are used to calculate VTran_lo-2p in the PD under worst case circumstances, the calculated PD voltages are 37.2V and 34.5V.
 This mismatches with the VTran_lo-2P specification in Table 145-28 which is 36V.

Proposed is to change the KTran_lo spec to something that results in 36V on the PD side. Otherwise we might get into Von/Voff PD issues.

Quoted text should follow this proposal.
 "A PSE shall maintain an output voltage no less than KTran_lo below VPort_PSE-2P min for transient conditions lasting more than 30 us and less than 250 us, and meet the requirements of 145.2.8.8. Transients less than 30 us in duration may cause the voltage at the PI to fall more than KTran_lo."

SuggestedRemedy

We can rename KTran_lo to VTran-2P, it is obvious it is the low transient voltage, because a minimum is specified.

Change item 3 in Table 145-16 from KTran_lo to VTran-2P.
 VTran-2P for Type3 is 45.3V (MIN)
 VTran-2P for Type4 is 49V (MIN)
 Change 'parameter' to read: "Output voltage during transient".

Change text in 145.2.8.3 to:
 "A PSE shall maintain an output voltage no less than VTran-2P for transient conditions lasting more than 30 us and less than 250 us, and meet the requirements of 145.2.8.8. Transients less than 30 us in duration may cause the voltage at the PI to fall below VTran-2P."

Change parameter name in Table 145-28, item 2 from VTran_lo-2P to VTran_PD-2P.

Proposed Response Response Status W

TFTD

Cl 145 SC 145.2.8.3 P 156 L 8 # i-337
 Lemahieu, Joris ON Semiconductor

Comment Type TR Comment Status X PSE Power

Input Voltage drop to 0V is excessive.

Drop to 0V during 30us spec seems to be written for (theoretical) diode bridge at PD input. Have diode reverse recovery and cable inductance effects (peak reverse recovery current) been taken into account here?

Active bridges seem very popular in 802.3bt PD solutions to reduce dissipation in the input rectifier stage.
 An immediate short at the input would significantly discharge Cport as it takes time to turn off the mosfet.

SuggestedRemedy

Increase minimum voltage level during first 30us and make spec compliant with active bridges at the PD input.

Proposed Response Response Status W

TFTD

Cl 145 SC 145.2.8.3 P 156 L 8 # i-248
 Picard, Jean Texas Instruments Inc

Comment Type TR Comment Status X PSE Power

The following sentence does not make sense. In reality the PSE cannot really short the PI voltage, all it can do is temporarily turn off its port (it's only a low side switch after all, with a 0.1uF cap).

"The minimum PD input capacitance CPort min or CPort-2P min defined in Table 145-28, allows a PD to operate for input voltage transients which cause VPD to drop as low as 0 V, lasting less than 30 us as specified in 145.3.8.6."

SuggestedRemedy

Use similar wording to the "at" standard, removing "which cause VPD to drop as low as 0 V".

The wording becomes this:

"The minimum PD input capacitance CPort min or CPort-2P min defined in Table 145-28, allows a PD to operate for input voltage transients lasting less than 30 us as specified in 145.3.8.6"

Proposed Response Response Status W

TFTD

TFTD YD

This is at the PD PI not at the PSE PI. At the PD the voltage can get to 0 or negative due to voltage changes in the PSE. You have LCR circuit on the way from PSE to PD. This was meant to protect ideal diode bridges.

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.8.4 P 156 L 18 # i-100
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status D PSE Power

TOPIC: and/or
 The Chicago Manual of Style says the following about the use of 'and/or':
 "Avoid this Janus-faced term. It can often be replaced by 'and' or 'or' with no loss in meaning.
 Where it seems needed, try 'or ... or both'. But also think of other possibilities."

 "V Noise , the specification for power feeding ripple and noise in Table 145-16, shall be met for common-mode and/or pair-to-pair noise values for power outputs from (I Hold max x V Port_PSE-2P min) to the maximum power per the PSE's assigned Class for PSEs at static operating V Port_PSE-2P."

The use of and/or in this sentence is particularly bad as it allow TWO interpretations of the shall.
 ALSO - we are using a lot of words to redundantly indicate this shall applies at any power level.

SuggestedRemedy

"V Noise , the specification for power feeding ripple and noise in Table 145-16, shall be met for common-mode and pair-to-pair noise values at static PSE output voltage."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

"V Noise, the specification for power feeding ripple and noise in Table 145-16, shall be met for common-mode and pair-to-pair noise values at all static PSE output voltages."

TFTD DS

TFTD. Proposed remedy now applies below the original minimum power output (I_Hold,max * V_Port_PSE-2P,min). Are we OK with this?

Cl 145 SC 145.2.8.5 P 156 L 37 # i-373
 Thompson, Geoffrey Individual

Comment Type E Comment Status X PSE Power

It is a fine point but lport is defined on the basis of the cabling, but a "port" is a feature of equipment, not cabling. Therefore the definition should be "lport is the total current sourced by a PSE or sunk by a PD."

SuggestedRemedy

Change text per comment.

Proposed Response Response Status W

TFTD

Cl 145 SC 145.2.8.5 P 156 L 51 # i-204
 Peker, Arkadiy Microsemi Corporation

Comment Type TR Comment Status X Pres: Darshan9

"Equation 145-8 contains the parts that allow us to calculate the value of Icon-2P in case of operating over 2-pairs and for the dual-signature case.
 However, for the most important use case which is operating over 4-pairs.
 Equation 145-8 contains the part "ICon-2P=min(Icon - IPort-2P-other, ICon-2P-unb) when operating over 4-pairs.
 -ICon is defined in Equation 145-9.
 -ICon-2P_unb is defined in Table 145-16 item 5.
 There is no information to find the value of ICon-2P_other in order to calculate the value of ICon-2P. As a result, the spec is broken."

SuggestedRemedy

Adopt darshan_09_0917.pdf

Proposed Response Response Status W

TFTD

WFP

Cl 145 SC 145.2.8.5 P 157 L 13 # i-101
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status X Pres: Yseboodt3

"A minimum current of I Con-2P-unb over one of the pairs of the same polarity under maximum unbalance condition (see 145.2.8.5.1) in the POWER_ON state."

The unbalance specification is tied together by ICon-2P-unb which serves 3 distinct roles:
 - It is the minimum current a PSE must be able to supply on a pairset
 - It is the maximum current a PSE may source when connected to a worst-case unbalance cable + PD
 - It is the maximum current a PD may draw when connected to a worst-case unbalance cable + PSE

That makes it that there is ZERO margin between PSE minimum and PD maximum.

SuggestedRemedy

Adopt yseboodt_03_0917_unbalancemargin.pdf which aims to create margin by introducing a new parameter that takes the role of specifying the minimum current a PSE must support on a pairset.

Proposed Response Response Status W

TFTD

WFP

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Cl 145 SC 145.2.8.5 P 157 L 14 # i-102
 Yseboodt, Lennart Philips Lighting

Comment Type E Comment Status D Repeats

"A minimum current of ICon-2P-unb over one of the pairs of the same polarity under maximum unbalance condition (see 145.2.8.5.1) in the POWER_ON state."
 When a state name is mentioned do not use the word "state".

SuggestedRemedy

"A minimum current of ICon-2P-unb over one of the pairs of the same polarity under maximum unbalance condition (see 145.2.8.5.1) in POWER_ON."

Proposed Response Response Status W

PROPOSED REJECT.

Repeat of 103

TFTD CJ
 technically, we have to accept and give the same remedy as 103...

Response DNA: I was hoping Lennart would withdraw

Cl 145 SC 145.2.8.5 P 158 L 10 # i-104
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status D Pres: Darshan15

"I Peak-2P-unb , defined in Equation (145-12), is the minimum current due to unbalance effects that a PSE supports on a pairset when powering a single-signature PD over 4 pairs."

What follows is a set of equations that define the value of IPeak-2P-unb as function of IPeak (which in turns depends on VPSE and RChan) and RChan-2P.

See: http://www.ieee802.org/3/bt/public/mar17/yseboodt_02_0317_ipeak2punb.pdf
 The value of IPeak-2P-unb is often lower than that of ICon-2P-unb. The PSE needs to support ICon-2P-unb, so this has the effect of 'clipping' IPeak-2P-unb to be at least ICon-2P-unb.

The real issue arises in the PD section, where we require a PD never to draw more than IPeak-2P-unb on any given pair.
 If that is a requirement (and it should be), then we can't have IPeak-2P-unb depend on VPSE and RChan, both parameters the PD knows nothing about.

Given that there is almost no gain for PSEs to be had from being able to tune IPeak-2P-unb, the most effective solution is to make IPeak-2P-unb a fixed number.

SuggestedRemedy

- Replace page 158, lines 12 through 44 by:

$$IPeak-2P-unb = \{ILIM-2P - 0.002$$

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Lennart, did this comment get imported correctly?

TFTD LY
 I forgot I'm not allowed to use "fg" in my comment text. The last line should be:
 $IPeak-2P-unb = \{ILIM-2P - 0.002\}A$

TFTD YD
 See darshan_15_0917.pdf.

WFP

TFTD CJ
 I will only agree to this comment if we get agreement that the way to test this parameter is to place a worst case PD unbalance circuit and not some current sink that checks for the actual current. The PD has to adhere to limits based on connection to a worst case PSE circuit, the PSE should be treated the same. It's great to have the numbers in the spec and those that don't deeply understand will design to those limits. But those that understand the way a system really works should be able to exploit that to their benefit and not fail only

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when tested by some non-PD circuit.

Cl 145 SC 145.2.8.5.1 P 158 L 45 # i-424

Darshan, Yair

Comment Type T Comment Status X Pres: Darshan3

Icn-2P_unb values need to be verified when using Equation 145-15 (Rpse_min/max) and Equation 145-26 (Rpd_min/max) with the test verification models described in Table 145-17 and Rsource_min/max requirements with their defined accuracies (+1/-%).

SuggestedRemedy

Adopt darshan_03_0917.pdf

Proposed Response Response Status W

TFTD

WFP

Cl 145 SC 145.2.8.5.1 P 158 L 46 # i-425

Darshan, Yair

Comment Type T Comment Status D Pres: Darshan1

The changes we did when we move from "channel" to "Link section" breaks some of the work we did for pair to pair resistance unbalance. To fix it, we need to add a text that defines the equipment connector as part of the PSE PI and PD PI when tested for pair-to-pair resistance unbalance for compliance. In this way we don't break the link section definition due to the fact that the PSE load when PSE is tested for compliance and PD voltage source output resistance, Rsource, when PD is tested for compliance include the effect of the equivalent portion of the link section.

SuggestedRemedy

Adopt darshan_01_0917.pdf for detailed analysis and proposed baseline.

Proposed Response Response Status W

TFTD

WFP

Cl 145 SC 145.2.8.5.1 P 158 L 47 # i-392

Thompson, Geoffrey

Individual

Comment Type ER Comment Status X Unbalance

This seems like an attempt to control the system imbalance (which is controlled by the combined specifications of the three elements, one of which is externally specified) from within the PSE spec.

SuggestedRemedy

This is all valuable tutorial material that would be valuable for further work on the topic so it should be moved (with suitable editing) to an informative annex.

Proposed Response Response Status W

TFTD

TFTD YD

"Reject this comment due to the following:1. No clear remedy what do.

2. No clear instructions what should stay and what should move to annex3. We already been in Spec, Move to Annex, Back to spec several times with many comments until it was clear that what we have now is important to have in the standard and not in the annex."

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CI 145 SC 145.2.8.5.1 P 159 L 27 # i-426

Darshan, Yair

Comment Type T Comment Status D Pres: Darshan2

This comment is not about active current balancing. This comment is about the typical use of PSE resistive elements to form Rpse_min and Rpse_max that meet equation 145-15 and when PSE connected to the PSE load specified in Table 145-17, will meet the values Icon-2P_unb in Table 145-16.

In D3.0, the maximum value of Rpse_min is not limited. Rpse_max is function of Rpse_min. If Rpse_min maximum value is not limited, it will cause the following issues:

- (a) The internal PSE power supply open load voltage to significantly increase in order to keep the PSE voltage at the PI 50V min or 52V min pending the PSE Type under load. This will result with working outside the PSE operating voltage range.
 - (b) power loss at extreme values of Rpse_min which doesn't make sense.
 - (c) Per Equation 145-15, if Rpse_min is increased, Rpse_max is increased and at higher values of Rpse_min (starting at 0.5 ohms at Class 7-8 and 1 ohm at class 5-6), the contribution of Rpse to unbalance compared to the channel and PD, resulting with the increase of system unbalance at long cable which violates Icon-2P_unb when tested with test verification model in Table 145-17.
 - (d) there is no practical benefit to increase Rpse_min to any value.
 - (e) The above is not relevant to active current balancing.
- See calculation results in darshan_02_0917.pdf.

SuggestedRemedy

(See calculation results in darshan_02_0917.pdf.)

Change from: "RPSE_min is the lower PSE common mode effective resistance in the powered pairs of the same polarity."

To: "RPSE_min is the lower PSE common mode effective resistance in the powered pairs of the same polarity. The value of Rpse_min shall be limited to:

- a) 1 ohms for class 5 and 6
- b) 0.5 ohm for class 7 and 8.

The value of Rpse_min is not limited when active current balancing is used.

Proposed Response Response Status W

PROPOSED REJECT.

TFTD

WFP

There is no reason to specify this. Reasons a, b, d, and e listed in the comment are not reasons to specify something, they are reasons for people not to make a product with high values of RPSE_min. Reason C (and A) points out that if they try to use a value that is too high, they will fail other specs.

TFTD LY

Fully agree this cannot be a 'shall', but we do have to specify over what range the RPSE equation produces valid results.

TFTD YD

"The main reason that we need to do it is that Equation 145-15 ACCURACY depends on the range of Rpse_min (the arguments used in the comment was the source of the inaccuracies). In other words: Typically, equation, any equation, has a range when it is valid. When the range is minus infity to plus infinity it means that it always correct. Since this equation done based on linear curve fitting, its range of existance is depened on limited value range of its subject parameter, Rpse_min, in this case. As a result, Rpse_min maximum value has to be limited. Change the proposed remedy to: After line 28, add the following text: ""Equation 145-15 is valid for R_pse_min up to a value of 1 ohm for Class 5 and Class 6, and 0.5 ohm for Class7 and Class 8.""

CI 145 SC 145.2.8.5.1 P 159 L 34 # i-107

Yseboodt, Lennart

Philips Lighting

Comment Type TR Comment Status D Unbalance

"A PSE shall not source more than I Con-2P-unb min on any pair when connected to a load as shown in Figure 145-22, using values of R load_min and R load_max as defined in Equation (145-16) and Equation (145-17)."

- ICon-2P-unb is a minimum, no need to specify I Con-2P-unb min
- We should make it obvious that this shall applies when connected to a given test fixture described in the next paragraphs.

SuggestedRemedy

Change quoted text to:

"A PSE shall not source more than I Con-2P-unb on any pair when connected to a test fixture described in Figure 145-22, using values of R load_min and R load_max as defined in Equation (145-16) and Equation (145-17)."

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD

See 427

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Cl 145 SC 145.2.8.5.1 P 159 L 34 # i-427
 Darshan, Yair

Comment Type T Comment Status X Unbalance

In the text below:
 "A PSE shall not source more than ICon-2P-unb min on any pair when connected to a
 load as shown in Figure 145-22, using values of Rload_min and Rload_max as
 specified in Equation (145-16) and Equation (145-17).", Need to be "PSE load" as in Figure
 145-22.

SuggestedRemedy

Change text to "A PSE shall not source more than ICon-2P-unb min on any pair when
 connected to the PSE load as shown in Figure 145-22, using values of Rload_min and
 Rload_max as specified in Equation (145-16) and Equation (145-17)."

Proposed Response Response Status W

TFTD

See 107

TFTD YD

Should be OBE by 107 since "PSE load" is implied in the "test fixture" that Lennart is using
 in his proposed remedy

Cl 145 SC 145.2.8.5.1 P 160 L 1 # i-108
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status X Pres: Darshan3

Table 145-17 contains the values needed to determine Rload, which is the load with which
 PSE unbalance is checked.
 Calculations show that when plugging in these numbers, some of the Classes fail to meet
 ICon-2P-unb.
 Eg, with an RPSE_min=0.3 ICon-2P-unb for Class 7 (low channel conditions) is not met:

Class 7, low channel conditions, ipt=1.195 i=0.784/0.412/0.784/0.412, VSupply=52.370
 VPSEPI=52.003
 RPSE_min = 0.250 and RPSE_max = 0.446
 PPD = 62.0, VLoad = 51.08, Vpd[1-4] = 52.11 52.14 0.26 0.23 = 51.92
 FAILS to meet ICon-2P-unb of 0.781

Other values of RPSE cause more errors, but all in Class 7.

SuggestedRemedy

Either we need to update ICon-2P-unb, or we need to update the values in Table 145-17.
 Input Yair is needed.

Proposed Response Response Status W

TFTD

WFP

TFTD YD

The problem was resolved by accepting comment i-420. See full update for ICon-2P_unb
 for all classes in darshan_03_0917.pdf for comment 419. In fact, make 420 and 108, OBE
 to 419. It will save time.

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Cl 145 SC 145.2.8.5.1 P 160 L 39 # i-428
 Darshan, Yair

Comment Type T Comment Status X Unbalance

This comment will be OBE by comment marked LOWER02 if LOWER02 will be accepted.
 In the text "ICon-2P-unb and Equation (145-15) are specified for total channel common mode pair resistance RChan-2P" the word "total" is not required. Remove it.

SuggestedRemedy

Change from "ICon-2P-unb and Equation (145-15) are specified for total channel common mode pair resistance RChan-2P" the word "total" is not required."

To: "ICon-2P-unb and Equation (145-15) are specified for channel common mode pair resistance RChan-2P" the word "total" is not required."

Proposed Response Response Status W

TFTD

See 422, 109

TFTD YD

Should be OBE to 422 if 422 will be accepted.

Cl 145 SC 145.2.8.5.1 P 160 L 39 # i-422
 Darshan, Yair

Comment Type T Comment Status X Unbalance

This comment is marked as LOWER02.

In the following text:

"ICon-2P-unb and Equation (145-15) are specified for total channel common mode pair resistance RChan-2P from 0.2 ? to 12.5 ? and worst-case unbalance contribution by a PD. PSEs that support channel common mode resistance less than 0.2 ?, or if RChan is less than 0.1 ?, the PSE should meet ICon-2P-unb requirements when connected to (Rload_min - 0.5 * RChan-2P) and (Rload_max - 0.5 * RChan-2P). This can be achieved by using a lower RPSE_max or higher RPSE_min than required by Equation (145-15). Lower RPSE_max values may be obtained by using smaller constant ? or higher RPSE_min in Equation (145-15) in the form of $RPSE_{max} = ? * RPSE_{min} + ?$."

The following may be improved:

1. The "total" is not required.
2. To simplify and clarify the text that explains what to do when shorter cabling than 0.2 ohm is used
3. To simplify the use of " $RPSE_{max} = ? * RPSE_{min} + ?$ "

SuggestedRemedy

Replaced the called out text with:

"The values for ICon-2P-unb and the relationship between RPSE_max and RPSE_min (Equation (145-15)) are valid given that RChan-2P (see 145.1.3) ranges from 0.2 ? to 12.5 ? and that the PD meets 145.3.8.10. In cases where RChan-2P is less than 0.2 ?, or RChan is less than 0.1 ?, PSE compliance with ICon-2P-unb can be evaluated using Rload_min and Rload_max both reduced by 0.5 * RChan-2P. This compliance will require a reduction in the ratio of RPSE_max to RPSE_min presented by Equation (145-15)."

Proposed Response Response Status W

TFTD

See 428, 109

TFTD YD

This text was discussed with Ken, Pete and Yair and agreed as better than the current text

TFTD DS

The reference text calls into question the accuracy of the PSE unbalance test as a de-facto guarantee that PSEs will provide interoperability, which must not be the case. Furthermore, the referenced text adds uncertainty for all PSE designers by suggesting a stricter set of PSE requirements might apply to them; in actuality, this refers to an application-specific case with extremely low resistance connections between PSE and PD.

Propose this paragraph be deleted or moved to Annex 145A.

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Cl 145 SC 145.2.8.5.1 P 160 L 45 # i-109
 Yseboodt, Lennart Philips Lighting

Comment Type T Comment Status X Unbalance

"This can be achieved by using a lower R PSE_max or higher R PSE_min than required by Equation (145-15). Lower R PSE_max values may be obtained by using smaller constant a or higher R PSE_min in Equation (145-15) in the form of $R PSE_{max} = a \times R PSE_{min} + b$."

Very long/complicated way to say that it can be achieved by decreasing the difference between Rpsemin and Rpsemax.

SuggestedRemedy

Change to:
 "This can be achieved by decreasing the difference between R_PSE_min and R_PSE_max as defined in Equation 145-15."

Proposed Response Response Status W

TFTD

See 422, 428

TFTD YD
 The proposed remedy cant be accepted as is. This is not just to decrease the difference it also touches the absolute values of Rpse_min/max. Instead, adopt 422 which is technically correct and clearer.

TFTD DS
 The reference text calls into question the accuracy of the PSE unbalance test as a de-facto guarantee that PSEs will provide interoperability, which must not be the case. Furthermore, the referenced text adds uncertainty for all PSE designers by suggesting a stricter set of PSE requirements might apply to them; in actuality, this refers to an application-specific case with extremely low resistance connections between PSE and PD.
 Propose this paragraph be deleted or moved to Annex 145A.

Cl 145 SC 145.2.8.5.1 P 161 L 1 # i-110
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status X Pres: Yseboodt2

Comparing Figure 145-22 with it's PD counterpart (Fig. 145-31), it contains a large amount of detail which is not relevant to the evaluation of Icon-2P-unb.

SuggestedRemedy

Adopt yseboodt_02_0917_Figure_145_22.pdf

Proposed Response Response Status W

TFTD

WFP

See 393

Cl 145 SC 145.2.8.5.1 P 161 L 2 # i-393
 Thompson, Geoffrey Individual

Comment Type ER Comment Status X Pres: Yseboodt2

Figure 145-22. This figure is very valuable in understanding the overall problem of resistance imbalance in a PoE system, however it doesn't help with the problem of designing a PSE when one has no control of the link section or the PD.

SuggestedRemedy

Tutorial material that would be valuable for further work on the topic. It should be moved to an informative annex.

Proposed Response Response Status W

TFTD

See 110

TFTD YD
 "Reject this comment due to the following:
 1. Figure 145-22 is needed for the spec. No clear remedy what to do instead.
 2. No clear instructions what should stay and what should move to the informative annex
 3. We already been in Spec, Move to Annex, Back to spec several times with many comments until it was clear that what we have now is important to have in the standard and not in the annex."

TFTD DS

The normative statement in this section is tied to Figure 145-22; equations 145-16, 145-17. These items should likely stay in the section.

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CI 145 SC 145.2.8.5.1 P 161 L 6 # i-111
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status D Editorial

Figures 145-22, Figure 145-31, Figure 145A-2, and Figure 145A-3 all depict some view on unbalance. A different notation for the names of the current is used in each.

SuggestedRemedy

Change Figures 145-22, Figure 145-31, Figure 145A-2, and Figure 145A-3 such that:

- Currents are named "i1" through "i4".
- i1 and i2 flow to the PD (positive)
- i3 and i4 flow from the PD (negative)
- where applicable, i1 and i3 represent Alt A / Mode A
- where applicable, i2 and i4 represent Alt B / Mode B

Update text that refers to Figure labelled currents to match.

Proposed Response Response Status W

PROPOSED ACCEPT.

Editorial license granted to adjust for changes to any of the figures made as a result of other comments.

TFTD YD

I am OK with remedy. I don't agree for the "Editorial licence to adjust for changes for any figures made as a result of other comment." This is too broad and whenever I agreed, I was sorry. Just correct things per specific comments so we will have control on the changes. The editor is not familiar with the reasoning for details in the drawings.

Response DNA: The editorial license is given to make sure we don't have conflicting comment responses.

CI 145 SC 145.2.8.5.2 P 161 L 18 # i-434
 Darshan, Yair

Comment Type E Comment Status X Unbalance

In the bottom of Figure 145-22, there is an arrow with a text "End-to-end pair-to-pair resistance".

This text need to be accurate and reflect the following:

- a) It is End-to-end pair to pair effective resistance and not just resistance.
- b) It is the boundaries of where the system unbalance is defined. This helps to understand the boundaries of the PSE PI to the PSE power supply elements that affect the unbalance and the same for the PD and the link segment.
- c) The term End to End effective resistance unbalance is describe in 145.2.8.5.1 e.g. P.158 L48 and many other places in the spec.

SuggestedRemedy

Change from "End-to-end pair-to-pair resistance"

To: "End-to-end pair-to-pair effective resistance unbalance boundaries"

Proposed Response Response Status W

TFTD

These terms are becoming very confusing and need simplifying.

CI 145 SC 145.2.8.5.1 P 161 L 20 # i-429
 Darshan, Yair

Comment Type E Comment Status X Pres: Yseboodt2

The title of figure 145-22 is good but not sufficiently accurate. It is system effective resistance unbalance and not just system resistance unbalance. This is in sync with the title of the clause "145.2.8.5.1 PSE PI pair-to-pair effective resistance and current unbalance" and the text all over clause 145.2.8.5.1 and 145.3.8.10 (44 occurrences).

SuggestedRemedy

Change from Figure 145-22--PSE PI unbalance specification and system resistance unbalance"

To: "Figure 145-22--PSE PI unbalance specification and system effective resistance unbalance"

Proposed Response Response Status W

TFTD

TFTD LY

OBE to yseboodt 02 (do not adopt both, creates conflict)

WFP

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Cl 145 SC 145.2.8.5.1 P 161 L 26 # i-112
 Yseboodt, Lennart Philips Lighting

Comment Type **TR** Comment Status **X** Pres: Yseboodt2

In the evaluation method for Figure 145-22, item b) says:
 "With the PSE powered on, adjust the load to P Class_PD ."

Which is wrong since the PSE load also comprises of the R_Ch_unb resistors.

SuggestedRemedy

Replace by:
 "Adjust to load such that a power of PClass-PD is consumed at the PD PI."

Note: text may need adjustment based on yseboodt_02_0917_Figure_145_22.pdf

Proposed Response Response Status **W**

TFTD

WFP

Cl 145 SC 145.2.8.5.2 P 161 L 26 # i-431
 Darshan, Yair

Comment Type **E** Comment Status **D** Pres: Yseboodt2

In the text "With the PSE powered on, adjust the load to PClass_PD.", missing "at the PD PI"

SuggestedRemedy

Change to: "With the PSE powered on, adjust the PSE load to PClass_PD at the PD PI."

Proposed Response Response Status **W**

TFTD

This instruction doesn't make sense. The PSE Load is the entire box in Figure 145-22. What are they supposed to adjust? I assume this really means to adjust the current draw in the small box that says "adjust" in it. We need to make this more clear.

See 431

WFP

TFTD YD

"1." See 431""? This is 431.

2. I agree the remedy is not clear. Change the remedy to: ""Adjust to load such that a power of Pclass-PD is consumed at the PD PI."". See i-112."

Cl 145 SC 145.2.8.5.1 P 161 L 28 # i-113
 Yseboodt, Lennart Philips Lighting

Comment Type **T** Comment Status **D** Unbalance

In the evaluation method for Figure 145-22, step 'e' (check the current), comes after the Rload_min/max exchange.

SuggestedRemedy

Swap steps d) and e) and adjust labels accordingly.

Proposed Response Response Status **W**

PROPOSED ACCEPT.

TFTD YD

The remedy is incorrect. The order of d and e are correct

Cl 145 SC 145.2.8.5.1 P 161 L 40 # i-114
 Yseboodt, Lennart Philips Lighting

Comment Type **ER** Comment Status **D** Editorial

It is unclear from Table 145-17 and Figure 145-22, that they describe a test fixture to test PSE unbalance.

Another comment improves Figure 145-22, however the title of Table 145-17 should make very clear we're describing components of a test fixture, not PD specification.

SuggestedRemedy

Change title of 145-17 to read: "PSE unbalance test fixture resistances".

Proposed Response Response Status **W**

PROPOSED ACCEPT IN PRINCIPLE.

Change title of 145-17 to read: "PSE unbalance test fixture resistances" on page 161 (comment says page 160).

TFTD YD

it should be: Change title of *Table* 145-17 to read: "PSE unbalance test fixture resistances". The page is correct. The commenter address the table and not the Figure

Response DNA: Proper response: Change title of Table 145-17 to read: "PSE unbalance test fixture resistances".

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Cl 145 SC 145.2.8.6 P 161 L 45 # i-116
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status D PSE Inrush

"The PSE shall limit I Inrush-2P and I Inrush during POWER_UP per the requirements of Table 145-16."

Nowhere in this subclause do we explain what these parameters are and how they relate to each other.

SuggestedRemedy

Insert the following text after the paragraph containing the quoted text:
 "Inrush-2P is the current to which the PSE limits it's pairset output current while in POWER_UP. Inrush is the total current to which the PSE limits it's output current while in POWER_UP. When connected to a single-signature PD, Inrush is the total inrush current limit, and Inrush-2P serves as the limit for 2-pair inrush, or as the inrush unbalance limit during 4-pair inrush.
 When connected to a dual-signature PD, only Inrush-2P is specified and serves as the inrush limit for each pairset independently."

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD. Need to make sure DS lines get deleted for linrush for this text to be accurate.

TFTD YD

The text is correct without deleting the lines suggested by Lennart in other comment. I disagree with deleting DS lines in item 6 Table 145-16 since there is a reason for it (limits the maximum current to 0.9A instead of 1.2A.)

Cl 145 SC 145.2.8.6 P 162 L 1 # i-301
 Stover, David Analog Devices Inc.

Comment Type T Comment Status X PSE Inrush

Figure 145-23 specifies the PSE inrush upperbound template; requirements for both Iport-2P and Iport as shown apply simultaneously. In Figure 145-23, Iport is limited to linrush,max while Iport-2P may load step up to 50A (>>linrush,max). As drawn, Iport-2p is limited to the lesser of these requirements: IInrush,max.

SuggestedRemedy

Remove IPort axis from Figure 145-23 or specify IPort behavior during load step.

Proposed Response Response Status W

TFTD

I don't follow your interpretation of the drawing.

TFTD DS

What is the upper bound of IPort during the 50A IPort-2P load step event? Figure 145-23 shows an 'exception' to the IPort-2P requirement without guidance on IPort requirements during this event.

Cl 145 SC 145.2.8.5.3 P 162 L 10 # i-433
 Darshan, Yair

Comment Type T Comment Status X Pres: Darshan10

The shape of the load need to be circle and not rectangular since it is constant power sink. All our spec is based on the fact that the PD load is constant power sink

SuggestedRemedy

Adopt the changes proposed in darshan_10_0917.pdf marked in BLUE.

Proposed Response Response Status W

TFTD

WFP

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Cl 145 SC 145.2.8.6 P 162 L 28 # i-118
 Yseboodt, Lennart Philips Lighting

Comment Type ER Comment Status D PSE Inrush

"The minimum value of I Inrush-2P includes the effect of end to end pair to pair resistance unbalance when operating over 4 pairs."

Seems like a leftover sentence from earlier inrush specification. There are only min values defined (for IInrush-2P) for dual-signature, where unbalance does not play a role.

SuggestedRemedy

Remove sentence.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD YD

No. It includes unbalance effect. Dual-signature does have unbalance but we overcome it in other ways. It doesn't change the fact that Inrush in dual signature will be split to two different currents one is lower and the other higher due to unbalance when the dual-signature use single load.!. We adressed unbalance in power on by requesting that each pair set will consume power up to Pclass_PD so the burden remains in the PD.

Cl 145 SC 145.2.8.6 P 162 L 32 # i-119
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status X PSE Inrush

"The minimum inrush requirement is a function of the pairset voltage and is as follows:

- a) During POWER_UP, for pairset voltages between 0 V and 10 V, the minimum I Inrush-2P requirement is 5 mA.
- b) During POWER_UP, for pairset voltages between 10 V and 30 V, the minimum I Inrush-2P requirement is 60 mA.
- c) During POWER_UP for pairset voltages above 30 V, the minimum I Inrush-2P and I Inrush requirement are as defined in Table 145-16."

I guess what we want to say is that these minimum capabilities apply for each powered pairset in POWER_UP.

SuggestedRemedy

Replace quoted text by:

"The minimum linrush and IInrush-2P current capability as defined in Table 145-16 applies when VPSE exceeds 30V.
 During POWER_UP, the minimum supported current on each powered pairset is:
 - 5mA when 0V < VPSE <= 10V
 - 60mA when 10V < VPSE <= 30V"

Proposed Response Response Status W

TFTD

How can this be both the linrush and linrush-2P minimum? The original sentence quotes pairset voltage and thus implies this is per pairset...

See 486

TFTD LY

The sentence: "The minimum linrush and IInrush-2P current capability as defined in Table 145-16 applies when VPSE exceeds 30V." applies only to what is in the Table. What is below isn't either IInrush or linrush-2P but is described separately.

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.8.6 P 162 L 33 # i-486

Johnson, Peter

Comment Type T Comment Status X PSE Inrush

(Re-filed comment from D 2.4) There is an inconsistency in the three minimum inrush current requirements a), b), and c) and Table 145-16. Conditions a) and b) specify "minimum Inrush-2P" requirements with actual values while Table 145-16 is blank for minimum Inrush-2P given Single Signature PD. Are these figures really applicable to Inrush-2P or are they applicable to Inrush? Item c) says refer to Table 145-16 for minimum Inrush-2P, but again, those boxes are blank for Single Signature.

SuggestedRemedy

Following modification has implementation implications but could resolve the confusion:

- a) ...voltages between 0 V and 10 V, the minimum I_Inrush when powering a Single Signature PD and the minimum I_Inrush-2P when powering a Dual Signature PD shall be 5 mA.
- b) ... voltages between 10 V and 30 V, the minimum I_Inrush when powering a Single Signature PD and the minimum I_Inrush-2P when powering a Dual Signature PD shall be 60 mA.
- c) ... voltages above 30 V, the minimum I_Inrush when powering a Single Signature PD and the minimum I_Inrush and I_Inrush-2P when powering a Dual Signature PD are specified in Table 145-16.

Proposed Response Response Status W

TFTD

See 119

Cl 145 SC 145.2.8.7 P 162 L 43 # i-120

Yseboodt, Lennart

Philips Lighting

Comment Type ER Comment Status D Sliding

Topic:SLIDING

Issue: we use the concept of 'sliding windows' in our draft very inconsistently, the SLIDING comments try to make the whole bunch consistent.

Aim: get everything in the form "measure xxx using a xx time sliding window".

"The cumulative duration of T CUT-2P is measured with a sliding window of at least 1 second width."

This one is pretty OK, minor harmonization needed (measured with => measured using).

SuggestedRemedy

"The cumulative duration of T CUT-2P is measured using a sliding window of at least 1 second width."

Proposed Response Response Status W

TFTD

Does this sentence help the reader have any understanding of what this is getting at?

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

CI 145 SC 145.2.8.8 P 162 L 54 # i-121
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status X PSE Power

"When connected to a single-signature PD, the PSE should remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset."

Let's say we have a PD (Class 5-8) that is operating in 4-pair mode, something occurs on one pairset only and the PSE flips to 2-pair mode.
 Per Equation 145-8, the PSE is now required to support the full assigned power over 2-pairs. Not something we really want.

We can fix this by re-assigning the PD to Class 4 in case of a flip to 2-pair. That way we don't violate ICable by delivering more power over 2-pair.

SuggestedRemedy

- Add the following statement to SEMI_PWRON_PRI and SEMI_PWRON_SEC:
 "pse_allocated_pwr = min(pse_allocated_pwr, 4)"

Proposed Response Response Status W

TFTD

TFTD YD
 REJECT. Technically incorrect. We are not violating ICable at all. When Flipping to 2-pair, the pair is current protected and the current limit is set to the same value per pairset as it was over 4-pairs so nothing is changed.

CI 145 SC 145.2.8.8 P 164 L 32 # i-123
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status X Sliding

Topic:SLIDING
 Issue: we use the concept of 'sliding windows' in our draft very inconsistently, the SLIDING comments try to make the whole bunch consistent.
 Aim: get everything in the form "measure xxx using a xx time sliding window".

"The PSE shall limit a pairset current to I LIM-2P for a duration of up to T LIM-2P in order to account for PSE dV/dt transients at the pairset.
 The cumulative duration of T LIM-2P may be measured with a sliding window."

Oh joy, a sliding window without any limitation on the width.

SuggestedRemedy

Replace the last quoted sentence by:
 "The cumulative duration of T LIM-2P may be measured using sliding window of at least 1 second width."

Proposed Response Response Status W

TFTD

Does this sentence help the reader have any understanding of what this is getting at?

CI 145 SC 145.2.8.9 P 165 L 12 # i-126
 Yseboodt, Lennart Philips Lighting

Comment Type E Comment Status D PSE Power

"The specification for TOff in Table 145-16 shall apply to the discharge time from VPort_PSE-2P to VOff of a pairset with a test resistor of 320 kohm attached to that pairset."
 VPort_PSE-2P is a range. The actual starting value for Toff is given in the next sentence.

SuggestedRemedy

"The specification for TOff in Table 145-16 shall apply to the discharge time from operating voltage to VOff of a pairset with a test resistor of 320 kohm attached to that pairset."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Change to: "The specification for TOff in Table 145-16 shall apply to the discharge time from the operating voltage to VOff of a pairset with a test resistor of 320 kohm attached to that pairset."

TFTD HS

It is hard to test the time duration when it starts at "operating voltage". Perhaps VPort_PSE-2P min?

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.8.9 P 165 L 13 # i-127
 Yseboodt, Lennart Philips Lighting

Comment Type E Comment Status D Editorial

"In addition, it is recommended that the pairset be discharged when turned off."

In other places we refer to this as "power not applied" or "power removed".

SuggestedRemedy

"In addition, it is recommended that the pairset be discharged when power is removed."

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD DS

Per i-77, "the PSE does not apply power, it applies voltage and the PD draws current, causing power to be sourced."

Suggest the following remedy instead:

"In addition, it is recommended that the pairset be discharged when voltage is not applied".

Cl 145 SC 145.2.8.10 P 165 L 19 # i-128
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status D PSE Power

"The specification for V Off in Table 145-16 shall apply to the PI voltage in the IDLE State."

Slew of issues:

- 'IDLE' not 'IDLE State'.
- Doesn't take 4-pair / pairsets into account
- There are more states than IDLE where this applies

SuggestedRemedy

Replace by:

"The voltage at the PI shall be equal or less than V_Off, as defined in Table 145-16, when the PSE is in DISABLED, IDLE, TEST_ERROR_BOTH, ERROR_DELAY.

The voltage at the corresponding pairset shall be equal or less than V_Off, as defined in Table 145-16, when the PSE is in IDLE_PRI, WAIT_PRI, ERROR_DELAY_PRI, IDLE_SEC, WAIT_SEC, or ERROR_DELAY_SEC."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Replace by:

"The voltage at the PI shall be equal or less than V_Off, as defined in Table 145-16, when the PSE is in DISABLED, IDLE, TEST_ERROR_BOTH, or ERROR_DELAY.

The voltage at the corresponding pairset shall be equal or less than V_Off, as defined in Table 145-16, when the PSE is in IDLE_PRI, WAIT_PRI, ERROR_DELAY_PRI, IDLE_SEC, WAIT_SEC, or ERROR_DELAY_SEC."

TFTD DS

Missing some required states (e.g., Voltage at pairset Y shall be <= V_Off when in TEST_MODE_X). If we're referring to the PSE state diagram here, it would be more convenient to hook to "alt_pwr_x" rather than enumerating states.

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.8.12 P 165 L 33 # i-286
 Stewart, Heath Analog Devices Inc.

Comment Type T Comment Status D PSE Power

145.6.1 states "All equipment subject to this clause shall conform to IEC 60950-1 or IEC 62368-1. In particular, the PSE shall be classified as a Limited Power Source in accordance with IEC 60950-1 or IEC 62368-1 Annex Q."
 However elsewhere in 145, limited power source requirements are redundantly stated. For many reasons it is normal to avoid redundantly specifying requirements called out in referenced standards.

SuggestedRemedy

Remove subclause 145.2.8.12
 Page 163 Figure 145-25 remove lines related to I_LPS and P_Type,max/V_PSE.
 Upperbound template will thus have a value of 1.3A from 4s to infinity.
 Page 164 remove lines 21 and 29 (both reference I_LPS)
 Page 244 Line 17 Remove PSE82.

Proposed Response Response Status W

PROPOSED REJECT.

If we remove this section, the only requirements for max power would be in the "other" section of clause 145 that people tend to skip over (I know that they are wrong to do so, but they do). This will lead to "BT" devices on the market that violate LPS and hurt the PoE brand.

TFTD HS

PDs and PSEs are already "shall" required to conform to LPS standards.
 We should not create a second set of requirements that could potentially conflict with referenced standards. The reject did not address the comment.

TFTD DS

Disagree with the proposed response. Compliant devices shall conform to cited standards, regardless of location in Clause 145. The only thing in question with this comment is, does Clause 145 need to redundantly state the requirements from IEC-60950? I believe the answer is 'no'.

Cl 145 SC 145.2.8.12 P 165 L 37 # i-129
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status D Editorial

Topic:SLIDING
 Issue: we use the concept of 'sliding windows' in our draft very inconsistently, the SLIDING comments try to make the whole bunch consistent.
 Aim: get everything in the form "measure xxx using a xx time sliding window".

"Type 4 PSEs shall not source more power than P Type max as defined in Table 145-16 calculated with any sliding window with a width up to 4 seconds."

SuggestedRemedy

"Type 4 PSEs shall not source more power than P Type max as defined in Table 145-16 measured using a sliding window with a width up to 4 seconds."

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD

Wait for outcome of 286

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.2.8.13 P 166 L 6 # i-130
 Yseboodt, Lennart Philips Lighting

Comment Type E Comment Status D PSE Power

"PSEs, when connected to a single-signature PD, shall reach the POWER_ON state within Tpon after completing detection on the last pairset. When connected to a dual-signature PD, PSEs shall reach the POWER_ON state for a pairset within T pon after completing detection on the same pairset."
 Statename should not be using word "state".

SuggestedRemedy

Change to:
 "PSEs, when connected to a single-signature PD, shall reach POWER_ON within Tpon after completing detection on the last pairset. When connected to a dual-signature PD, PSEs shall reach POWER_ON for a pairset within Tpon after completing detection on the same pairset."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Change to:
 "PSEs, when connected to a single-signature PD, shall reach POWER_ON within Tpon after completing detection on the last pairset. When connected to a dual-signature PD, PSEs shall reach the respective power on state for a pairset within Tpon after completing detection on the same pairset."

TFTD HS

First "aftervcompleting" should be "after completing"
 Second, this brings up another deficiency in this text. A invalid detect can take up to 499ms. This creates the opportunity for a new PD to be inserted. I'm still working on a fix for this. Tpon should only be restarted based on completion of a _valid_ detection on either pairset. Tpon should be stopped when either pairset is in a power on state. A new _detection_ or power on on either pairset should not be started if tpon has expired.

TFTD CJ

there is a typo in the proposed response. 'after completing'

Cl 145 SC 145.3.2 P 168 L 31 # i-131
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status X Pres: Yseboodt1

This subclause deals with what kind of input power configurations a PD must be able to handle and operate under.
 It does not properly cover all of the compliant configurations a PSE can have.

SuggestedRemedy

Adopt yseboodt_01_0917_pdinpower.pdf

Proposed Response Response Status W

TFTD

WFP

Cl 145 SC 145.3.3.4 P 170 L 48 # i-136
 Yseboodt, Lennart Philips Lighting

Comment Type T Comment Status D PD SD

Variable pd_current_limit in the PD state diagram.
 The description of TRUE/FALSE says "The PD is (not) required to control the input current."

What this is really about is _limiting_ the input current.

SuggestedRemedy

Replace 'control' in the text with the TRUE/FALSE values by 'limit'.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD DS

Delete pd_current_limit. In all cases pd_current_limit is either redundant or misleading to pd_max_power usage:

In INRUSH:

pd_max_power <= inrush (no limit)

pd_current_limit <= false (no limit)

In POWER_DELAY:

pd_max_power <= min(3,pd_req_class)

pd_current_limit <= true (limit to I_Inrush_PD(-2P))

in POWERED:

pd_max_power <= min(pse_assigned_class, pd_req_class)

pd_current_limit <= false (no limit)

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.3.3.4 P 172 L 5 # i-137
 Yseboodt, Lennart Philips Lighting

Comment Type T Comment Status D PD SD

Variable present_det_sig:
 "Controls presenting the detection signature (see 145.3.4) by the PD.
 Values:
 invalid: A non-valid PD detection signature is to be applied to the PI.
 valid: A valid PD detection signature is to be applied to the PI over each pairset.
 either: Either a valid or non-valid PD detection signature may be applied to the PI."

Why does valid say 'over each pairset', but invalid does not ?

SuggestedRemedy

Given that this is single-signature, all of these should apply on both pairsets.
 Change to:
 "Controls presenting the detection signature (see 145.3.4) by the PD over each pairset.
 Values:
 invalid: A non-valid PD detection signature is to be applied to the PI.
 valid: A valid PD detection signature is to be applied to the PI.
 either: Either a valid or non-valid PD detection signature may be applied to the PI."

Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.

TFTD LY
 Comment is AIP with empty proposed response.

Response DNA: Yeah, I was trying to come up with better text and forgot to change it back to straight ACCEPT when I gave up.

TFTD YD
 "1. 'Invalid, valid and either is more stronger definition if it say explicitly ""per pairset and not at the PI. Using ""PI"" regarding detection may not be strong requirement. One might interprete that if I have valid sig on one of the pairset (a pairset is part of the PI) than it is done..2. In addition, it AIP but final response is missing."

TFTD DS
 This comment is "AIP" but no OBE or alternate remedy is included in the proposed response.

Cl 145 SC 145.3.3.7 P 174 L 1 # i-310
 Stover, David Analog Devices Inc.

Comment Type TR Comment Status D Pres: Stover1

pd_acs_req flag handling in "main" PD state machine has unintended behavior. For example, if pd_acs_req is set TRUE and PD is consequently reset prior to presenting Autoclass power, pd_acs_req will not be reset as FALSE.

SuggestedRemedy

See stover_01_0917.pdf

Proposed Response Response Status Z
 PROPOSED REJECT.

This comment was WITHDRAWN by the commenter.

TFTD

Cl 145 SC 145.3.3.7 P 174 L 23 # i-138
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status X Pres: Yseboodt7

The variable pd_acs_req indicates if a PD saw a long class event and must do Autoclass. This variable's description is very misleading in 145.3.3.4, moreover, we don't need it because we can use "long_class_event * pd_autoclass_enabled" to get the same effect.

I now also notice that Figure 145-27 doesn't work (eg. pd_acs_req is set to FALSE in IDLE_ACS, preventing it from being true in the arc from IDLE_ACS to WAIT_ACS).

SuggestedRemedy

Adopt yseboodt_07_0917_pdautoclassfix.pdf

Proposed Response Response Status W

TFTD

WFP

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.3.3.7 P 175 L 38 # i-326
 Abramson, David Texas Instruments Inc

Comment Type **TR** Comment Status **D** PD SD

The variable "nopower" should be set back to FALSE in the INRUSH state as the PD can transition back to INRUSH from NOPOWER.

SuggestedRemedy

Add "nopower <= FALSE" to INRUSH

Proposed Response Response Status **W**

PROPOSED ACCEPT.

TFTD LY

I am pretty sure that is NOT what you want. You will get the pleasure of rejecting one of your own comments now.

Response DNA: why?

TFTD HS

nopower is meant to be sticky until return to OFFLINE/IDLE.

Cl 145 SC 145.3.5 P 183 L 22 # i-143
 Yseboodt, Lennart Philips Lighting

Comment Type **TR** Comment Status **X** PD Signatures

"A single-signature PD shall present a valid detection signature, as defined in Table 145-20, on a given Mode when no voltage or current is applied to the other Mode, and shall present an invalid detection signature on that Mode when any voltage between 10.1 V and 57 V is applied to the other Mode. These requirements apply to both Mode A and Mode B."

The requirement only holds for corrupting voltages above 10.1V, whereas connection check entirely operates below 10.1V.

See http://www.ieee802.org/3/bt/public/may17/yseboodt_09_0517_signature.pdf for problem description.

SuggestedRemedy

Change first paragraph of 145.3.5 to read:

"A single-signature PD shall present a valid detection signature, as defined in Table 145-20, on a given Mode when no voltage or current is applied to the other Mode, and shall not present a valid detection signature on that Mode when any voltage between 3.7 V and 57 V is applied to the other Mode. These requirements apply to both Mode A and Mode B.

NOTE - A detection signature is only considered valid when it meets Table 145-20 over the entire PD detection voltage range of 2.7 V to 10.1 V."

Proposed Response Response Status **W**

TFTD

Cl 145 SC 145.3.5 P 183 L 24 # i-436
 Darshan, Yair

Comment Type **T** Comment Status **X** PD Signatures

In the text "A single-signature PD shall present a valid detection signature, as defined in Table 145-20, on a given Mode when no voltage or current is applied to the other Mode, and shall present an invalid detection signature on that Mode when any voltage between 10.1 V and 57 V is applied to the other Mode. These requirements apply to both Mode A and Mode B."

The part "and shall present an invalid detection signature on that Mode when any voltage between 10.1 V and 57 V is applied to the other Mode. These requirements apply to both Mode A and Mode B." doesn't guarantee (especially "between 10.1 V and 57 V") that for any voltage X in the range of 2.7V to 57V that is applied to the 1st pair and is higher by 1 V from the voltage applied to the 2nd pair that is being detected, will be result with invalid signature in the pair that is being detected.

SuggestedRemedy

Change from: "A single-signature PD shall present a valid detection signature, as defined in Table 145-20, on a given Mode when no voltage or current is applied to the other Mode, and shall present an invalid detection signature on that Mode when any voltage between 10.1 V and 57 V is applied to the other Mode. These requirements apply to both Mode A and Mode B."

To: "A single-signature PD shall present a valid detection signature, as defined in Table 145-20, on a given Mode when no voltage or current is applied to the other Mode, and shall present an invalid detection signature on that Mode when any voltage between Vx and 57 V is applied to the other Mode when Vx is greater by at least 1V from the voltage applied to the other mode. These requirements apply to both Mode A and Mode B."

Proposed Response Response Status **W**

TFTD

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.3.6.1 P 185 L 7 # i-340
 Jones, Chad Cisco Systems, Inc.

Comment Type E Comment Status D Editorial

the sentence at line 4 should be merged with the first sentence of the third paragraph (on line 7) to make one paragraph. The third paragraph would then be the remainder of the text at line 8. see proposed change where I've made the edit.

I also, gave a second option that combines to one paragraph and reorders the sentences. no change to the wording has occurred, this is purely editorial.

The reason for the change is the arrangement now implies the rest of the third paragraph only applies to DS PDs.

SuggestedRemedy

new paragraphs:

Single-signature PDs shall advertise class signatures according to the PD Type and PD requested Class, as defined in Table 145-24. Dual-signature PDs shall advertise class signatures according to the PD Type and PD requested Class on each pairset, as defined in Table 145-25.

The PD requested Class on a pairset is the maximum amount of power requested by the PD on that pairset. Dual-signature PDs may advertise different class signatures on each pairset. A dual-signature PD that is powered over only one pairset shall present a valid class signature on the unpowered pairset.

Alternate option for rearranging:

The PD requested Class on a pairset is the maximum amount of power requested by the PD on that pairset. Single-signature PDs shall advertise class signatures according to the PD Type and PD requested Class, as defined in Table 145-24. Dual-signature PDs shall advertise class signatures according to the PD Type and PD requested Class on each pairset, as defined in Table 145-25. Dual-signature PDs may advertise different class signatures on each pairset. A dual-signature PD that is powered over only one pairset shall present a valid class signature on the unpowered pairset.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Rearrange as:

Single-signature PDs shall advertise class signatures according to the PD Type and PD requested Class, as defined in Table 145-24. Dual-signature PDs shall advertise class signatures according to the PD Type and PD requested Class on each pairset, as defined in Table 145-25.

The PD requested Class on a pairset is the maximum amount of power requested by the PD on that pairset. Dual-signature PDs may advertise different class signatures on each pairset. A dual-signature PD that is powered over only one pairset shall present a valid class signature on the unpowered pairset.

TFTD LY

The sentence "The PD requested Class on a pairset is the maximum amount of power requested by the PD on that pairset." ONLY applies to dual-signature. This no longer

apparent from the re-ordering. I don't understand the issue being addressed by this comment.

TFTD DS

Proposed response is not true for all PDs. For a single-signature PD, the PD requested Class on a pairset is the maximum amount of power requested by the PD on BOTH pairsets; for example, a single-signature PD does not request Class 8 power on "[solely] that pairset".

To address the confusion, adopt the following remedy:

* Before "The PD requested Class on a pairset...", add "For dual-signature PDs,"

* After "Single-signature PDs shall advertise class signatures...", add "For single-signature PDs, the PD requested Class on either pairset is the maximum amount of power requested by the PD on both pairsets."

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Cl 145 SC 145.3.6.1 P 186 L 32 # i-153
 Yseboodt, Lennart Philips Lighting

Comment Type **TR** Comment Status **X** PD Reset

In Table 145-26, Item 6, we find V_Reset_PD which is a range between 0V and 2.81V. The additional information points to 145.3.8.1, which says nothing about this parameter.

VReset_PD isn't mentioned anywhere in the document, with the exception that it is used in the state diagram.

Specifically, there is a global arc into IDLE with $VPD < V_Reset_PD * other_conditions$.

Because V_Reset_PD is a range, consistent with other parameters that are a range, this means the PD can choose any voltage between 0V and 2.81V and use this as the reset threshold.

This is wrong - the PD should return to IDLE and stay there whenever the voltage is less than 2.81V.

SuggestedRemedy

- Change the definition of VReset_PD in 145.3.3.3 to read as follows:
"VReset_PD max: The maximum PD reset voltage (see Table 145-26).
- Change all occurrences of "VReset_PD" to "VReset_PD max" in the state diagrams in 145.3.3.7
- Change the additional information in Table 145-26, item 6 to read "See 145.3.6.1" (PD Multiple-Event class signature)
- Append a paragraph to 145.3.6.1 that reads as follows:
"V_Reset_PD, as defined in Table 145-26, is the voltage range in which the PD transitions to IDLE, thereby resetting the class event count."
- Make the same changes for dual-signature as appropriate.

Proposed Response Response Status **W**

TFTD

From page 186, line 48: VReset_th is the PI voltage threshold at which the PD transitions from a DO_MARK_EVENT state to IDLE as shown in Figure 145-26 and Figure 145-28.

That being the case, shouldn't we use Vreset_th since that is when the PD actually goes back to IDLE? However, the transition from IDLE to DO_DETECTION is then based on Vreset_PD which makes sense. So you may instantaneously transition through IDLE to detection...

TFTD DS

Change " $VPD < VReset_PD$ " to " $VPD < VReset_th$ " in global entry arcs into PD IDLE state (Figures 145-26, 145-28).

Cl 145 SC 145.3.8 P 187 L 1 # i-154
 Yseboodt, Lennart Philips Lighting

Comment Type **ER** Comment Status **D** Editorial

Table 145-28, the big PD Table, nearly every parameter has the value specified 'per the assigned Class'.

Exceptions: V_Trans_Io-2P, Voverload-2P, Tinnrush_PD, Tdelay-2P, Islewrate,VNoise_PD, Von_PD, Voff_PD, TClass_PD, and Vbfd.

All of the exceptions apply to both Type 3 and Type 4. All of the others are determined by Class.

We don't need the PD Type column in this Table at all, it doesn't tell us anything new, nor has it any technical significance.

SuggestedRemedy

Remove PD Type column from Table 145-28.

Proposed Response Response Status **W**

PROPOSED ACCEPT.

TFTD YD

Make sense but need discussion

TFTD HS

Voverload-2P violates this and needs the Type column.

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.3.6.2 P 187 L 13 # i-329
 Abramson, David Texas Instruments Inc

Comment Type ER Comment Status D Editorial

"The PD shall not draw more power than the power consumed during the time from TAUTO_PD1 to TAUTO_PD2..."
 We have a name for that amount of power, its called Pautoclass_PD as defined in the previous sentence.

SuggestedRemedy

Change sentence to: "The PD shall not draw more than Pautoclass_PD at any point..."

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD LY

Please quote completely, remedy is ambiguous.

Response DNA:

Here is the full sentence:

The PD shall not draw more power than Pautoclass_PD at any point until VPD falls below VReset_th, unless the PD successfully negotiates a higher power level, up to the PD requested Class, through Data Link Layer classification as defined in 145.5.

Cl 145 SC 145.3.8 P 188 L 21 # i-156
 Yseboodt, Lennart Philips Lighting

Comment Type ER Comment Status D PD Power

Table 145-28, item 2, V_Trans_lo-2P says in the additional information "For time duration defined in 145.2.8.3".
 It is not immediately apparant that this applies to transients of no more than 250 microseconds.
 In general pointing to the PSE section inside of the PD section for parameters is bad.

SuggestedRemedy

- Replace add. info by: "See 145.3.8.1."

- Add the following to 145.3.8.1:

"During a voltage transient, VPD may fall as low as VTran_lo-2P for up to 250 microseconds."

Note: if the other comment on KTran/VTran is accepted, the parameter name is VTran_PD-2P rather than VTran_lo-2P.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD HS

Wait for outcome of i-311

Cl 145 SC 145.3.8 P 188 L 51 # i-157
 Yseboodt, Lennart Philips Lighting

Comment Type E Comment Status D Editorial

Table 145-28, parameter Tdelay-2P.

For parameters that deal with time and are not exclusive to dual-signature, the "-2P" suffix doesn't make too much sense.

SuggestedRemedy

Rename Tdelay-2P to Tdelay throughout Clause 145.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD YD

Reject: The issue is not that it is exclusive for dual-sig. These parameters are part of a group that ensures that each pairset can be protected individually for single-signature and dual-signature. Using -2P add clarity for the intent and prevent intrpretations that the control on each pairset must be doe simultaneously.

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

CI 145 SC 145.3.8 P 189 L 7 # i-482
 Bennet, Ken

Comment Type T Comment Status D PD Power

"Table 145-28, items 10, 11 Describe input average power by class, labels it PClass_PD(-2P), and specifies it with a value in the Max Column, inferring that it has a range.

PClass_PD is a constant, and a limit. Items 8 and 9 correctly convey this. Items 10, 11 are ambiguous, and may result in misinterpretations of PClass_PD."

SuggestedRemedy

"1) In items 10, 11, change the description to ""Maximum""input average power..." And
 2) Either Merge the min and max cells for items 10, 11, or set both the min and the max values to the same PClass_PD value"

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

In items 10, 11, change the description to "Maximum input average power..."

TFTD LY

There are a whole bunch of parameters that are either a minimum or a maximum. That is obvious from only one of the two columns being filled out and the other empty. None of them state "Minimum" or "Maximum" in the parameter description. Here is the way to read this parameter: "PClass PD is the input average power, ... and it is a maximum because only the "Max" column is filled out". Where is the confusion ?

TFTD DS

Also change "PClass_PD-2P, Class 1" to 3.84 (is 3.86) to match "PClass_PD, Class 1".

CI 145 SC 145.3.9 P 189 L 42 # i-437
 Darshan, Yair

Comment Type T Comment Status X PD Power

This comment marked CLASS8_PPD. Table 145-28 item 12, Ppeak_PD: It should be 74.9 (1.05*71.3=74.865=>74.9W.

SuggestedRemedy

Option 1 (Recommended):
 Change from 74.8W to 74.9W
 Option 2:
 Keep it 74.8W

Proposed Response Response Status W

TFTD

Is there a reason we wouldn't round it up?

See 421

TFTD YD

The reason why we don't round it up is when you will use equations in the spec you will get wrong results for other parameters so the way I am doing it, all spec parts are in 100% sync to within less than 0.1W.

CI 145 SC 145.3.8.1 P 191 L 15 # i-328
 Abramson, David Texas Instruments Inc

Comment Type ER Comment Status D Editorial

Description of "nopower" is not in sync with state diagram which shows a transition to a new state.

SuggestedRemedy

Change "When the PD has reached POWER_DELAY or POWERED and VPD falls below VOff_PD, the PD may show a valid or invalid detection signature, and may or may not draw mark current, draw any class current, and show MPS."

to: ""When the PD is in POWER_DELAY or POWERED and VPD falls below VOff_PD, the PD transitions to NOPOWER and may show a valid or invalid detection signature, and may or may not draw mark current, draw any class current, and show MPS."

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD HS

This implies the allowance only exists while in the NOPOWER state, which is not true. Better to reference the nopower variable.

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.3.8.2 P 191 L 27 # i-341
 Jones, Chad Cisco Systems, Inc.

Comment Type ER Comment Status D

missing comma in this text:
 including any peak power drawn per 145.3.8.4 [comma] shall be calculated over a 1 second sliding

SuggestedRemedy

change to: including any peak power drawn per 145.3.8.4 shall be calculated over a 1 second sliding

Proposed Response Response Status W

TFTD

wait for 330, 159

TFTD CJ

I neglected to actually include the comma in my suggested remedy...
 Assuming we will accept 159 (because 330 removes the shall) the sentence should read:

The maximum average power, P Class_PD or P Class_PD-2P in Table 145-28 or PDMaxPowerValue in 145.5.3.3.3, including any peak power drawn per 145.3.8.4, shall be measured using a 1 second sliding window.

Cl 145 SC 145.3.8.2 P 191 L 27 # i-330
 Abramson, David Texas Instruments Inc

Comment Type TR Comment Status X PD Power

"The maximum average power, PClass_PD or PClass_PD-2P in Table 145-28 or PDMaxPowerValue in 145.5.3.3.3, including any peak power drawn per 145.3.8.4 shall be calculated over a 1 second sliding window."

What/Who is this a requirement on? The PSE? The guy in the lab who is measuring it during QC?

SuggestedRemedy

Change to: "The maximum average power, PClass_PD or PClass_PD-2P in Table 145-28 or PDMaxPowerValue in 145.5.3.3.3, including any peak power drawn per 145.3.8.4 is calculated over a 1 second sliding window."

Proposed Response Response Status W

TFTD

See 159

TFTD DS

The best of both worlds:
 "The maximum average power, PClass_PD or PClass_PD-2P in Table 145-28 or PDMaxPowerValue in 145.5.3.3.3, including any peak power drawn per 145.3.8.4, is measured using a sliding window with a width of 1 second."

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.3.8.2 P 191 L 27 # i-159
 Yseboodt, Lennart Philips Lighting

Comment Type ER Comment Status X Sliding

Topic:SLIDING
 Issue: we use the concept of 'sliding windows' in our draft very inconsistently, the SLIDING comments try to make the whole bunch consistent.
 Aim: get everything in the form "measure xxx using a xx time sliding window".

"The maximum average power, P Class_PD or P Class_PD-2P in Table 145-28 or PDMaxPowerValue in 145.5.3.3.3, including any peak power drawn per 145.3.8.4 shall be calculated over a 1 second sliding window."

SuggestedRemedy

"The maximum average power, P Class_PD or P Class_PD-2P in Table 145-28 or PDMaxPowerValue in 145.5.3.3.3, including any peak power drawn per 145.3.8.4 shall be measured using a 1 second sliding window."

Proposed Response Response Status W

TFTD

See 330

TFTD DS

The best of both worlds:

"The maximum average power, PClass_PD or PClass_PD-2P in Table 145-28 or PDMaxPowerValue in 145.5.3.3.3, including any peak power drawn per 145.3.8.4, is measured using a sliding window with a width of 1 second."

TFTD CJ

I neglected to actually include the comma in my suggested remedy...

Assuming we will accept 159 (because 330 removes the shall) the sentence should read:

The maximum average power, P Class_PD or P Class_PD-2P in Table 145-28 or PDMaxPowerValue in 145.5.3.3.3, including any peak power drawn per 145.3.8.4, shall be measured using a 1 second sliding window.

Cl 145 SC 145.3.8.3 P 192 L 11 # i-488
 Johnson, Peter

Comment Type T Comment Status X PD Inrush

Present text is "A PD may limit the inrush current below I_Inrush_PD and I_Inrush_PD-2P to allow for large values..."

This instance is part of a broader problem where certain parameters in certain tables have a MAX is specified but no MIN, and are treated as if they are constants rather than ranges with no minimum value. If the parameter is truly a constant, then it seems it should appear in both MIN and MAX columns of the table.

SuggestedRemedy

The quick fix in this instance is to use I_Inrush_PD(max) and I_Inrush_PD-2P(max).

Proposed Response Response Status W

TFTD

TFTD LY

If a parameter "P" has both a Min and a Max, then P is a range. Referring to simply P means any value in the range. If a parameter "P" only has a Min or a Max, then P is a minimum or a maximum. Referring to P then means referring to a single number in the context of either a minimum or a maximum. Does the draft contain references to parameters that are a Min or Max, but get treated like a range ? Then we should fix those.

Cl 145 SC 145.3.8.3 P 192 L 21 # i-489
 Johnson, Peter

Comment Type T Comment Status X PD Inrush

Present text is "PDs shall draw less than I_Inrush_PD and I_Inrush_PD-2P from T_Inrush_PD(max) until T_delay-2P(min), when..."

At face value, this says neither the PD nor the PSE should be current limiting after T_Inrush_PD(max). But it also suggests that a PD that implements current limiting at a low threshold (e.g. 100mA) must then drop below that threshold after Tinrush_PD(max). Is that what was meant by this paragraph?

SuggestedRemedy

I cannot propose a solution here without a better understanding of what was meant by the paragraph. I would want to be sure that the paragraph is either correctly using I_Inrush_PD and I_Inrush_PD-2P or that the intent requires using I_Inrush_PD(max) and I_Inrush_PD-2P(max)

Proposed Response Response Status W

TFTD

The intent is to say that after Tinrush_PD(max) the PD must have its current controlled so that it draws less than linrush(-2p). After T_delay-2P it can then draw the power assigned to it during classification.

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.3.8.4 P 192 L 48 # i-164

Yseboodt, Lennart

Philips Lighting

Comment Type TR Comment Status D PD Power

"Peak operating power shall not exceed P Peak_PD."

It is not stated that this applies to single-signature PDs only.

SuggestedRemedy

"Peak operating power for single-signature PDs shall not exceed P Peak_PD."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

The shall is already contained in the Table 145-28.

Replace sentence with: "Ppeak_PD is the maximum peak operating power and applies to single-signature PDs."

TFTD HS

These are very useful for PICS. Is there a technical reason to remove them?

Cl 145 SC 145.3.8.4 P 192 L 52 # i-165

Yseboodt, Lennart

Philips Lighting

Comment Type TR Comment Status D PD Power

"Peak operating power shall not exceed P Peak_PD-2P."

It is not stated that this applies to dual-signature PDs only.

SuggestedRemedy

"Peak operating power for dual-signature PDs shall not exceed P Peak_PD-2P."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

The shall is already contained in the Table 145-28.

Replace sentence with: "Ppeak_PD-2P is the maximum peak operating power on a pairset and applies to dual-signature PDs."

TFTD HS

These are very useful for PICS. Is there a technical reason to remove them?

Cl 145 SC 145.3.8.4 P 193 L 31 # i-439

Darshan, Yair

Comment Type T Comment Status X PD Power

In the text "The equations in Table 145-28 are used to approximate the ratiometric peak powers of Class 1 through Class 8." . The equations are not in Table 145-28 and are missing for this clause.

SuggestedRemedy

1. Change from "The equations in Table 145-28 are used to approximate the ratiometric peak powers of Class 1 through Class 8."

To: "Equations 145-X and Equation 145-Y are used to approximate the ratiometric peak powers of Class 1 through Class 8."

2. Add the following text and equations at the end of this paragraph:

$P_{Peak_PD} = 1.05 * P_{DMaxPowerValue}$ (145-X)

$P_{Peak_PD-2P} = 1.05 * P_{DMaxPowerValue_mode(X)}$ (145-Y)

Where

$P_{DMaxPowerValue}$ as defined in Table 145-22

$P_{DMaxPowerValue_mode(X)}$ as defined in Table 145-22

Proposed Response Response Status W

TFTD

How did we get here? Did we replace equations with numbers at some point and not update this?

1. Change from "The equations in Table 145-28 are used to approximate the ratiometric peak powers of Class 1 through Class 8."

To: "Equations 145-X and Equation 145-Y are used to approximate the ratiometric peak powers of Class 1 through Class 8."

2. Add the following text and equations at the end of this paragraph:

$P_{Peak_PD} = 1.05 * P_{DMaxPowerValue}$ (145-X)

$P_{Peak_PD-2P} = 1.05 * P_{DMaxPowerValue_mode(X)}$ (145-Y)

Where

$P_{DMaxPowerValue}$ is defined in Table 145-22

$P_{DMaxPowerValue_mode(X)}$ is defined in Table 145-22

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.3.8.4 P 193 L 34 # i-440
Darshan, Yair

Comment Type T Comment Status D PD Power

In the text "These equations may be used to calculate PPeak_PD or PPeak_PD-2P for Data Link Layer classification by substituting PClass_PD or PClass_PD-2P with PDMaxPowerValue and for Autoclass by substituting PClass_PD with PAutoclass_PD." Missing "or PDMaxPowerValue_mode(X)"

SuggestedRemedy

Change from: "These equations may be used to calculate PPeak_PD or PPeak_PD-2P for Data Link Layer classification by substituting PClass_PD or PClass_PD-2P with PDMaxPowerValue and for Autoclass by substituting PClass_PD with PAutoclass_PD."

To: "These equations may be used to calculate PPeak_PD or PPeak_PD-2P for Data Link Layer classification by substituting PClass_PD or PClass_PD-2P with PDMaxPowerValue or DMaxPowerValue_mode(X) and for Autoclass by substituting PClass_PD with PAutoclass_PD."

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD DS

Typo; accept suggested remedy, changing "or DMaxPowerValue_mode(X)" to "or PDMaxPowerValue_mode(X)"

Cl 145 SC 145.3.8.4.1 P 193 L 41 # i-483
Bennet, Ken

Comment Type T Comment Status D PD Power

"This comment addresses all statements in this paragraph that reference Pport_PD (and Pport_PD-2P). One example is: ""the peak power shall not exceed PPort_PD for...""

""Pport_PD"" is the input average power. The statements should reference the MAXIMUM input average power to be correct. "

SuggestedRemedy

For each occurrence of Pport_PD and Pport_PD-2P, either precede it with "maximum", or add a "_max" suffix.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Editorial license given to make sure maximum is appropriate for each occurrence.

TFTD LY

Agree with prepending with word "maximum". Ken - please provide specific editing instructions.

Cl 145 SC 145.3.8.6 P 194 L 4 # i-484
Bennett, Ken

Comment Type T Comment Status X PD Power

"The sentence starting with ""A single-signature PD includes CPort..."" leads into a listing of PD Types and Cport values that ""Intrinsically meet the requirements in this subclause"". These are informative statements, and are not entirely correct:

1) A type 4 PD with 360uF can be assigned a class corresponding to Type 3 limits. The Type 3 limit is 180uF, so the Type 4 limit of 360uF is not true in this case.

2) It's conceivable for any of the cases that a transient could cause a power surge and/or fault in a PD for reasons other than just Cport."

SuggestedRemedy

Delete the text starting at line 4 ("A single signature PD includes...") and ending at line 17, just after the list of PD types and capacitances.

Proposed Response Response Status W

TFTD

Should we just transition this list to class based?

Cl 145 SC 145.3.8.6 P 194 L 30 # i-315
Stover, David Analog Devices Inc.

Comment Type TR Comment Status X PD Power

*** Comment submitted with the file 94179800003-i_tr_3.png attached ***

Math for TR3 doesn't pencil out given the input cap requirements listed in this section. See attachment for simulation showcasing the problem statement. As a result, I_TR_LIM,max for assigned Class >= 5 needs slightly increased.

SuggestedRemedy

Modify I_TR3,max for single-signature PDs assigned Class >= 5 from "3" to "3.1"

Proposed Response Response Status W

TFTD

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.3.8.6 P 194 L 37 # i-338
 Lemahieu, Joris ON Semiconductor

Comment Type TR Comment Status X PD Power

The PD state diagram states that does not need to implement a current limit in the POWERED state.
 (pd_current_limit <= FALSE)

This new ITR_LIM spec now seems to indicate the opposite.

SuggestedRemedy

Suppress the ITR_LIM requirement:

- Delete "the peak current shall not exceed ITR_LIM, as defined in Table 145-30, and"
- Delete Table 145-30

Proposed Response Response Status W

TFTD

We should also discuss if we want to change the variable name "pd_current_limit" in the SD since it is very misleading. PDs are not required to "limit current", they are just subject to policing at certain times and thus should not draw unlimited current (which they can during Inrush.

TFTD DS

I_TR_LIM requirement does apply to the POWERED state.

See response to i-136 (pd_current_limit is redundant with pd_max_power and should be deleted).

Cl 145 SC 145.3.8.7 P 195 L 11 # i-343
 Jones, Chad Cisco Systems, Inc.

Comment Type E Comment Status X PD Power

Chair notes... lines 11- 15, this is not information that helps ensure interoperability. It may cause more confusion to the reader than help. This was discussed in previous meetings but deferred to 3.0.

SuggestedRemedy

delete: Limits are provided to preserve data integrity. To meet EMI standards, lower values may be needed. NOTE--The worst-case condition is when both PSE and PD generate the maximum noise allowed by Table 145-16 and Table 145-28, which may cause a higher noise level to appear at the PI than the standalone case as specified by this clause.

Proposed Response Response Status W

TFTD

Cl 145 SC 145.3.8.8 P 195 L 17 # i-331
 Abramson, David Texas Instruments Inc

Comment Type ER Comment Status D Editorial

Why is classification stability time in the PD power section? Why not in the classification section?

SuggestedRemedy

Move 145.3.8.8 to 145.3.6.1.2. Also move item 19 in Table 145-28 to Table 145-26

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Move 145.3.8.8 to 145.3.6.1.2 after making all other changes to 145.3.8.8. Also move item 19 in Table 145-28 to Table 145-26.

TFTD DS

Backfeed voltage (Vbfd, item 19) is not referenced in section 145.3.8.8. Please provide justification for moving Vbfd from power supply limits table to multi-event classification table.

Cl 145 SC 145.3.8.10 P 196 L 7 # i-313
 Stover, David Analog Devices Inc.

Comment Type TR Comment Status D Pres: Yseboodt3

ICon-2p-unb has no maximum; this statement ("Single-signature PDs shall not exceed ICon-2P-unb for longer than TCUT-2P min and 5% duty cycle") does not enforce any current limitation on the PD.

SuggestedRemedy

Change "ICon-2p-unb" to "ICon-2p-unb,min"

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD LY

See yseboodt 03 which makes ICon-2P-unb a maximum.

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.3.8.10 P 196 L 7 # i-487
 Johnson, Peter

Comment Type T Comment Status X PD Power

The text "Single-signature PDs shall not exceed ICon-2P-unb for longer than TCUT-2P min and 5 % duty cycle, and shall not exceed IPeak-2P-unb, as defined in Equation (145-12) on any pair..." fails to account for the fact that there are many combinations of PSE voltage and PD class where IPeak-2P_unb is a value LESS than ICon-2P-unb. It makes no sense that peak power must be less than continuous power.

SuggestedRemedy

This creates a fundamental dilemma because IPeak-2P_unb is a function of V_PSE and therefore only the PSE knows what IPeak-2P_unb current is, not the PD. To be universal, PD current balance, both instantaneous and average, must therefore be restricted to ICon-2P-unb. Language would be: "Single-signature PDs shall not exceed ICon-2P-unb on any pair..."

Proposed Response Response Status W

TFTD

Cl 145 SC 145.3.8.10 P 197 L 1 # i-173
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status X Pres: Darshan3

Calculations using the model in Figure 145-31, Equation 145-27, and Equation 145-26 show that pair currents often exceed ICon-2P-unb, even though line 39 on page 195 promises: "PDs that meet Equation (145-26) intrinsically meet unbalance requirements."

I guess... that changes in earlier drafts to power parameters require us to update the magic numbers in Equation 145-26.

SuggestedRemedy

Don't know how to fix this... Yair ?

Proposed Response Response Status W

TFTD

TFTD YD

See darshan_03_0917.pdf for remedy

WFP

Cl 145 SC 145.3.9 P 197 L 16 # i-333
 Abramson, David Texas Instruments Inc

Comment Type TR Comment Status D PD MPS

"A PD shall have TMPS_PD measured with a series resistance representing the worst case cable resistance between the measurement point and the PD PI."

Sentence places requirement on measurer rather than PD, needs to be reworded.

SuggestedRemedy

Replace with: "A PD shall meet the TMPS_PD requirement with a series resistance representing the worst case cable resistance between the measurement point and the PD PI."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Replace with: "A PD shall meet the TMPS_PD requirement with a series resistance representing the worst case cable resistance between the measurement point and the PD PI."

TFTD HS

Typo "series" otherwise AIP (already fixed)

TFTD CJ

spelling error in suggested remedy. Make it AIP and fix spelling.

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

CI 145 SC 145.3.9 P 198 L 10 # i-287
 Stewart, Heath Analog Devices Inc.

Comment Type E Comment Status D PD MPS

All other tables carefully describe whether an item or row is attributable to single-signature or dual-signature PDs.
 Table 145-31 does not follow this convention

SuggestedRemedy

Change Table 145-31 as follows
 Item 1
 Change "Class 1 to 4" to "Single-signature PD, Class 1 to 4"
 Change "Class 5 to 8" to "Single-signature PD, Class 5 to 8"
 Change "Class 1 to 5" to "Dual-signature PD, Class 1 to 5"

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Change Table 145-31 as follows:
 Item 1
 Change "Class 1 to 4" to "Single-signature PD, Class 1 to 4"
 Change "Class 5 to 8" to "Single-signature PD, Class 5 to 8"
 Item 2
 Change "Class 1 to 5" to "Dual-signature PD, Class 1 to 5"

TFTD LY

You guys have no feeling whatsoever for Table esthetics. Better solution: - change description of item 1 to read: "Total input current per the assigned Class, for single-signature PDs" - change description of item 2 to read: "Input current on each powered pairsetm for dual-signature PDs".

Response DNA: Lennart, you have no feeling for spelling. What is a pairsetm?

TFTD YD

Class 1-4 could be legacy which is not single-sig

Response DNA: No, this clause is only specifying Types 3 and 4 which are either single-sig or dual-sig.

CI 145 SC 145.4.3 P 201 L 19 # i-383
 Thompson, Geoffrey Individual

Comment Type ER Comment Status X AES

Is this a PSE spec or a PD spec? Which PI is it measured at. Is this a controlling spec (it has a "shall") or a resultant spec that is a check of other specs? If this is not met where do you go to fix it?

SuggestedRemedy

Define what portion of the system this applies to and where to measure it. If it is an element spec then move it into the element that it is related to. If it is a system check spec then remove the shall and refer to the controlling element specs that will remedy any failure.

Proposed Response Response Status W

TFTD

CI 145 SC 145.4.6 P 205 L 42 # i-219
 Mcclellan, Brett Marvell Semiconducto

Comment Type TR Comment Status D AES

E_d_out is a time domain peak to peak voltage but the formula defines E_d_out as varying across frequency. E_d_out isn't measured at individual frequencies.

SuggestedRemedy

delete formula (145-31) and the text defining f and fmax
 change text on line 38 from:
 "shall not exceed the requirements Equation (145-31)" (note the missing 'of')
 to "shall not exceed 10 mV peak-to-peak when measured in the band from 1 MHz to 10 MHz and shall not exceed 1mV peak-to-peak when measured in the band from 10 MHz to 100 MHz for 2.5GBASE-T, 10 MHz to 250 MHz for 5GBASE-T, and 10 MHz to 500 MHz for 10GBASE-T"

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD GZ

Same as 227

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.4.7 P 205 L 51 # i-387
 Thompson, Geoffrey Individual

Comment Type TR Comment Status X AES

It is unclear whether this is a spec for the cabling or a load spec for the PSE. It needs to have a more complete requirement and be moved to the PSE or link segment clause. Expressing it in terms of the "PHY" and the "MDI" causes further confusion as which MDI is not specified nor is what to be done for a midspan system.

SuggestedRemedy

Clarify and place as appropriate.

Proposed Response Response Status W

TFTD

Cl 145 SC 145.4.9.1.1 P 208 L 9 # i-226
 McClellan, Brett Marvell Semiconducto

Comment Type E Comment Status X AES

Most of the text and formulas in 145.4.9.1.x and 145.4.9.2.x are identical to 33.4.9.1.x and 33.4.9.2.x. Rather than repeat the same requirements, 145.4.9.1.x and 145.4.9.2.x should just reference Clause 33 instead of duplicating text and formulas.

SuggestedRemedy

For each subclause 145.4.9.1.x and 145.4.9.2.x delete redundant text and formulas and place a reference to the requirements in 33.4.9.1.x and 33.4.9.2.x.

Proposed Response Response Status W

TFTD

TFTD GZ

Recommend not to do this – clause 33 might get deprecated in the future, and it would cause a lot of work.

Cl 145 SC 145.4.9.1.1 P 208 L 31 # i-220
 McClellan, Brett Marvell Semiconducto

Comment Type TR Comment Status D AES

NEXT loss for PSE midspan is 40dB at 100MHz, however 2.5/5GBASE-T budgets 43dB for connectors.

SuggestedRemedy

change "40" to "43"

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD YD

Need to check

Cl 145 SC 145.4.9.1.3 P 209 L 37 # i-240
 Zimmerman, George Aquantia, ADI, Comm

Comment Type T Comment Status X AES

Return loss on PSE midspan for 2.5G/5GBASE-T should be based on Cat 5e not on clause 40 requirements predating cat 5e. Return loss limit at 20MHz violates the RL spec in 126.7.2.3 for 2.5G and 5G (17dB). Make consistent with Cat 5e connector return loss specifications.

SuggestedRemedy

Delete "or 2.5G/5GBASE-T" from 2nd row of 1st column of Table 145-35.

Insert new row "2.5G/5GBASE-T" between 10/100/1000BASE-T row and 5GBASE-T row, with frequency ranges of:

1<f<= 31.5 MHz at a return loss value of 30 dB, and

31.5 MHz<f<=100MHz at a return loss value of 20 - 20log10(f/100) dB

Change 5GBASE-T row return loss value (100 MHz<= f<= 250 MHz) from 14 dB to 20 dB

Proposed Response Response Status W

TFTD

align with 221

Cl 145 SC 145.4.9.1.3 P 209 L 41 # i-221
 McClellan, Brett Marvell Semiconducto

Comment Type TR Comment Status X AES

The return loss limit at 20MHz violates the RL spec in 126.7.2.3 for 2.5G and 5G (17dB).

SuggestedRemedy

create a separate table entry for 2.5GBASE-T with the following limits based on Cat5E:

1 MHz<f<=31.5 MHz 30 dB

31.5 MHz<f<=100 MHz 20-20log10(f/100)

Proposed Response Response Status W

TFTD

align with 240

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Cl 145 SC 145.4.9.1.3 P 209 L 42 # i-222
 Mcclellan, Brett Marvell Semiconducto

Comment Type **TR** Comment Status **X** AES

at 100MHz the limit of 14dB is only 4dB margin vs the 2.5/5G spec

SuggestedRemedy

create a separate table entry for 5GBASE-T with the following limits based on Cat6:

1 MHz<f<=50 MHz 30 dB
 50 MHz<f<=250 MHz 24-20log10(f/100)

Proposed Response Response Status **W**

TFTD

TFTD GZ

Reason: These are the same issue as i-210/i-239 except for 5GBASE-T instead of 2.5GBASE-T. We expect the resolution here will be to adopt the equation of i-239 for 5GBASE-T (Using Cat5e connector requirements frequency extended for a 5G midspan rather than Cat 6), but use the separate-entry structure in the i-211 comment, so the resolution is a bit of a mixture.

TFTD YD

Go with CAT5E spec to have some margins to MIDSPAN. Not see a reason why to tighten the spec and give the link section the margin. From "channel/link section point of view" it should be OK. Base on 10G experience.
 Same for i-222.

Cl 145 SC 145.4.9.2 P 210 L 19 # i-336
 Maguire, Valerie The Siemon Company

Comment Type **T** Comment Status **D** AES

Support of 2.5GBASE-T with category 5e and support of 5GBASE-T with category 6 is only in the case that the cabling meets the additional requirements specified in clause 126.7 of 802.3bz.

SuggestedRemedy

Add a footnote referencing back to the 2.5GBASE-T and 5GBASE-T column rows that says, "For defined uses cases (refer to IEEE Std 802.3bz(TM)-2016). Category 6A cord in ISO/IEC 11801-1 or ANSI/TIA-568-C.2 recommended."

Proposed Response Response Status **W**

PROPOSED ACCEPT.

TFTD LY

Very terse sentences,,, suggest: "For defined uses cases refer to IEEE Std 802.3bz(TM)-2016. Use of Category 6A cord in ISO/IEC 11801-1 or ANSI/TIA-568-C.2 is recommended."

TFTD CJ

I don't know that we reference to specific TF documents (802.3bz...) not use TM in our docs. At a minimum replace BZ with Clause 125.

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.5 P 212 L 0 # i-374
 Thompson, Geoffrey Individual

Comment Type TR Comment Status D Management

There is no parallel in cl. 145 to cl. 33.5. Although the group agreed that no one (that they knew of) had implemented MDIO in cl. 33 devices and, therefore, they didn't want to include it in cl. 145, there is a clear requirement in the project paperwork to do so. See Scope: "The scope of this project is to augment the capabilities of the IEEE Std 802.3 standard with 4-pair power and associated power management information."

SuggestedRemedy

Define a parallel and optional equivalent to cl. 33.5 in cl. 145.

Proposed Response Response Status W

PROPOSED REJECT.

TFTD

A specific remedy is needed.

Geoff, we are not required to do everything in the scope of the project. The scope is there to limit us from doing things outside of it.

TFTD LY

This does not break interoperability in any way, since the 33.5 interface is not related to either the PI or the MDI. It is an interface between a MAC and a PHY.

Cl 145 SC 145.5 P 212 L 0 # i-376
 Thompson, Geoffrey Individual

Comment Type TR Comment Status D Management

There is no parallel in cl. 145 to cl. 33.5. Although the group agreed that no one (that they knew of) had implemented MDIO in cl. 33 devices and, therefore, they didn't want to include it in cl. 145, there is a clear requirement in the project paperwork to do so. See Objectives: - 4PPoE PSEs will be backwards compatible with IEEE 802.3-2012 PDs. - Update management parameters."

SuggestedRemedy

Define a parallel and optional equivalent to cl. 33.5 in cl. 145.

Proposed Response Response Status W

PROPOSED REJECT.

TFTD

We have updated the management objects by deciding we no longer need them.

TFTD LY

This does not break interoperability in any way, since the 33.5 interface is not related to either the PI or the MDI. It is an interface between a MAC and a PHY.

Cl 145 SC 145.5 P 212 L 0 # i-375
 Thompson, Geoffrey Individual

Comment Type TR Comment Status D Pres: Yseboodt5

There is no parallel in cl. 145 to cl. 33.5. Although the group agreed that no one (that they knew of) had implemented MDIO in cl. 33 devices and, therefore, they didn't want to include it in cl. 145, there is a clear requirement in the project paperwork to do so. See Scope: "5 Criteria - Compatibility: All enhancements will be backward compatible with IEEE Std 802.3-2012 Clause 33."

SuggestedRemedy

Define a parallel and optional equivalent to cl. 33.5 in cl. 145.

Proposed Response Response Status W

PROPOSED REJECT.

A specific and complete remedy is needed.

TFTD

TFTD LY

This does not break interoperability in any way, since the 33.5 interface is not related to either the PI or the MDI. It is an interface between a MAC and a PHY.

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.5 P 212 L 25 # i-377
 Thompson, Geoffrey Individual

Comment Type TR Comment Status D Pres: Yseboodt5

The entire text for "Management function requirements" is missing, either as complete text or by reference to cl. 33.5.

SuggestedRemedy

Add text to specify how to control and/or read the management functions to the draft.

Proposed Response Response Status W

PROPOSED REJECT.

A specific and complete remedy is needed.

TFTD

TFTD LY

This does not break interoperability in any way, since the 33.5 interface is not related to either the PI or the MDI. It is an interface between a MAC and a PHY.

Cl 145 SC 145.5 P 212 L 30 # i-178
 Yseboodt, Lennart Philips Lighting

Comment Type TR Comment Status X DLL

"Single-signature PDs advertising a Class 4 signature or higher and dual-signature PDs support Data Link Layer classification (see 145.3.6). Data Link Layer classification is optional for all other devices."

Incorrect statement about dual-sig devices.

Also, it is better to talk about 'requested Class' than use the old term 'advertise class signature'.

SuggestedRemedy

Replace by:

"Single-signature PDs requesting Class 4 or higher and dual-signature PDs that request Class 4 or higher on either Mode support Data Link Layer classification (see 145.3.6). Data Link Layer classification is optional for all other devices."

Proposed Response Response Status W

TFTD

wait for outcome of Stover's comment making DLL required for all DS PDs.

Cl 145 SC 145.5.3.6.3 P 226 L 2 # i-441
 Darshan, Yair

Comment Type T Comment Status X Pres: Yseboodt4

This comment is marked LLDLP?_ADHOC_1.

In the LLDLP adhoc we made some changes to the PSE DLL state machine to reflect the changes made in the concept of how to fill in the TLV values of the pse_allocated_power and pse_allocated_power_alt(X) fields.

SuggestedRemedy

Adopt yseboodt_04_0917_LLDLP.pdf

Proposed Response Response Status W

TFTD

WFP

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.5.3.6.3 P 226 L 5 # i-442
 Darshan, Yair

Comment Type T Comment Status X Pres: Yseboodt4

This comment is marked LLDP?_ADHOC_2.
 This comment and proposed remedy depend on the outcome of the LLDP adhoc recommendations regarding the question if pse_dll_ready_alt(X) need to be specified per alternative as currently is or need to be pse_dll_ready. In case that it is going to be pse_dll_ready, see the proposed remedy.

SuggestedRemedy

1. Change from: "(!pse_dll_enable_alt(X) + !pse_dll_ready_alt(X)) * (sig_type = dual)"
 To: (!pse_dll_enable_alt(X) + !pse_dll_ready * (sig_type = dual))
2. In page 224 line 41 to change the pse_dll_ready_alt(X) variable definition to:
 "pse_dll_ready
 An implementation-specific control variable that indicates that the PSE has initialized Data Link Layer classification. This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.20).
 Values:
 FALSE: Data Link Layer classification has not completed initialization.
 TRUE: Data Link Layer classification has completed initialization.
3. Delete aLldpXdot3LocReadyA and aLldpXdot3LocReadyB from Table 30-7.
- 4) Delete 30.12.2.1.18a aLldpXdot3LocReadyA content.
- 5) Delete 30.12.2.1.18b aLldpXdot3LocReadyB content.
- 6) In Table 145-50 page 222 in the PSE section: Change from "aLldpXdot3LocReadyA" to "aLldpXdot3LocReady" and from "pse_dll_ready_alt(X=A)" to "pse_dll_ready)".
- 7) In Table 145-50 page 222 in the PSE section: Delete "aLldpXdot3LocReadyB" and "pse_dll_ready_alt(X=B)".

Proposed Response Response Status W

TFTD
 Need input from LLDP ad hoc.

Cl 145 SC 145.5.3.7.4 P 229 L 2 # i-443
 Darshan, Yair

Comment Type T Comment Status X Pres: Yseboodt4

This comment is marked LLDP?_ADHOC_3.
 In the LLDP adhoc we made some changes to the PD DLL state machine to reflect the changes made in the concept of how to fill in the TLV values of the pd_requested_power and pd_requested_power_mode(X) fields.

SuggestedRemedy

Adopt yseboodt_04_0917_LLDP.pdf

Proposed Response Response Status W

TFTD
 WFP

Cl 145 SC 145.5.3.7.4 P 229 L 5 # i-444
 Darshan, Yair

Comment Type T Comment Status X Pres: Yseboodt4

This comment is marked LLDP?_ADHOC_4.
 In the condition (!pd_dll_enable_mode(X) + !pd_dll_ready_mode(X)) to the IDLE state the pd_dll_ready_mode(X) need to be pd_dll_ready In order to allow progressing to the INITIALIZE state in case PD want power on the unpowered pairset.

SuggestedRemedy

1. Change from: "(!pd_dll_enable_mode(X) + !pd_dll_ready_mode(X))"
 To: (!pd_dll_enable_mode(X) + !pd_dll_ready)
2. In page 228 line 28 to change the pd_dll_ready_mode(X) variable definition to:
 "pd_dll_ready
 An implementation-specific control variable that indicates that the PD has initialized Data Link Layer classification. This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.20).
 Values:
 FALSE: Data Link Layer classification has not completed initialization.
 TRUE: Data Link Layer classification has completed initialization."
- 3) In Table 145-40 page 222, PD section: Change from "aLldpXdot3LocReadyA" to "aLldpXdot3LocReady" and from "pd_dll_ready_mode(X=A)" to "pd_dll_ready)".
4. In Table 145-40 page 222, PD section delete the row "aLldpXdot3LocReadyB" , "pd_dll_ready_mode(X=B)"

Proposed Response Response Status W

TFTD
 WFP

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145 SC 145.7.3.3 P 250 L 16 # i-339
 Lemahieu, Joris ON Semiconductor
 Comment Type E Comment Status D PICS
 Error
 SuggestedRemedy
 Change 'Transient TR2 applied' to 'Transient TR3 applied'.
 Proposed Response Response Status W
 PROPOSED ACCEPT.
 TFTD YD
 To check

Cl 145A SC 145A.2 P 261 L 39 # i-185
 Yseboodt, Lennart Philips Lighting
 Comment Type E Comment Status D Annex
 Rdiff is defined in equation 145A-3 but nowhere used.
 SuggestedRemedy
 Remove equation 145A-3 + the sentence above.
 Proposed Response Response Status W
 PROPOSED ACCEPT.
 TFTD YD
 Rdiff is required. It is the 100 miliohm. We need to integrate Rdiff in the text and then it will be OK

Cl 145A3 SC 145A3.1 P 262 L 51 # i-447
 Darshan, Yair
 Comment Type E Comment Status X Pres: Darshan7
 In the text: "The effective resistance is the measured voltage Veff, divided by the current through the path e.g. the effective value of RPSE_min for i1 is $RPSE_min = V_{eff1} / i1$ as shown in Figure 145A-2.". The effective resistance of what?
 SuggestedRemedy
 Change the mentioned text to (**):
 "The effective resistance ****Rpse_min or RPSE_max**** is the measured voltage Veff, divided by the current through the path e.g. the effective value of RPSE_min for i1 is $RPSE_min = V_{eff1} / i1$ as shown in Figure 145A-2.
 Proposed Response Response Status W
 TFTD
 WFP

Cl 145A3 SC 145A3.2 P 262 L 52 # i-448
 Darshan, Yair
 Comment Type T Comment Status X Pres: Darshan7
 The verification procedure of the measurements of Rpse_min and Rpse_max is missing from 145A.3

SuggestedRemedy
 Add the following text after line 54 in page 262:
 "Rpse_min and RPSE_max effective resistance verification procedure is described below:
 1) With the PSE powered on and connected to a constant power sink in the PD section through the elements shown in Figure 145A-2, which is set to PClass_PD measured at the PD PI, measure the currents i1, i2, i3 and i4 and the voltages Veff1, Veff2, Veff3 and Veff4.
 2) Calculate the RPSE_min and RPSE_max values of each pair of the same polarity by calculating the following:
 For the positive pairs:
 $R1 = RPSE_min = V_{eff1} / i1$
 $R2 = RPSE_max = V_{eff2} / i2$
 For the negative pairs:
 $R3 = RPSE_min = V_{eff3} / i3$
 $R4 = RPSE_max = V_{eff4} / i4$
 3) Verify that on each pair of the same polarity, RPSE_min and RPSE_max meets Equation 145-15.
 4) Repeat steps 1 to 3 with the RCh_unb_min, RPD_min swapped location with RCh_unb_max, RPD_max. "

Proposed Response Response Status W
 TFTD
 WFP

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145A3 SC 145A3.2 P 263 L 5 # i-449
Darshan, Yair

Comment Type T Comment Status X Pres: Darshan7

- Figure 145A-2 needs some improvements and corrections:
 a) It needs to be in sync with Figure 145-22 regarding the separation of Rload_min/max to its components in order to allow setting Pclass_PD at the PD PI.
 B) To describe the PSE load in a clear way.
 C) Adding the borders of the link section
 d) defining from what Rpse_min and Rpse_max consist of?
 e) Clear definition of the measurements point of Veff_i
 f) To correct the left border of the End to End pair to pair resistance arrow.

SuggestedRemedy

Replace Figure 145A-2 with the new proposal in darshan_07_0917.pdf

Proposed Response Response Status W

TFTD

WFP

Cl 145B SC 145B.1.1 P 266 L 7 # i-450
Darshan, Yair

Comment Type T Comment Status X Annex

Figure 145B-3, CC_DET_SEQ=0 for dual-signature is parallel detection and not staggered detection nor staggered power on.
 This drawing should be deleted since it doesn't fit to the definition of CC_DET_SEQ=0 for dual-signature in page 109 line 41.

SuggestedRemedy

- Options:
 1. Delete Figure 145-3 since it doesn't fit the definitions in Page 109 line 41 for dual-signature.
 2. Update the definition for CC_DET_SEQ=0 for dual-signature to parallel and staggered detection and verify that state machine support it.

Proposed Response Response Status W

TFTD

Cl 145B SC 145B P 267 L 7 # i-451
Darshan, Yair

Comment Type T Comment Status X Pres: Darshan11

Figure 145B-6 for the staggered option for the dual signature for CC_DET_SEQ=1, shows that the second alternative DETECTION starts only after the Power up of the primary alternative which is OK but not limited just to this use case. The detection can starts also after the detection of the primary alternative. We need show it by additional drawing (145-6A), or drawing that shows all possibilities.

SuggestedRemedy

Adopt darshan_11_0917.pdf

Proposed Response Response Status W

TFTD

WFP

Cl 145B SC 145B.1.2 P 267 L 11 # i-452
Darshan, Yair

Comment Type T Comment Status X Pres: Darshan11

The title of Figure 145B-6 is "Figure 145B-6--PSE implementing CC_DET_SEQ=1, do_cxn_chk result is dual, staggered power on" which is correct per the drawing description however per the definition of CC_DET_SEQ=1 for dual-signature in page 109 line 43, CC_DET_SEQ is about Connection check and detection sequences while if it is staggered power on or not in dual-signature PD, is not the main issue to emphasis.

SuggestedRemedy

Change the title of Figure 145b-6 from:
 "Figure 145B-6--PSE implementing CC_DET_SEQ=1, do_cxn_chk result is dual, staggered power on"
 To : "Figure 145B-6--PSE implementing CC_DET_SEQ=1, do_cxn_chk result is dual, staggered detection and staggered power on"

Proposed Response Response Status W

TFTD

WFP

IEEE P802.3bt D3.0 4-Pair PoE Initial Sponsor ballot comments

Cl 145B SC 145B.1.3 P 268 L 13 # i-453
 Darshan, Yair

Comment Type T Comment Status D Annex

The title of Figure 145B-9 is "Figure 145B-9--PSE implementing CC_DET_SEQ=2, do_cxn_chk result is dual, staggered power on" which is correct per the drawing description however per the definition of CC_DET_SEQ=2 for dual-signature in page 109 line46, CC_DET_SEQ is about Connection check and detection sequences while if it is staggered power on or not in dual-signature PD, is not the main issue to emphasis.

SuggestedRemedy

Change the title of Figure 145B-9 from :
 "Figure 145B-9--PSE implementing CC_DET_SEQ=2, do_cxn_chk result is dual, staggered power on"
 To : "Figure 145B-9--PSE implementing CC_DET_SEQ=2, do_cxn_chk result is dual, staggered detection and staggered power on"

Proposed Response Response Status W
 TFTD

This figure shows parallel detection at the beginning of the process and then a 2nd detection before the staggered power on.

Cl 145B SC 145B.1.4 P 268 L 46 # i-454
 Darshan, Yair

Comment Type T Comment Status X Pres: Darshan8

The title of Figure 145B-11 is "Figure 145B-11--PSE implementing CC_DET_SEQ=3, do_cxn_chk result is dual", missing the remain fact that it is staggered detection per the definition of CC_DET_SEQ=3 for dual-signature in page 109 line 48.

SuggestedRemedy

Change the title of Figure 145B-9 from :
 "Figure 145B-11--PSE implementing CC_DET_SEQ=3, do_cxn_chk result is dual"
 To : "Figure 145B-11--PSE implementing CC_DET_SEQ=3, do_cxn_chk result is dual, staggered detection and staggered power on"

Proposed Response Response Status W
 TFTD

WFP

The more comments about these figures I see, the more it would make sense for only optional behavior or function results are called out. For example, SEQ 3 says that CC is followed by staggered detection, so why do we need to call that out in the figure title?

Cl 145B SC 145B.1.4 P 268 L 268 # i-455
 Darshan, Yair

Comment Type T Comment Status X Pres: Darshan8

CC_DET_SEQ=3 means: Connection check is followed by staggered detection. Figure 145B-11 for dual-signature PD shows that CC_DEC_SEQ=3 is only possible when the Detection of the 2nd pairset starts after Tpon +Tx of 1st pairset which is possible but not the only possibility per CC_DET_SEQ=3 definition. We need clearly to show that first we see CC, and then staggered detection, and then the classification and power_on can be staggered or not. We need to add Figure 145B-11A to show this possibility that shows all possibilities.

SuggestedRemedy

Adopt darshan_08_0917.pdf

Proposed Response Response Status W

TFTD

WFP