

TDL #275 and #276 D2.1

Addressing comments: #108, #420, #421, #281

Make the following changes:

PSE-PD stability

33A.1 Recommended PSE design guidelines and test setup

1. Make the following changes:

In order to prevent potential oscillations between the PSE and PD, the sum of the PSE port output impedance (~~Z_{o_port}~~ Z_{o_pse}), the cable impedance (Z_c), the PD input port circuitry impedance (~~Z_{pd_cir}~~ Z_{cir_pd}) and the PD EMI output filter impedance (Z_{emi}) should be lower than the PD power supply input impedance ($Z_{in_ps_pd}$). All the above impedances are converted to the equivalent series impedance form as described by Figure 33A-1. ~~This sub-clause focuses on the PSE part.~~

PSE ~~Port~~PI output impedance consists of two parts:

- PSE power supply output impedance (Z_{o_ps}), which is a function of the load at the PSE ~~PI~~(~~PPort~~), and
- the ~~Series~~series elements (Z_{ser}) that connect the PSE power supply output to the PSE ~~PI~~port.

Therefore, the total PSE ~~PI~~Port output impedance during normal powering mode is ~~Z_{o_port}~~ $Z_{o_pse} = Z_{o_ps} + Z_{ser}$.

In order to maintain PSE-PD stability, the following guidelines apply:

- $Z_{o_ps\ max} = 0.3\ \Omega$ at frequencies up to 100 kHz at the highest output power level ~~Class~~ that the PSE supports, as defined in Table 33–13. At lower power levels than the highest output power level PSE support, $Z_{out_ps_max} = 0.3\ \Omega \times P_{Class\ max} / P_{class}$.

Z_{o_ps} can be extracted from ~~Z_{port}~~ Z_{o_port} by measuring ~~$V_{Port-2P}$~~ $V_{Port_PSE-2P} / I_{Port}$ (with an external power dynamic analyzer system) as a function of frequency and subtracting from ~~Z_{port}~~ Z_{o_port} the value of Z_{o_ser} ~~Z_{ser} ($f=DC$)~~ which is limited by the value of ~~Z_{ser}~~ Z_{o_ser} at DC (low frequency).

- The value of Z_{o_ps} is not limited if the following conditions are met simultaneously:
 - a) ~~If~~ $Z_{o_ps} < Z_{o_ser}$

b) ~~and V_{pse} $V_{Port-2P}$ is kept to in the range of $V_{Port-2P} - V_{Port-PSE-2P_{min}}$ and $V_{Port-2P} - V_{Port-PSE-2P_{max}}$ as defined in Table 33–18 during dynamic load changes from 10 Hz to 100 kHz, then the value of $Z_{o_{ps}}$ is not limited.~~

Verification of these guidelines can be made by measuring the ~~PSE PI port~~ output impedance from 10 Hz to 100 kHz with the maximum load per the PSEs assigned Class, as defined in Table 33–13 at short cable length, or by performing simulations.

See Figure 33A–1 for the PSE-PD system impedance allocation.

2. Update Figure 33A-1 as follows:

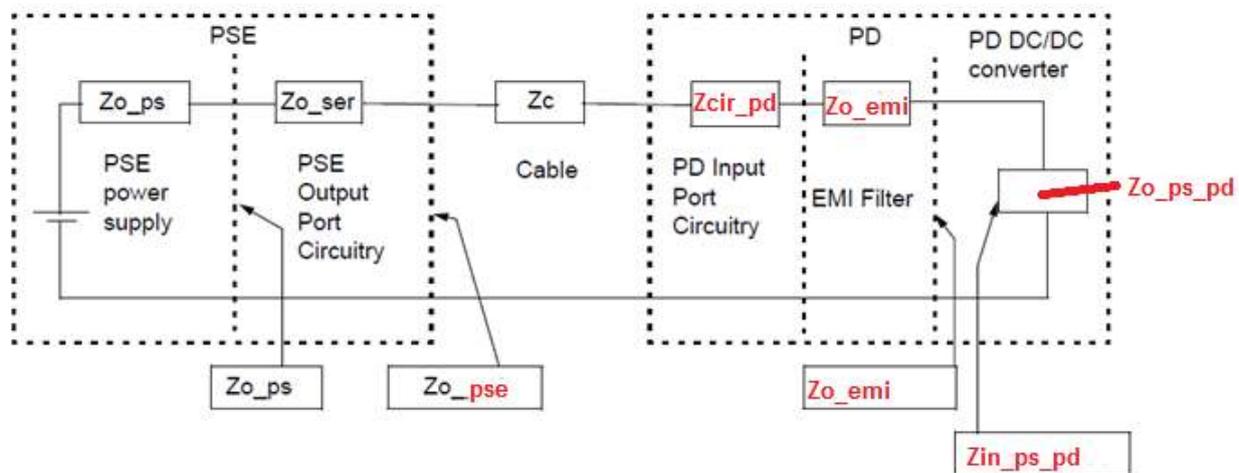


Figure 33A–1—PSE-PD system impedance allocation

~~See Figure 33A–2 for the test setup and Figure 33A–3 for the test requirements.~~

3. Delete Figure 33A-2 (no need to teach how to measure impedance of a port)
4. Delete Figure 33A-3 (the test requirements are in the text)
5. Make the following changes:

33A.2 Recommended PD design guidelines

PD ~~port-PI~~ input impedance consists of the following two parts:

— PD ~~PI port~~ input circuits Z_{cir_pd} and ~~including~~ the EMI filter (~~Z_{in_ser}~~) Z_{emi} , and

— PD power supply input impedance (~~$Z_{in_ps_pd}$~~), which is fed by the output of the EMI filter (~~Z_{o_emi}~~).

In order to maintain stability with the PSE, the PD power supply input impedance (~~$Z_{in_ps_pd}$~~) should be higher than the output impedance of the total network ~~that precedes it ($Z_{o_emi} + Z_{cir_pd} + Z_c + Z_{o_pse}$)~~, including the PD EMI output filter impedance fed by the channel output impedance, which is fed by the PSE port output impedance.

The worst-case scenario is when the channel length is zero (in terms of lower damping factor).

~~The a~~ Access to the PD input power supply is not possible through the PD port for evaluating the various impedances ~~in the PD~~ and derivation of the above ~~individual impedances~~ parameters. The following guidelines are recommended when measuring the PD input impedance:

— The PD power supply input impedance ($Z_{in_ps_pd}$) at ~~$P_{class_PD_max}$~~ max load of ~~$P_{port_PD} = P_{port_PD_max}$~~ as defined in Table 33–30 should be higher than 30 Ω at any frequency up to the PD power supply crossover ~~closed loop~~ frequency. If the PD power supply is consuming less than ~~its maximum power capability defined by $P_{class_PD_max}$, $P_{port_PD} = P_{port_PD_max}$~~ as defined in Table 33–30, then $Z_{in_ps_pd\ min} = 30 \times \frac{P_{class_PD_max}}{P_{port_PD_max}} \times \frac{P_{port_PD_max}}{P_{port_PD}}$.

— The PD power supply EMI filter output impedance should be $Z_{o_emi} = 2.7 \Omega$ max. If the PD power supply is consuming less than ~~$P_{class_PD_max}$ i.e. $P_{port_PD} = P_{port_PD_max}$~~ , then $Z_{o_emi} = 2.7 \times \frac{P_{class_PD_max}}{P_{port_PD_max}} \times \frac{P_{port_PD_max}}{P_{port_PD}}$.

See Figure 33A–1 for the PSE-PD system impedance allocation.

End of Baseline

The following is a clean version with out markups.

Replace 33A.1 and 33A.2 with the following:

PSE-PD stability

33A.1 Recommended PSE design guidelines and test setup

In order to prevent potential oscillations between the PSE and PD, the sum of the PSE port output impedance (Z_{o_pse}), the cable impedance (Z_c), the PD input port circuitry impedance (Z_{cir_pd}) and the PD EMI output filter impedance (Z_{emi}) should be lower than the PD power supply input impedance ($Z_{in_ps_pd}$). All the above impedances are converted to the equivalent series impedance form as described by Figure 33A-1.

PSE PI output impedance consists of two parts:

- PSE power supply output impedance (Z_{o_ps}), which is a function of the load at the PSE PI, and
- the series elements (Z_{ser}) that connect the PSE power supply output to the PSE PI.

Therefore, the total PSE PI output impedance during normal powering mode is
 $Z_{o_pse} = Z_{o_ps} + Z_{ser}$.

In order to maintain PSE-PD stability, the following guidelines apply:

- $Z_{o_ps\ max} = 0.3\ \Omega$ at frequencies up to 100 kHz at the highest output power level that the PSE supports, as defined in Table 33–13. At lower power levels than the highest output power level PSE support, $Z_{out_ps_max} = 0.3\ \Omega \times P_{Class\ max} / P_{class}$.

Z_{o_ps} can be extracted from Z_{o_port} by measuring $V_{Port_PSE-2P} / I_{Port}$ (with an external power dynamic analyzer system) as a function of frequency and subtracting from Z_{o_port} the value of Z_{ser} which is limited by the value of Z_{ser} at DC (low frequency).

- The value of Z_{o_ps} is not limited if the following conditions are met simultaneously:
 - a) $Z_{o_ps} < Z_{ser}$
 - b) V_{pse} is kept in the range of $V_{Port_PSE-2P\ min}$ and $V_{Port_PSE-2P\ max}$ as defined in Table 33–18 during dynamic load changes from 10 Hz to 100 kHz..

Verification of these guidelines can be made by measuring the PSE PI output impedance from 10 Hz to 100 kHz with the maximum load per the PSEs assigned Class, as defined in Table 33–13 at short cable length, or by performing simulations.

See Figure 33A–1 for the PSE-PD system impedance allocation.

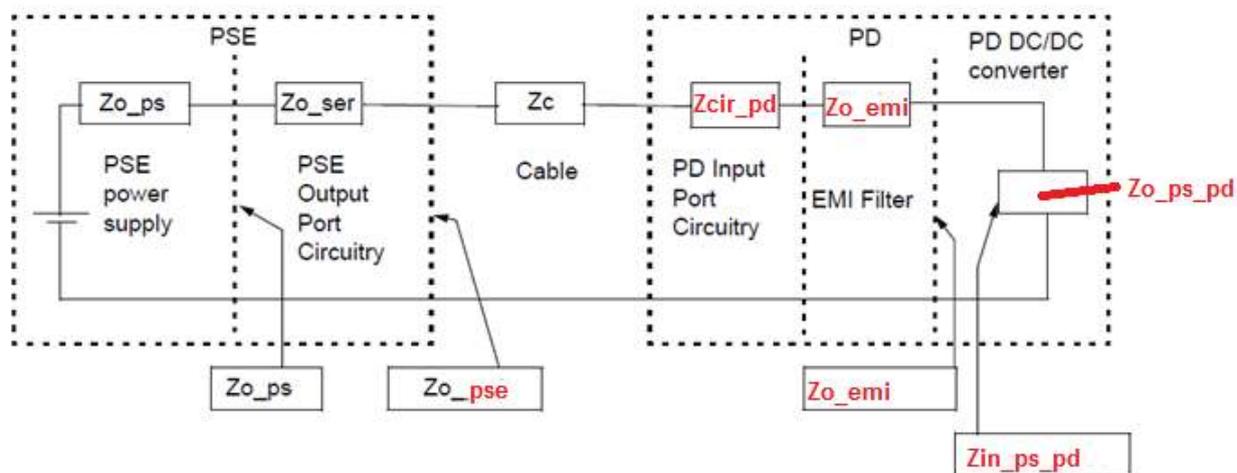


Figure 33A-1—PSE-PD system impedance allocation

33A.2 Recommended PD design guidelines

PD PI input impedance consists of the following two parts:

- PD PI input circuits Z_{cir_pd} and the EMI filter Z_{emi} , and
- PD power supply input impedance $Z_{in_ps_pd}$.

In order to maintain stability with the PSE, the PD power supply input impedance $Z_{in_ps_pd}$ should be higher than the output impedance of the total network that precedes it ($Z_{o_emi} + Z_{cir_pd} + Z_c + Z_{o_pse}$).

The worst-case scenario is when the channel length is zero (in terms of lower damping factor).

Access to the PD input power supply is not possible through the PD port for evaluating the various impedances in the PD and derivation of the above individual impedances. The following guidelines are recommended when measuring the PD input impedance:

- The PD power supply input impedance ($Z_{in_ps_pd}$) at $P_{class_PD_max}$ as defined in Table 33-30 should be higher than 30Ω at any frequency up to the PD power supply crossover closed loop frequency. If the PD power supply is consuming less than its maximum power capability defined by $P_{class_PD_max}$, as defined in Table 33-30, then $Z_{in_ps_pd} \min = 30 \times P_{class_PD_max} \max / P_{port_PD}$.
- The PD power supply EMI filter output impedance should be $Z_{o_emi} = 2.7 \Omega$ max. If the PD power supply is consuming less than $P_{class_PD_max}$ i.e. P_{port_PD} , then $Z_{o_emi} = 2.7 \times P_{class_PD} / P_{port_PD}$.

See Figure 33A-1 for the PSE-PD system impedance allocation.

End of Baseline