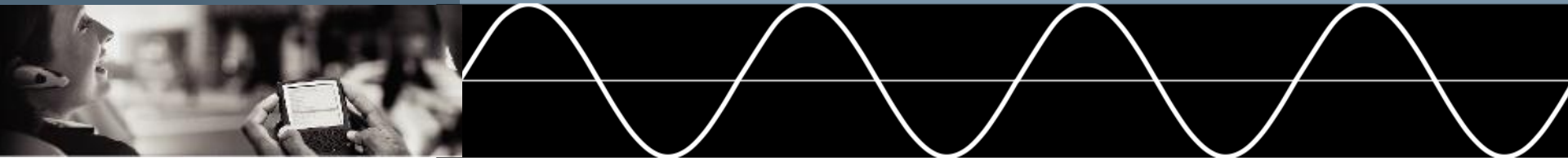# IEEE802.3bt

PD PI Current Definitions

J. Heath – Linear Technology

The PD PI is defined as all 8 conductors at the MDI

1.4.256 Medium Dependent Interface (MDI): The mechanical and electrical or optical interface between the transmission medium and the MAU (e.g., 10BASE-T) or the PHY (e.g., 1000BASE-T) and also between the transmission medium and any associated (optional per IEEE 802.3, Clause 33) Powered Device (PD) or Endpoint Power Sourcing Equipment (PSE).

1.4.324 Power Interface (PI): The mechanical and electrical interface between the Power Sourcing Equipment (PSE) or Powered Device (PD) and the transmission medium. In an Endpoint PSE and in a PD the Power Interface is the MDI.

33.3 Powered devices (PDs)

A PD is the portion of a device that is either drawing power or requesting power by participating in the PD detection algorithm. A device that is capable of becoming a powered device may or may not have the ability to draw power from an alternate power source and, if doing so, may or may not require power from the PI. PD capable devices that are neither drawing nor requesting power are also covered in this subclause.

A PD is specified at the point of the physical connection to the cabling. Characteristics such as the losses due to voltage correction circuits, power supply inefficiencies, separation of internal circuits from external ground or other characteristics induced by circuits after the PI connector are not specified. Limits defined for the PD are specified at the PI, not at any point internal to the PD, unless specifically stated.

PI Definition is all 8 wires, cannot require 4 pair power

33.3.1 PD PI

The PD shall be capable of accepting power on either of two sets of PI conductors. The two conductor sets are named Mode A and Mode B. In each four-wire connection, the two wires associated with a pair are at the same nominal average voltage. Figure 33–8 in conjunction with Table 33–13 illustrates the two power

Table 33–13—PD pinout

Conductor	Mode A	Mode B
1	Positive V_{PD}, Negative V_{PD}	
2	Positive V_P, Negative V_{PD}	
3	Negative V_{PD}, Positive V_{PD}	
4		Positive V_{PD}, Negative V_{PD}
5		Positive V_{PD}, Negative V_{PD}
6	Negative V_{PD}, Positive V_{PD}	
7		Negative V_{PD}, Positive V_{PD}
8		Negative V_{PD}, Positive V_{PD}

The PD shall be implemented to be insensitive to the polarity of the power supply and shall be able to operate per the PD Mode A column and the PD Mode B column in Table 33–13.

NOTE—PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that simultaneously require power from both Mode A and Mode B are specifically not allowed by this standard.

The PD shall not source power on its PI.

The PD shall withstand any voltage from 0 V to 57 V at the PI indefinitely without permanent damage.

57V on both Mode A and Mode B will not damage compliant PDs

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LINEAR
TECHNOLOGY

When Powered, the PD must Pollute Signature

- The current standard is clearly trying to prevent a PD from being powered on both Mode A and Mode B at the same time by compliant PSEs.

33.3.4 PD valid and non-valid detection signatures

A PD presents a valid detection signature while it is in a state where it accepts power via the PI, but is not powered via the PI per Figure 33–16.

A PD presents a non-valid detection signature at the PI while it is in a state where it does not accept power via the PI per Figure 33–16.

A Type 2 PD presents a non-valid detection signature when in a mark event state per Figure 33–16.

When a PD presents a valid or non-valid detection signature, it shall present the detection signature at the PI between Positive V_{PD} and Negative V_{PD} of PD Mode A and PD Mode B as defined in 33.3.1. When a PD becomes powered via the PI, it shall present a non-valid detection signature on the set of pairs from which it is not drawing power.

Maximum Permissible PD PI Power is 25.5W

33.3.7 PD power

The power supply of the PD shall operate within the characteristics in Table 33–18.

The PD may be capable of drawing power from a local power source. When a local power source is provided, the PD may draw some, none, or all of its power from the PI.

Table 33–18—PD power supply limits

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional information
1	Input voltage	V_{Port_PD}	V	37.0	57.0	1	See 33.3.7.1, Table 33–1
				42.5	57.0	2	
4	Input average power, Class 0 and Class 3	P_{Class_PD}	W		13.0	1	See 33.3.7.2, Table 33–1
	Input average power, Class 1				3.84	1	
	Input average power, Class 2				6.49	1	
	Input average power, Class 4				25.5	2	

Summary

- PD PI is all 8 wires, both Mode A and Mode B
- 57V on simultaneously on both Mode A and Mode B will not damage compliant PDs
- PD maximum power is 25.5W at the PI for compliant PDs
- The standard is clearly trying to prevent PSEs from powering both Mode A and Mode B at the same time (today).
  - We went to the trouble to pollute the signature
- 4 pair power to legacy PDs is
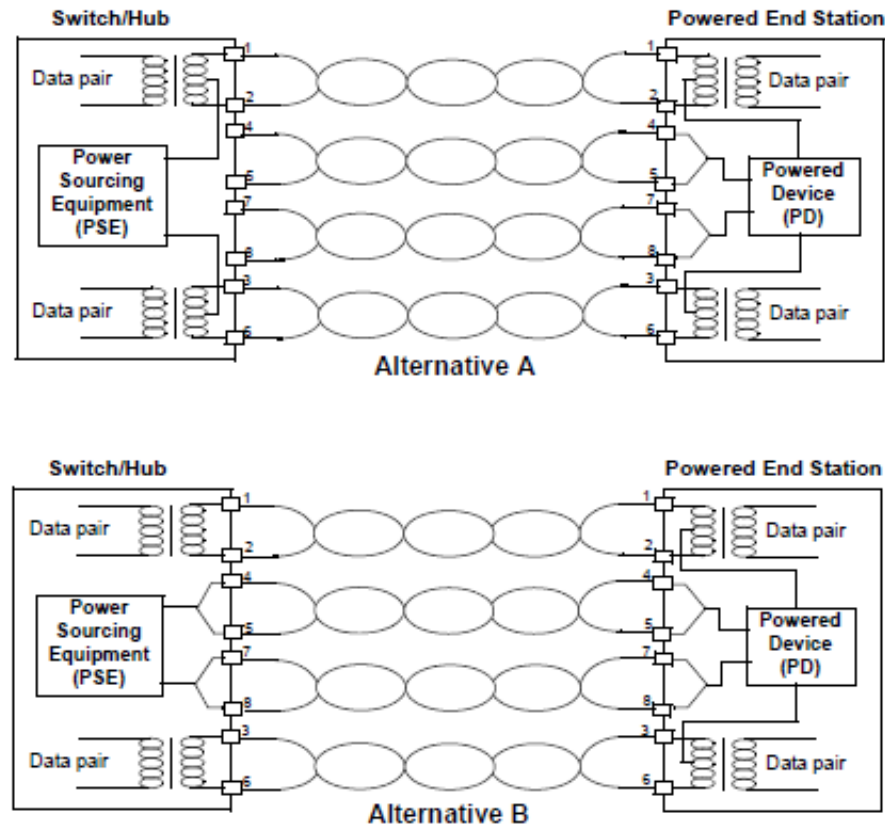 - Desirable
  - Safe

Appendix A

Figure 33–4—10BASE-T/100BASE-TX Endpoint PSE location overview