

# Extended Power baseline proposal

v150

[lennart.yseboodt@philips.com](mailto:lennart.yseboodt@philips.com)

[matthias.wendt@philips.com](mailto:matthias.wendt@philips.com)

[ydarshan@microsemi.com](mailto:ydarshan@microsemi.com)

Supporters: Sesa Panguluri, Koussalya Balasubramanian, Rick Frosch, Faisal Ahmad

# Terms

- $P_{\text{Class\_PD}}$  = PD maximum input average power per its class.
- $P_{\text{Class}}$  = PSE maximum power per  $P_{\text{Class\_PD}}$  at worst case channel DC resistance.

# Goal

Objective:  $P_{\text{Class}} - P_{\text{Class\_PD}}$  is power reserved for cable losses. The goal is to make this power available to the PD if it has additional information about actual channel losses. The amount of power available depends on actual channel losses.

Two things are needed:

- Table 33-18 Item 4 forbids PDs from exceeding  $P_{\text{class\_PD}}$
- An upper limit needs to be introduced

# Table 33-18 -- PD power supply limits

| Item | Parameter  | Symbol    | Unit | Min | Max  | PD Type | Additional information   |
|------|--|-----------|------|-----|------|---------|--------------------------|
| 4    | Input average power, Class 0 and Class 3         | PClass_PD | W    |     | 13.0 | 1       | See 33.3.7.2, Table 33-1 |
|      | Input average power, Class 1                     |           |      |     | 3.84 | 1       |                          |
|      | Input average power, Class 2                     |           |      |     | 6.49 | 1       |                          |
|      | Input average power, Class 4                     |           |      |     | 25.5 | 2       |                          |
|      | Input average power, Class 5                     |           |      |     | TBD  | 3       |                          |
|      | Input guaranteed available average power Class 6 |           |      |     | TBD  | 3       |                          |
|      | Input guaranteed available average power Class 7 |           |      |     | TBD  | 4       |                          |

Info: the highest power class for Type 3 and Type 4 is reworded to yield the same information but allow the PD to exceed the guaranteed available average power. The PD needs to know about actual channel losses, this is introduced in 33.3.7.2.

# 33.3.7.2 Input average power

## 33.3.7.2 Input average power

The maximum average power,  $P_{Class\_PD}$  in Table 33–18 or  $PDMaxPowerValue$  in 33.6.3.3, is calculated over a 1 second interval. PDs may dynamically adjust their maximum required operating power below  $P_{Class\_PD}$  as described in 33.6.

NOTE—Average power is calculated using any sliding window with a width of 1 s.

For Type 3 and 4 PDs the input guaranteed available average power is the maximum power the PD may consume when no additional information is available to the PD regarding actual channel DC resistance. If the PD has information about actual channel resistance then the PD may exceed the maximum guaranteed power provided that the  $I_{port}$  does not exceed  $P_{class}/V_{pse}$ .  $P_{class}$  is defined in Table 33-11.

Info: this sets the upper bound for PD consumption above the guaranteed power, expressed in the  $I_{port}$  current not to exceed the current the PSE minimally must be able to deliver.

# Annex 1-1

Q: How much power must a PSE minimally have available ?

|    |  |            |   |   |  |      |                            |
|----|--|------------|---|---|--|------|----------------------------|
| 11 | Continuous output power capability in POWER_ON state | $P_{Con}$  | W | $P_{Class}$                             |  | 1, 2 | See 33.2.7.10, Table 33-7. |
| 12 | PSE Type power minimum                               | $P_{Type}$ | W | $I_{Cable} \times (V_{Port\_PSE\ min})$ |  | 1, 2 | See 33.1.4.                |

Two answers:  $P_{Class}$  and  $P_{Type}$  (what is the difference between  $P_{con}$  and  $P_{type}$  ?)  
 $P_{Type}$  is eg. 30W for Type 2

# Annex 1-2

Table 33-7—Physical Layer power classifications ( $P_{Class}$ )

| Class | Minimum power levels at output of PSE ( $P_{Class}$ ) |
|-------|---|
| 0     | 15.4 Watts  |
| 1     | 4.00 Watts  |
| 2     | 7.00 Watts  |
| 3     | 15.4 Watts  |
| 4     | $P_{Type}$ as defined in Table 33-11                  |

NOTE 1—This is the minimum power at the PSE PI. For maximum power available to PDs, see Table 33-18.

NOTE 2—Data Link Layer classification takes precedence over Physical Layer classification.

$P_{Type}$  is 30W ( $I_{cable} * V_{PSE\ min}$ )

# Annex 1-3

The minimum power output by the PSE for a particular PD class is defined by Equation (33-3). Alternatively, PSE implementations may use  $V_{PSE} = V_{Port\_PSE\ min}$  and  $R_{Chan} = R_{Ch\ max}$  to arrive at over-margined values as shown in Table 33-7.

$$P_{Class} = \left\{ V_{PSE} \times \left( \frac{V_{PSE} - \sqrt{V_{PSE}^2 - 4 \times R_{Chan} \times P_{Class\_PD}}}{2 \times R_{Chan}} \right) \right\}_W \quad (33-3)$$

where

|                 |  |
|-----------------|--|
| $V_{PSE}$       | is the voltage at the PSE PI as defined in 1.4.413 |
| $R_{Chan}$      | is the channel DC pair loop resistance             |
| $P_{Class\_PD}$ | is the PD's power classification (see Table 33-18) |

Interpretation: a PSE may, if it knows  $R_{Chan}$ , set  $P_{class}$  anywhere between  $P_{Class\_PD}$  and  $P_{Type}$

**Q: How much power must a PSE minimally have available ?**

**Follow Eq. 33-3 or Table 33-7 ?**