Reconsideration of 100G-EPON FEC

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ZTE
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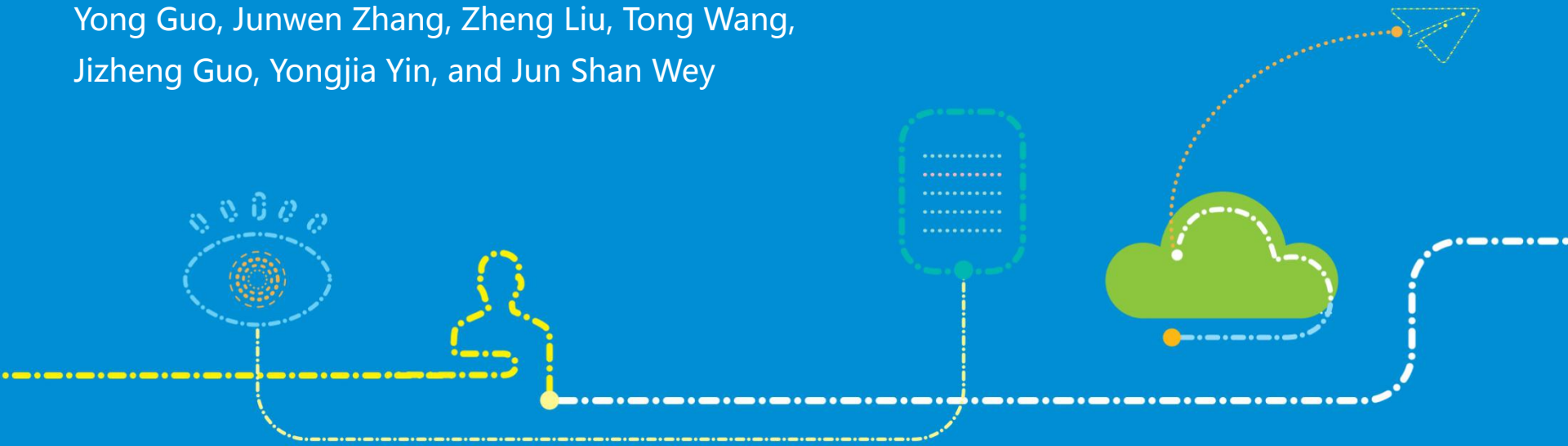


Motivation

- Both RS and LDPC codes providing higher coding gain have been proposed to close the optical power budget gap
  - Vanveen_3ca_1_0317: RS(1023, 847), OH=17.2%; RS(2047,1739), OH=15%
  - laubach_3ca_1_0517: LDPC(18493, 15677), code rate=84.7%
  - Jingyinrong_3ca_2_0717: LDPC 22*125*128, code rate=82.4%; LDPC 13*76*256, code rate=84.8%
- Concerns about LDPC code
  - Power budget gap
  - Error floor issue
  - CDR loss of lock
- If we can close the power budget gap using RS code, is it worth the risk of committing to LDPC for 25G?

What is the size of optical power budget gap?

- Size of the optical power budget gap will impact which FEC code should be used
  - 0.5 dB: harstead_3ca_5_0117, johnson_3ca_2_0117
  - 1.5 dB: guo_3ca_2_0517
  - 1-2 dB: laubach_3ca_1_0517
- Analysis in laubach_3ca_1_0517
  - Gap~ 1dB: RS with longer code word (e.g., 1KB) could work
  - Gap~ 2dB: LDPC (e.g., 2KB) could be useful

Improvement of transceivers to close the gap

- Minimum 25G Tx optical power by 2020:
  - Yields and cost will be improved by the time of commercialization

	Cooled DML	Uncooled DML	EML
liudekun_3ca_4_0517	> 4 dBm	> 4 dBm	3-4 dBm
harstead_3ca_1a_0716	7 dBm	6.5 dBm	5 dBm

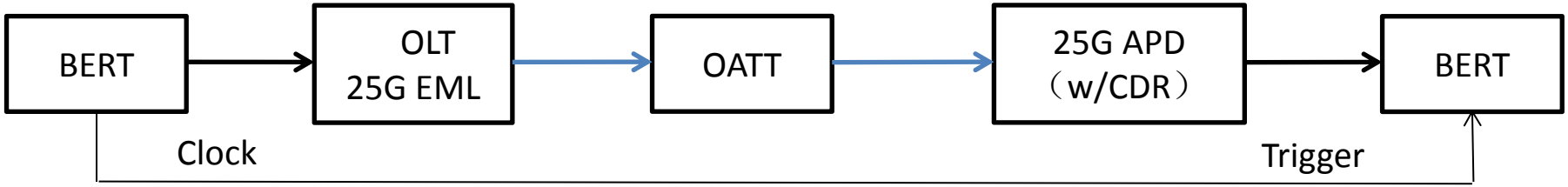
- Receiver sensitivity
  - Starting point is -24.2 dBm at 1E-3 and 8 dB ER (harstead_3ca_4_0117)
  - Potentially -28dBm (pan_3ca_1_0916, pan_3ca_1_0916)
  - Further improvement proposals see guo_3ca_1_0917

Loss budget is 28.2 dB with Tx power at +4 dBm and Rx sensitivity at -24.2 dBm
→ ~ 2 dB gap in optical power budget

Error floor issue in LDPC

- Error-floor is a challenging problem of LDPC and is still an open question
  - Error floor of LDPC codes is dominated by sub-structures in the Tanner graph. Girth, stopping sets, trapping sets, and decoding algorithm, can significantly affect error floor of LDPC
  - Error floor could be anywhere between 1E-2 to 1E-12: an open issue to clarify
- Only one existing proposal has shown no error floor above 1E-14:
  - laubach_3ca_1_0517 shows no results below 1E-12
  - zhao_3ca_1_0517 shows no error floor above 1E-14
- Simulation results are not sufficient for error floor estimation, because no theoretical tool is available to accurately predict the error floor of LDPC codes
- FPGA-based verification is needed to verify LDPC error floor

Burst mode CDR loss of lock not yet confirmed



Test Setup

- TX: 1310nm EML with ER: 8dB@PRBS31
- RX: 25G ONU RX (APD ROSA) with CDR
- CDR Loop Bandwidth is set to 10MHz or 20MHz

Test Result

- 25G CDR can work in the lock state at BER 1E-2 with loop bandwidth of 10MHz and 20MHz
- 25G CDR loses the lock state at BER below 3E-2

Summay and Proposal

- There are still several FEC questions to be answered before making a code selection
  - Error floor below 1E-12 is not verified in hardware (FPGA)
  - Burst-mode operation of LDPC code is not yet proven. CDR is verified only in continuous mode
  - 2-5x increase in complexity comparing to RS code
- Power budget gap can be closed optically to within the range for RS codes
- We propose to
  - Use RS code for 25G-EPON (power budget proposal see guo_3ca_1_0917)
  - Further study of LDPC code for 50G/100G-EPON

Thank you

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