IEEE 802.3 10Mb/s Backplane Ethernet Call For Interest Consensus Presentation

Orlando, FL Nov 9th-12th, 2017

Today's presentation

Presenters and Contributors:

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¹⁾ Full Affiliations listed in "Contributors and Supporters"

Agenda

Overview Discussion

Jon Lewis, Dell EMC

Presentations

10BP in Servers

10BP in Switches

10BP Technical Feasibility

– 10BP Why Now?

Q&A

Straw Polls

Jon Lewis, Dell EMC

Amrik Bains, Cisco

Mandeep Chadha, Microsemi

George Zimmerman, CME¹

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CFI Objectives

- To gauge the interest in studying 10Mb/s Backplane Ethernet
- We do not need to:
 - Fully explore the problem
 - Debate strengths and weaknesses of solutions
 - Choose a solution
 - Create a PAR or 5 Criteria
 - Create a standard
- Anyone in the room may vote or speak

Overview: About 802.3cg/10SPE

- Single pair connection
- Low cost/data rate suitable for sensors
- Supports power and data
- Supports multiple reaches (e.g. 15m, 1000m, etc.)
- Supports Point-to-Point and Multi-Drop
- Targets Automobile, Industrial and Building Automation
 - Addressing installed cable base in Industrial and Building Automation

Overview: Intra-system Management Interface

- Internal serial control interfaces are common in servers/switches.
- They form a high percentage of design/debug/support issues.
- 10BP (10 Mb/s Single Pair Ethernet on the backplane) could consolidate a number of commonly used interfaces (e.g., I2C/SMBus, MDIO).
- Systems shipping in 10s of millions annually, each contain many of these interfaces.
- Implementations using FPGAs or micro controllers could support a "faster & richer" interface, and be easier to debug using standard Ethernet tools.
- "Backplane" includes a variety of physical transmission elements (e.g. PCB traces, connectors,)

Intra-system Management Interface

- This is used to perform configuration/monitoring of components in Servers/Switches
- Many different components with various management interfaces
- > I2C/SMB Bus
 - Optical Module, AC/DC Power Supplies, FAN Control, DC-DC Converters, Temp monitors, EPROM etc....
 - > 2 wire Clock + Shared Data (Tx/Rx)
 - Clock speed 100KHz, data BW (25 to 30Kb/s) limited due half-duplex and protocol overhead
- > UART: Universal Asynchronous Rx/Tx
 - > Micro-controllers/CPU: Console port
 - > 2 wire Rx/Tx
 - > 9.6Kb/s 115Kb/s

- MDIO (IEEE 802.3 Clause 22/45): Copper PHYs and Fiber PHYs
 - > 2 wire
 - > Tx/Rx shared (half-duplex)
 - Max specified MDC clock of 2.5MHz (avg. BW 1Mb/s)
- > SPI:
 - > SD card, Sensors, eMMC
 - Minimum of 4 wire Clock, Rx, Tx and Save Select (when multiple devices connected to same data pins)
 - > Typically 12 to 25Mb/s
 - > More data wires can be used for higher bandwidth

Management Interfaces have not kept up with BW requirements

Different Software Drivers for each interface type

Why NOT use current IEEE-10BASE-T/10BASE2?

- 10BASE-T
 - Does not support FULL-Duplex over a single-pair (2 pins)
- 10BASE2:
 - Does not support FULL-Duplex
 - AC signal + DC offset, shielded media required to avoid EMC not suitable for backplane
 - "This MAU is not recommended for new installations. Since September 2011, maintenance changes are no longer being considered for this clause."

Common set of Technology issues with current Interfaces

- High voltage I/O: 2.5/3V
 - Harder to implement as silicon technology shrinks to nm
 - Cross-talk Impacts high speed signals running at 10G and higher data rates
- I2C/10BASE2 are non-differential
 - Creates EMC issues

Using 2 pins provides significant cost benefits, and minimizes disruption to system design

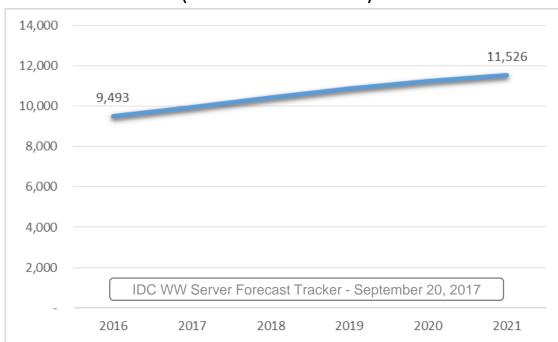
10BP in Servers

Jon Lewis, Dell EMC

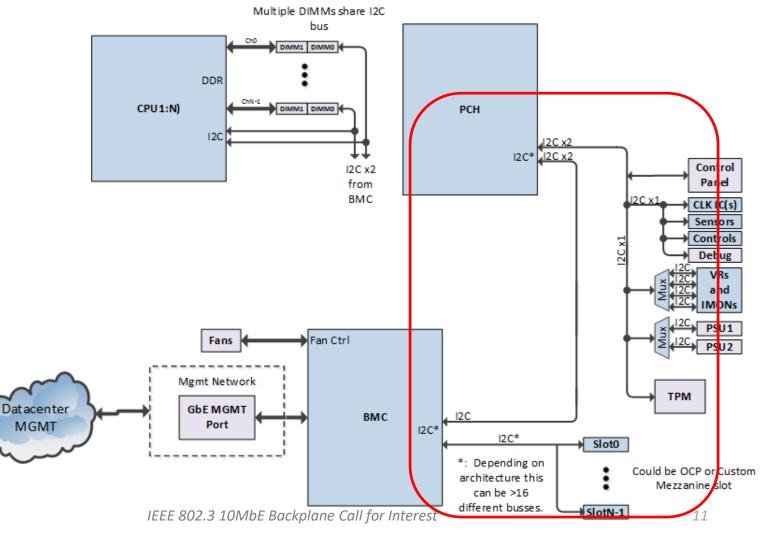
Server Market size info

- Total endpoint device >200 million parts per year
 - >20 endpoints per Server
- Total switch device >10 million per year
 - ~1 switch per Server
- Per year
 - 200 million endpoints
 - 10 million switches

WW 2017Q2 <u>x86</u> Server <u>Annual Unit</u> Forecast (units in thousands)



Server: Current



DIMM1 DIMM0 Server: DDR Likely some of these would be connected through bridging **Future** DIMM1 DIMMO CPU1:N) devices either in the switch or stand-alone devices Control CLK I C(s) Sensors IEEE 802.3cg Ethernet Controls Connections Debug Fans Switch PSU 1 Mgmt Network Datacenter GbE MGMT **BMC** MGMT Port Slot0 Could be Standard PCIe slot, OCP or other custom Mezzanine slot Nov 2017 IEEE 802.3 10MbE Backplane Call for Interest SlotN-1 12

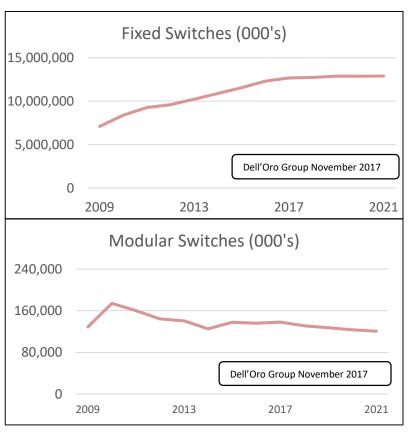
10BP in Switches & Other Backplanes

Amrik Bains, Cisco

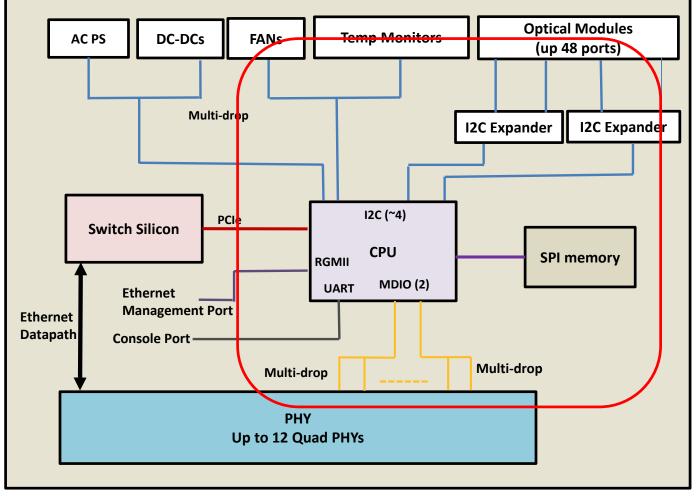
Switch market size info

- Switch Market units per year*
 - fixed ~13 million units per year
 - modular ~140 thousand units per year
- Average number of devices in
 - fixed ~20 endpoints, ~2 switches
 - modular ~60 endpoints, ~8 switches
- Total devices per year
 - endpoints >268 million
 - switches >27 million

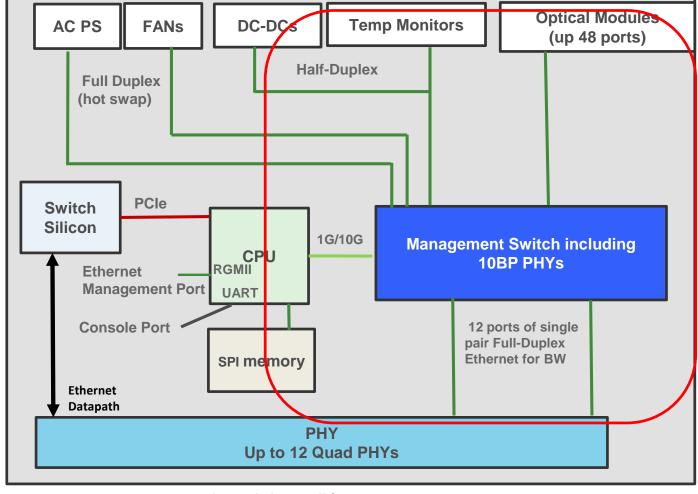
*Derived from market data on ports assuming average of 40 ports per unit for Fixed switches 168 port per chassis for Modular switches



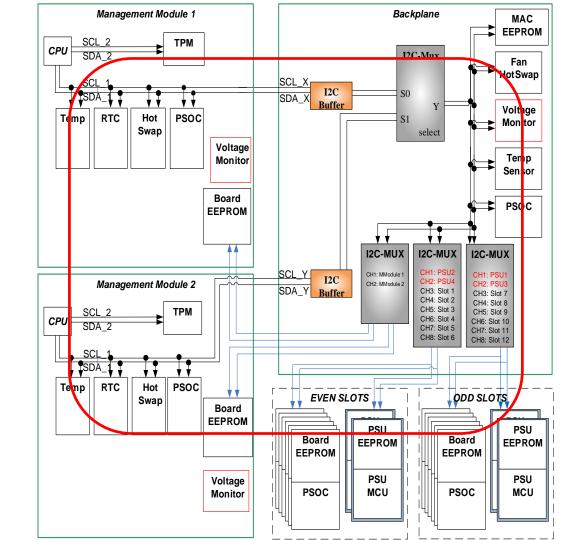
Fixed Switch: Current



Fixed Switch: Future



Modular Switch: Current



Slide: David Tremblay, HPE

Nov 2017

Modular Switch: Future

Management Module 1 Backplane 1G/10Gbps CPU 10Mbps MAC Management Switch **EEPROM** TPM RTC PSOC Fan Temp Hot 10Mbps **HotSwap** Swap 10Mbps Voltage Management Monitor Switch Voltage Board Monitor EEPROM 10Mbps Temp Sensor 10Mbps 10Mbps **PSOC** Management Module 2 1G/10Gps CPU TPM 10Mbps 10Mbps Management Switch PSOC Temp RTC Hot **EVEN SLOTS** ODD SLOTS Swap PSU **PSU** Board **Board EEPROM EEPROM EEPROM EEPROM** Voltage Board Monitor **EEPROM PSU** PSU **PSOC** MCU **PSOC** MCU

Slide: David Tremblay, HPE

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Industrial Backplane

Applications

Current Solutions

- □ Application areas are Factory Automation and Machine Control
- Programmable Logic Controllers (PLC) backplane

PCB backplane that is connectorized, usually mounted on metal plate
Power Supply
CPU / Controller is master of the PLC

backplane Local PLC rack IO: E.g. Analog In, Analog Out, Digital In, Digital Out, Relay, speciality, ..

☐ Remote I/O Islands

Two Flavors: Remote IO and Distributed IO Remote – IO Controller by main PLC Distributed – local "Comm Head" module controls the IO

Custom – ASICs / Legacy Systems

- such as Modicon Quantum, or Premium
- Dual Port RAM
- Token based
- CAN at 1 Mbit/Sec

100 MbE and 1GbE Ethernet with Copper PHYs (8 pins)

- such as Schneider's Modicon M580 ePAC
- Higher End PLCs Not 10BP candidate

Future Solutions with 10BPE

10BPE could enable migration from custom/CAN based backplane for lower cost PLC and IO islands

Low cost IO modules both in PLC rack and IO islands need to use very low cost microprocessors in the \$1-\$2 range that have 10Meg MACs

Why 10BP?

- Ecosystem complexity reduction:
 - Standard Ethernet driver instead of many custom serial interface drivers reduces coding and validation.
- Provide a standard ubiquitous management communication path.
- Same number of pins as existing interfaces, while increasing functionality.
- As compute and network nodes "converge" there is a fine line between the server and the network
- Automated alert support is more robust than multi-master SMBus.
 - Reduces the need for Software Polling

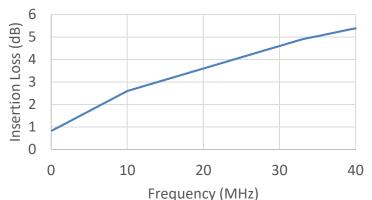
10BP Technology Feasibility

Mandeep Chadha, Microsemi

Lengths/link segment

- IEEE 802.3cg has a short reach link segment adopted
 - Based on cabling and connector measurements
- Consistent with needs of "backplane" channels

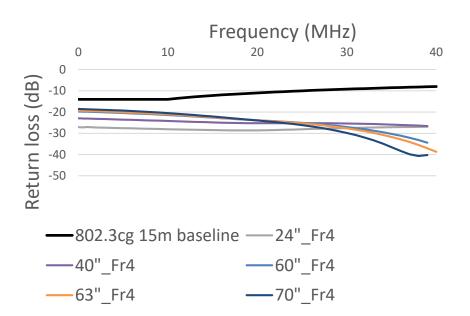
IEEE P802.3cg 15m Link Segment



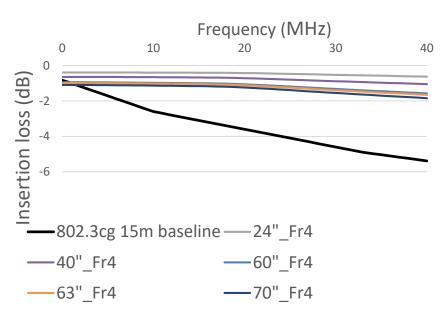
 Adopt the equations on slide 18 of <u>http://www.ieee802.org/3/cg/public/Sept2017/DiBiaso_Bergner_01c_0917.pdf</u> as a baseline for the 10SPE short reach link segment.

IL <	1+1.6(f-1)/9 dB 2.6+2.3(f-10)/23 dB 4.9+2.3(f-33)/33 dB	f=0.3 10 MHz f=10 33 MHz f=33 40 MHz
RL>	14 dB 14-10*log10(f/10) dB	f=0.3 10 MHz f=10 40 MHz
MC >	30 dB 30-20log10(f/20) dB	f=0.3 20 MHz f=20 200 MHz

Example "Backplane" channel characteristics



No issues with meeting proposed 10SPE Return Loss specifications



Insertion Loss spec proposed for 10SPE can be met for channels up to 40" FR4

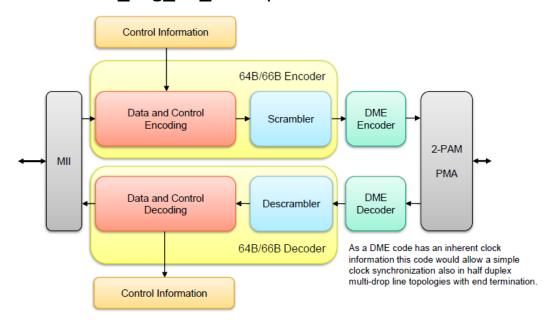
10Mb/s Ethernet in Micros/FPGAs

- Low insertion loss of channel gives lots of choices
- Many encoding types available
 - Differential Manchester, NRZ, etc.
 - All are low-complexity and have been implemented in FPGA format
- Duplexing method is new for micros/FPGAs
 - E.g., echo-cancelled full-duplex or half-duplex on medium
 - Being considered for short-reach channel in P802.3cg

10BP Complexity Estimate

- Proposals under consideration for PHY implementations of short-reach 10SPE use easily realizable analog and digital circuits using standard logic processes
- PMA
 - Differential line driver, analog hybrid/EC, clock sync
- Digital
 - TX PCS, Scrambler, Encoder
 - RX Decoder, Descrambler, PCS
- Construct as a macro that can be instantiated in ASIC or FPGA

10SPE short reach PHY proposal in slide 16 of Graber 3cg 12 0717.pdf



10BP - Why Now?

George Zimmerman, CME

Why Now?

- Interest from Network Equipment and Computer OEMs has created the potential for large volume short-reach interconnects
- Leverage investment in standardization of 10Mbps single-pair technology
 - Relevant PHY experts are gathered in IEEE 802.3cg
 - While 10Mbps Ethernet systems are old hat, there aren't any single-pair versions standardized
 - Open and common interoperable specifications simplify the market
 - Requirements and needs are consistent with 802.3cg short-reach objective
- Every time I turn around, there's a new application being proposed
- BUT: Existing 802.3cg project documentation is specific to "single balanced twisted pair copper cabling"

The Rub: 802.3cg PAR Scope, very specific

5.2.b. Scope of the project: Specify additions to and appropriate modifications of IEEE Std 802.3 to add 10 Mb/s Physical Layer (PHY) specifications and management parameters for operation, and associated optional provision of power, on single balanced twisted-pair copper cabling.

- Limitations: PHY & optional powering project, Rate = 10Mbps
- The medium is <u>single balanced twisted-pair copper cabling</u>
 - 2-pair, 4-pair, PCB backplane, parallel pairs, single ended are out of scope
- The Physics: addressing backplane applications is a natural
 - Including PCB "pairs": The electrons don't care about twisting the wires or read PAR documents...
- A standard can fill a broader need with 802.3cg solutions, avoiding proprietary extensions

802.3cg Supports Backplane Use Cases

Motion #15

- Move that the 802.3cg Task Force supports the inclusion of in-system use cases, as described in bains_lewis_10spe_01a_0910.pdf, subject to a successful CFI and Study Group outcome.
- M: P. Jones S:R. Naismith
- Procedural > 50%
- Y:30 N: 0 A:0
 - Motion Passes

Going Forward

- Study group could propose PAR/CSD modifications for 802.3cg
 - Expect most work could be done quickly, by close of January meeting
 - Study group could pre-discuss modifications of 802.3cg objectives
 - Target approval of modified P802.3cg project documentation March 2018
- P802.3cg continues its work on short-reach and long reach PHYs
 - 10BP contributors work offline to prepare and build consensus
 - Fold in required changes to support 10BP before May WG ballot milestone
- We've seen this before adding 25GBASE-T to 40GBASE-T IEEE P802.3bq, adding 200G to 802.3bs.
- Simpler than adding a speed:
 - NO new PHY
 - NO new MAC interface
 - NO new lane definition

Q&A

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Straw Polls

Straw Poll 1

Should a study group be formed for "10Mb/s Backplane Ethernet"?

• Y: N: A:

Room count:

Straw Poll 2

I would participate in a "10Mb/s Backplane Ethernet" study group in IEEE 802.3

Tally:

Straw Poll 3

My company would support participation in a "10Mb/s Backplane Ethernet" study group

Tally:

Future Work

Ask 802.3 at Thursday's closing meeting to form study group

- If approved:
 - 802 EC votes on Friday to approve the formation of the study group
 - First study group meeting would be during the January 2018 802.3 interim meeting (in Geneva)

End