147. New text and table to be inserted as per comment #91 on 802.3cg d2.3 (corrected proposal, rev2)

The PHY shall comply with the timing requirements specified in Table 147–1.

Table 147–1—10BASE-T1S delay constraints

Event	Minimum value	Maximum value	Unit of measure	Input timing reference	Output timing reference
TX_EN sampled to MDI output	120	440	ns	Rising edge of MII_TXCLK	First DME clock transition at the MDI
TX_EN sampled to CRS asserted	0	1040	ns	Rising edge of MII_TXCLK	Rising edge of CRS
TX_EN sampled to CRS deasserted	880	1920	ns	Rising edge of MII_TXCLK	Falling edge of CRS
MDI input to CRS asserted	400	1040	ns	First DME clock transition at the MDI	Rising edge of CRS
MDI input to CRS deasserted	640	1120	ns	Last DME encoded zero clock transition at the MDI	Falling edge of CRS
COL input to CRS asserted	0	25.6	µs	Start of corrupted transmitted signal at the MDI	Rising edge of CRS
COL input to CRS deasserted	0	3.2	µs	End of transmission at the MDI	Falling edge of CRS
MDI input to RX_DV asserted	2.4	4	µs	First DME clock transition at the MDI	Rising edge of RX_DV
MDI input to RX_DV deasserted	640	1900	ns	Last DME encoded zero clock transition at the MDI	Falling edge of RX_DV