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IEEE 802.3cg

PCLA Timings

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Background

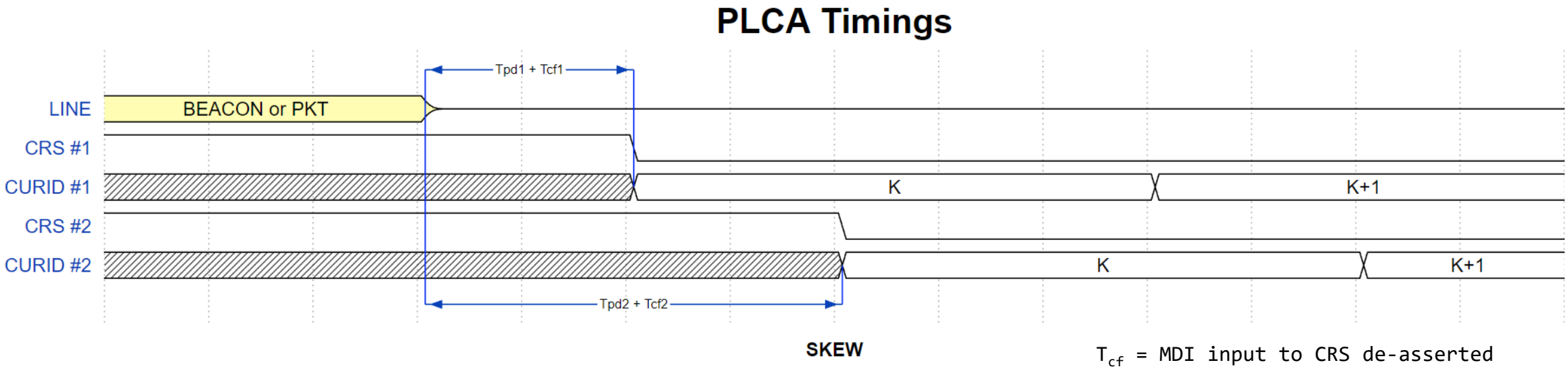
- Supporters
  - Tim Baggett (Microchip)

- Comments:
  - i-191 (Tim Baggett)
  - i-320 (Tim Baggett)

Outline

- Under any circumstance, a packet sent by a node during its own TO shall be received by any other node within the corresponding TO boundaries.
  - This shall take into account both the line propagation delay (T_{pd}) and the PHY internal delays, that is CRS rise/fall latency (T_{cr} / T_{cf}) and transmit latency (T_{tx}).
- This is very similar to the setup/hold requirements of any synchronous digital system
- A violation of these requirements would result in possible physical collisions on the line

TO skew



T_{cf} = MDI input to CRS de-asserted
T_{pd} = propagation delay on the line

$$T_{sk} = \left(T_{pd2} - T_{pd1}\right) + \left(T_{cf2} - T_{cf1}\right)$$

$$\min T_{pd} = 0 \ (nodes\ close\ to\ each\ other)$$

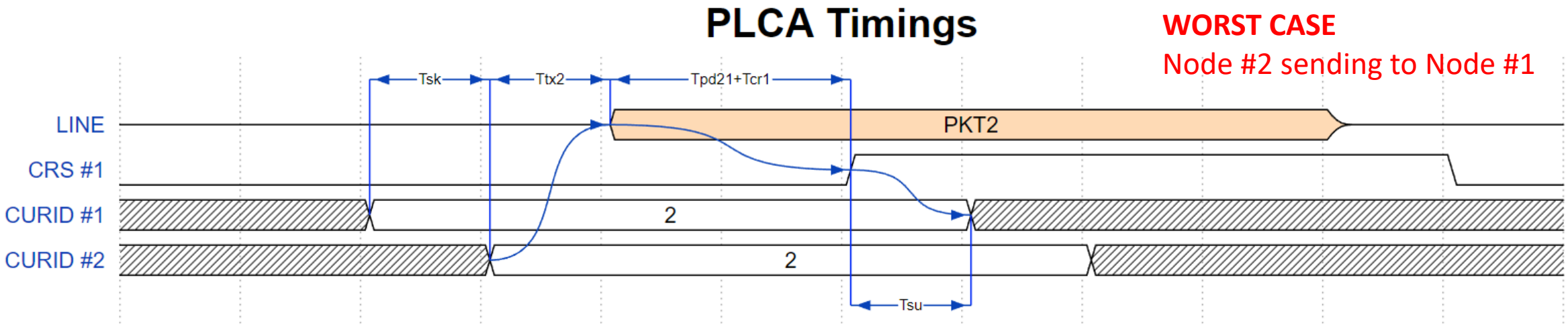
$$\max T_{pd} = \sim 200ns = 2 \text{ BT } (25 \text{ mt cable } @8\frac{\text{ns}}{\text{m}}, \text{reasonable worst case for UTP cables})$$

Minimum skew (min T_{sk}) is 0 (nodes close to each other, same CRS falling time)

Maximum skew (max T_{sk}) is delta T_{pd} (time distance between nodes) + max T_{cf} - min T_{cf}

Note: max skew can be negative but this is equivalent as swapping nodes #1 and #2, therefore we define it as positive in this presentation

Setup requirement



WORST CASE

Node #2 sending to Node #1

SETUP REQUIREMENT

$$T_{su} = TO_{timer} - \left(T_{sk} + T_{tx2} + T_{pd12} + T_{cr1}\right)$$

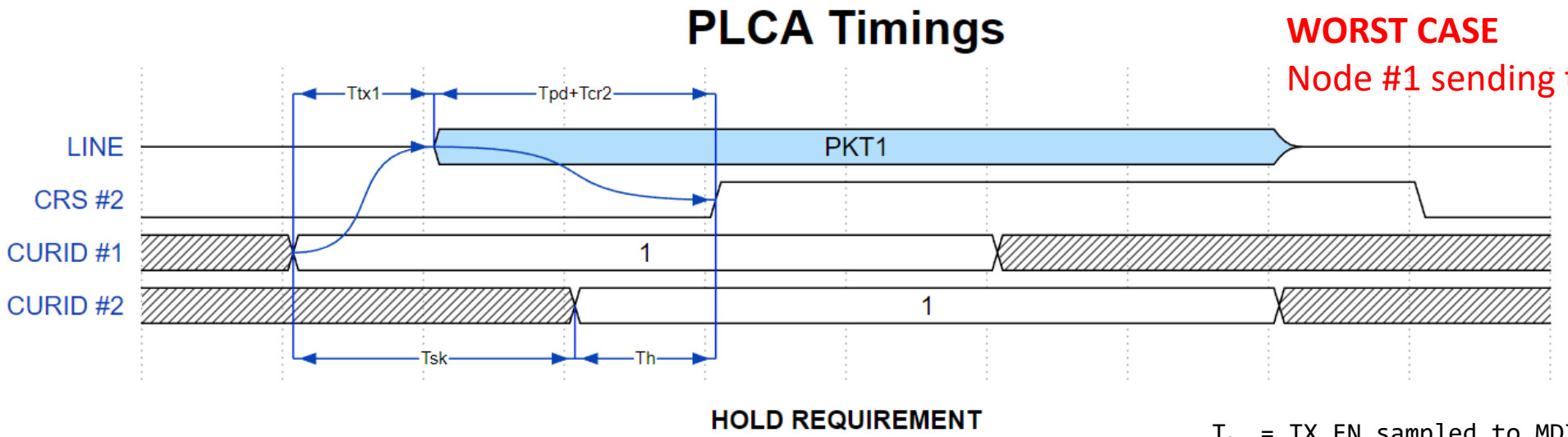
$T_{su} > 0$ to meet the TO

T_{tx} = TX_EN sampled to MDI output
T_{cr} = MDI input to CRS asserted
T_{cf} = MDI input to CRS de-asserted

Worst case T_{su} is for max T_{sk}, max T_{tx}, max T_{pd} and max T_{cr} which gives:

Eq. 1: $\max T_{tx} + \max T_{cr} + \max T_{cf} - \min T_{cf} < TO_{timer} - 2 \max T_{pd}$

Hold requirement



WORST CASE

Node #1 sending to Node #2

T_{tx} = TX_EN sampled to MDI output
T_{cr} = MDI input to CRS asserted
T_{cf} = MDI input to CRS de-asserted

$$T_h = T_{tx1} + T_{pd} + T_{cr2} - T_{sk}$$

$T_h > 0$ to meet the TO

Worst case T_H is for min T_{tx}, min T_{pd}, min T_{cr} and max T_{sk} (calculated for min T_{pd}) which gives:

Eq. 2: $\min T_{tx} + \min T_{cr} + \min T_{cf} - \max T_{cf} > 0$

10BASE-T1S timings

Table 147–6—10BASE-T1S delay constraints

Event	Minimum value	Maximum value	Unit of measure	Input timing reference	Output timing reference
TX_EN sampled to MDI output	120	440	ns	Rising edge of MII_TXCLK	First DME clock transition at the MDI
TX_EN sampled to CRS asserted	0	1040	ns	Rising edge of MII_TXCLK	Rising edge of CRS
TX_EN sampled to CRS deasserted	880	1920	ns	Rising edge of MII_TXCLK	Falling edge of CRS
MDI input to CRS asserted	400	1040	ns	First DME clock transition at the MDI	Rising edge of CRS
MDI input to CRS deasserted	640	1120	ns	Last DME encoded zero clock transition at the MDI	Falling edge of CRS
COL input to CRS asserted	0	25.6	µs	Start of corrupted transmitted signal at the MDI	Rising edge of CRS
COL input to CRS deasserted	0	3.2	µs	End of transmission at the MDI	Falling edge of CRS
MDI input to RX_DV asserted	2.4	4	µs	First DME clock transition at the MDI	Rising edge of RX_DV
MDI input to RX_DV deasserted	640	1900	ns	Last DME encoded zero clock transition at the MDI	Falling edge of RX_DV

- To guarantee PLCA RS interoperability, the setup/hold requirements has to be met assuming the worst case PHY timings
- Substituting Table 147-6 values in Equations 1 and 2 (slides 4, 5)
- HOLD check:
  $120ns + 400ns + 640ns - 1120ns > 0$

  → $40ns > 0$ (OK)

- SETUP check:
  $440ns + 1040ns + 1120ns - 640ns < TO_{timer} - 400ns$

  → $To_{timer} > 2360ns$ (23.6 BT)

Conclusion

- TO_{timer} is configurable but its default value is 20 BT
- To guarantee plug & play PLCA operation the default value should be set to 24 BT
- Proposed text change:

30.3.9.2.5 aPLCATransmitOpportunityTimer

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
This value is assigned to define the time between PLCA transmit opportunities for the node. aPLCATransmitOpportunityTimer maps to the duration of the timer to_timer. The value of aPLCATransmitOpportunityTimer represents the duration of to_timer in bit times. Valid range is 1 to 255, inclusive. The default value is ~~20~~ 24. See 148.4.5.4.;

THANK YOU!