OAM Status Bytes History

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Answer to Comment #2

BASE-T1 OAM Origination

- 1000BASE-T1, Clause 97, included an OAM Frame

	D8	D7	D6	D5	D4	D3	D2	D1	D0
Symbol 0	Even Parity	Reserved	Reserved	Reserved	Reserved	PingRx	PingTx	SNR<1>	SNR<0>
Symbol 1	Odd Parity	Valid	Toggle	Ack	TogAck	Message_Number<3:0>			
Symbol 2	Odd Parity	Message<0><7:0>							
Symbol 3	Odd Parity	Message<1><7:0>							
Symbol 4	Odd Parity	Message<2><7:0>							
Symbol 5	Odd Parity	Message<3><7:0>							
Symbol 6	Odd Parity	Message<4><7:0>							
Symbol 7	Odd Parity	Message<5><7:0>							
Symbol 8	Odd Parity	Message<6><7:0>							
Symbol 9	Odd Parity	Message<7><7:0>							
Symbol 10	Odd Parity	CRC16							first bit
Symbol 11	Odd Parity	final bit	CRC16						

Figure 97–15—OAM Frame

BASE-T1 OAM Definition

- OAM implementation is optional
- If implemented, some functionality was required
- Mechanism provided for user specific messaging

BASE-T1 OAM Additions

- OAM is still optional
- The definition for Symbol 0 through Symbol 9 has not changed for bits D0 through D7
- The definition of bit D8 has changed and bit D9 has been added for MultiGBASE-T1 as it uses a 10-bit RS-FEC
- P802.3ch is adding additional OAM Symbols to enable PHY status sharing with the link partner

BASE-T1 OAM Additions

- Additional OAM bytes are needed for functions that require confirmation of communication availability
- While implementation is not mandatory, there is a desire to have these implemented as defined

Comment on D2.0

- Comment: I am very confused why an informative annex would have state diagrams that describe the required behavior of the OAM functions needed for the operation of the link
- Proposed Change: Seems like this annex ought to be normative

149B Informative Annex History

- The state diagrams that show the handshaking to clear the REC were implemented in D1.1
- As a result of comment resolution on D1.1, it was decided to move the definition of the additional OAM bytes to an Informative Annex
- Comment 57 Straw Poll - Chicago rules
  - 1. Change the appropriate bits to RO and add the specific usage definitions in Clause 45: 1
  - 2. Keep the bits R/W and move the content of 149.3.8.2.11 into an informative annex with appropriate linking language: 13
  - 3. Add a note in 45.2.3.7.6 that these bits can be set by the PHY. If this is the case, the bits that are set by the PHY should not be written to.: 2
- Some content was moved for D1.2 (149.3.9.2.12), but the content in 149.3.8.4 was not. Comment #20 on D1.2 moved the rest of the content to Annex 94B
- This included the state diagrams as we wanted to keep all of this definition together

Backup

OAM Symbol 10

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	Status Valid	Power Supply warning	PHY internal temp warning	No MAC messages warning	Degraded link segment	Pair swapped	Clear REC	REC Cleared

This status symbol provides information on potential issues recognized by the PHY that may impact the PHY/Frame performance. Each status bit shall be updated to reflect the current PHY status.
Specific usage shown below defined in Informative Annex.

- Status Valid: Sent as 1 if the remaining bits are valid, sent as 0 if any bit is not valid
- Power Supply warning: Sent as 1 if the PHY power supply(s) is near the limit, otherwise sent as 0
- PHY internal temperature warning: Sent as 1 if the PHY internal temperature is near the shutdown temperature, otherwise sent as 0
- No MAC messages warning: Sent as 1 if there are no messages from MAC, otherwise sent as 0
- Degraded Link Segment: Sent as 1 if there is a potential issue with the link segment, otherwise sent as 0
- Pair swapped: Sent as 1 if the + and – signal lines are swapped, otherwise sent as 0
- Clear REC: Sent as 1 if REC<15:0> should be cleared, otherwise sent as 0
- REC Cleared: Sent as 1 if REC<15:0> has been cleared, otherwise sent as 0

OAM Symbol 11

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0

This symbol is reserved for future use.

OAM Symbols 12&13 Proposal

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Symbol 12	0	1	REC<15>	REC<14>	REC<13>	REC<12>	REC<11>	REC<10>	REC<9>	REC<8>
Symbol 13	0	1	REC<7>	REC<6>	REC<5>	REC<4>	REC<3>	REC<2>	REC<1>	REC<0>

REC<15:0>: This 2 byte symbol indicates the number error RS-FEC block errors, both correctable and uncorrectable, that have been seen by the PHY's receiver since it was last cleared. This counter shall be cleared when Clear REC (Symbol<10><1>) is received as 1. If the counter reaches 0xFFFF, it shall stay there until cleared by Clear REC.

Behavior of REC

It was decided that the text definition was not clear and should be replaced by state diagrams.

1. Link status transitions from down to up, Node A sets Clear REC to 0, REC<15:0> to 0x000 and REC Cleared to 0.
2. Node B sets Clear REC to 0, REC<15:0> to 0x000 and REC Cleared to 0
3. Node A and Node B increment their REC<15:0> based on the errors they detect
4. Node A sets Clear REC to 1 through MDIO command
5. Node B PHY clears REC<15:0> (=> 0x000) and sets REC Cleared to 1
6. While Node A sends Clear REC as 1, Node B increments REC<15:0> when errors are detected and continues to send REC Cleared as 1
7. Node A sends Clear REC as 0 based on MDIO command, Node B continues to increment REC<15:0> when errors are detected and sends REC Cleared as 0
8. Steps 3 to 7 continue while Link is maintained