78.5 Communication link access latency

PHY or interface type	Case	$T_{w\_sys\_tx}$ (min) (uS)	T_{w_phy} (min) (uS)	$T_{phy\_shrink\_tx}$ (max) (uS)	$T_{phy\_shrink\_rx}$ (max) (us)	$T_{w\_sys\_rx}$ (min) (uS)
10GBase-T1	Case 1	8.96	8.96			2.56
	Case 2	6.4	6.4			2.56
5GBase-T1	Case 1	17.92	17.92			5.12
	Case 2	12.8	12.8			5.12
2.5GBase-T1	Case 1	35.84	35.84			10.24
	Case 2	25.6	25.6			10.24

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149.2.2.3.1 Semantics of the primitive

PMA_UNITDATA.request(tx_symb) During transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb the value of the symbols to be sent over the MDI. The tx_symb may take on one of the values ~~in the set {–3, –1, 1, 3}.~~

SYMB: A multi-level symbols. In normal operation, this symbol may take on one of the values in the set {-1, -1/3, +1/3, +1} The symbols may additionally take the value 0 when zeros are to be transmitted in the following two cases: 1) when PMA_TXMODE.indication is SEND_Z during PMA training, and 2) after data mode is reached, the transmit function is in the LPI transmit mode and lpi_tx_mode is QUIET

ALERT: used to indicate that the PMA should transmit the link synchronization sequence to be used as EEE LPI.

149.3.5 LPI signaling The bit S_n is mapped to the transmit symbol T_n as follows: if $S_n = 0$ then $T_n = +1$, if $S_n = 1$ then $T_n = -1$. The PHY shall acquire descrambler state synchronization to the PAM2 training sequence and report success through scr_status. For side-stream descrambling, the MASTER PHY employs the receiver descrambler generator polynomial per Equation (149–7) and the SLAVE PHY employs the receiver descrambler generator polynomial per Equation (149–6). The PHY shall acquire descrambler state synchronization to the PAM2 training sequence and report success through scr_status. For side-stream descrambling, the MASTER PHY employs the receiver descrambler generator polynomial per Equation (149–7) and the SLAVE PHY employs the receiver descrambler generator polynomial per Equation (149–6).

PHYs with EEE capability have transmit and receive functions that can enter and leave the LPI mode independently. The PHY can transition to the LPI mode when the PHY has successfully completed training and pcs_data_mode is TRUE. The transmit function of the PHY initiates a transition to the LPI transmit mode when it generates 8 RS-FEC frames composed entirely of LPI control characters, as described in 149.3.2.2.21. The transmit function of the link partner signals the transition using the sleep signal. When the transmitter begins to send the sleep signal, it asserts tx_lpi_active and the transmit function enters the LPI transmit mode. Within the LPI mode PHYs use a repeating quiet-refresh cycle (see Figure 149–11). The first part of this cycle is known as the quiet period and lasts for a time lpi_quiet_time equal to ~~99~~ 95 RS-FEC frame periods. The quiet period is defined in 149.3.5.2. The second part of this cycle is known as the refresh period and lasts for a time lpi_refresh_time equal to 1 RS-FEC frame period. The refresh period is defined in 149.3.5.3. A cycle composed of one quiet period and one refresh period is known as a LPI cycle and lasts for a time lpi_qr_time equal to ~~100~~ 96 RS-FEC frame periods. lpi_offset, lpi_quiet_time, lpi_refresh_time, and lpi_qr_time are timing parameters that are integer multiples of the RS-FEC frame period. lpi_offset is a fixed value equal to lpi_qr_time/2 + 4 that is used to ensure refresh signals and alert times are appropriately offset by the link partner's.

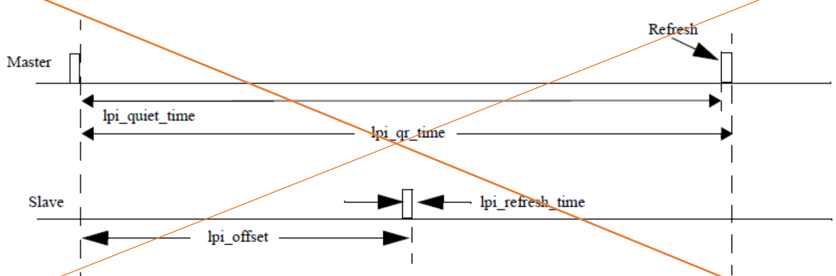
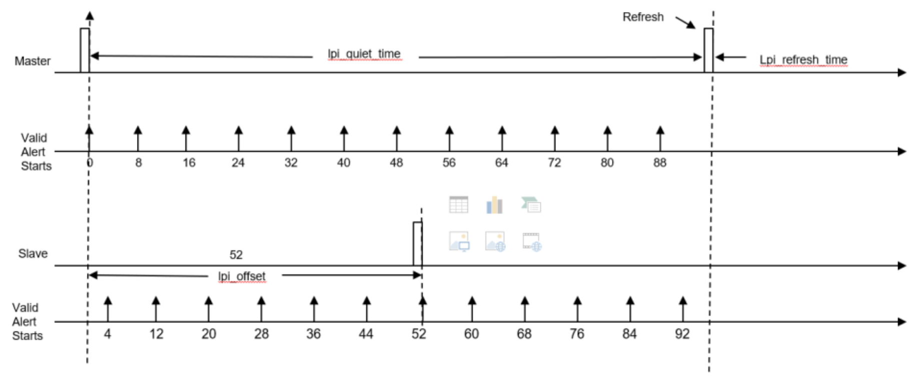


Figure 149–11—Timing periods for LPI signals



PHYs begin the transition from the LPI receive mode when the alert signal is detected by the PMA as defined in 149.4.2.3.

149.3.5.1 LPI Synchronization

To maximize power savings, maintain link integrity, and ensure interoperability, EEE-capable PHYs must synchronize refresh intervals during the LPI mode. The transition to PCS_Test is used as a fixed timing reference for the link partners. Refresh signaling is derived by counting RS-FEC frames from the transition to PCS_Test. At the Master RS-FEC frame count of zero and all multiples of ~~100~~96 RS-FEC frames thereafter denote the start of the cycle. An EEE-capable PHY in SLAVE mode is responsible for synchronizing its RS-FEC frame count to the MASTER's RS-FEC frame count during link up. The SLAVE shall ensure that its partial RS-FEC frame count is synchronized to the MASTER's partial RS-FEC frames within 1 partial RS-FEC frame. The start of the SLAVE quiet-refresh cycle is delayed from the MASTER by ~~50~~52 RS-FEC frames. This offset ensures that the MASTER and SLAVE ~~wake/sense~~ALERT windows are offset from each other and that the refresh periods are a half cycle offset. Following the transition to PAM4, the PCS continues to count transmitted RS-FEC frames (tx_rsfc), and uses the counter to generate refresh, ALERT and wake control signals for the transmit functions.

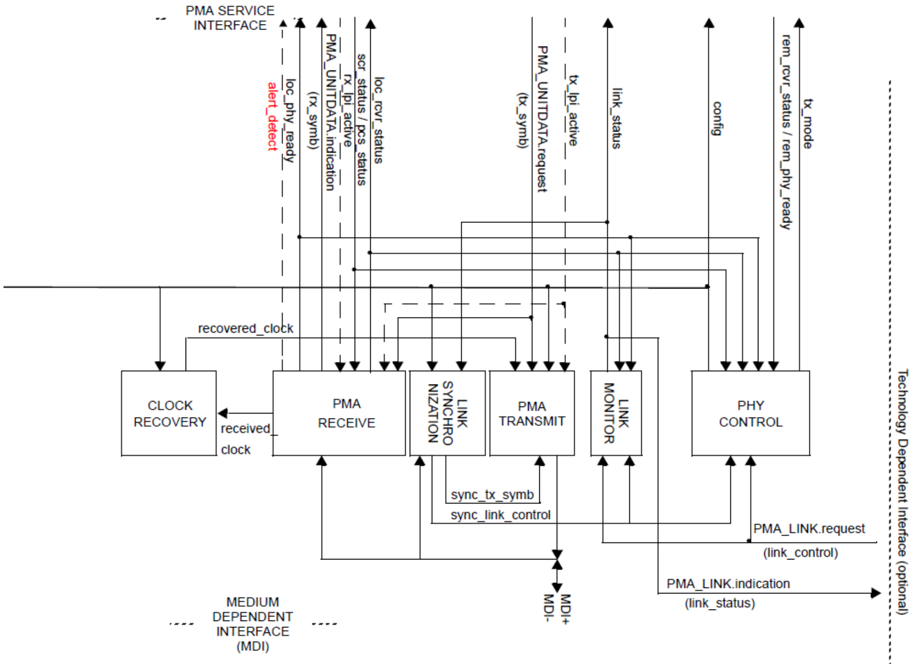
Table 149–3—Synchronization logic derived from slave signal RS-FEC frame count

Slave-side variable	u=tx_rsfc
tx_refresh_active=true	lpi_offset – lpi_refresh_time <= mod(u, lpi_qr_time) < lpi_offset
tx_alert_start=true	mod(u, alert_period) = wake_period/2

Table 149–4—Synchronization logic derived from master signal RS-FEC frame count

Master-side variable	v=tx_rsfc
tx_refresh_active=true	mod(v, lpi_qr_time) >= lpi_quiet_time
tx_alert_start=true	mod(v, wake_period) = 0

149.4.1 PMA functional specifications



NOTE—The recovered_clock arc is shown to indicate delivery of the recovered clock signal back to PMA TRANSMIT for loop timing.

Figure 149–17—PMA reference diagram