Proposal for intuitive and extendable mapping of interleaving register bits

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Registers for interleaving choice

- Comment 91 by William Lo
- Agree that registers are needed
- More intuitive and extendable mapping is desirable
- Aspects:
  - Explicit selection of a particular interleaving factor
  - Extendability with higher interleaving factors
  - Phrasing

Proposed solution (Register table)

- Assign to respective tables
  - 1.2311.12:11 - Interleave request (R/W)
  - 1.2312.12:11 - Link partner interleave request (RO)
- For both registers
  - 00: L=1 → No interleaving
    - Default for 2.5GBASE-T1
  - 01: L=2 → RS-FEC interleaving factor two
    - Default for 5GBASE-T1, Reserved for 2.5GBASE-T1
  - 10: L=4 → RS-FEC interleaving factor four
    - Default for 10GBASE-T1, Reserved for 2.5GBASE-T1 and 5GBASE-T1
  - 11 = Reserved

Word-smithing sub-clauses

- 45.2.1.194.x Interleave request (1.2311.12:11)
  - Bits 1.2311.12:11 control the Reed-Solomon interleave setting of this PHY. Reed-Solomon interleaving is described in 149.3.2.2.17. This is communicated to the link partner via Infofields as specified in 149.4.2.4.3.
- 45.2.1.195.x Link partner interleave request (1.2312.12:11)
  - Bits 1.2312.12:11 contain the Reed-Solomon interleave setting requested by the link partner. Reed-Solomon interleaving is described in 149.3.2.2.17. This is communicated by the link partner via Infofields as specified in 149.4.2.4.3.

Motion