Asymmetric Framework

William Lo

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Motivations and Requirements for Asymmetric Speeds

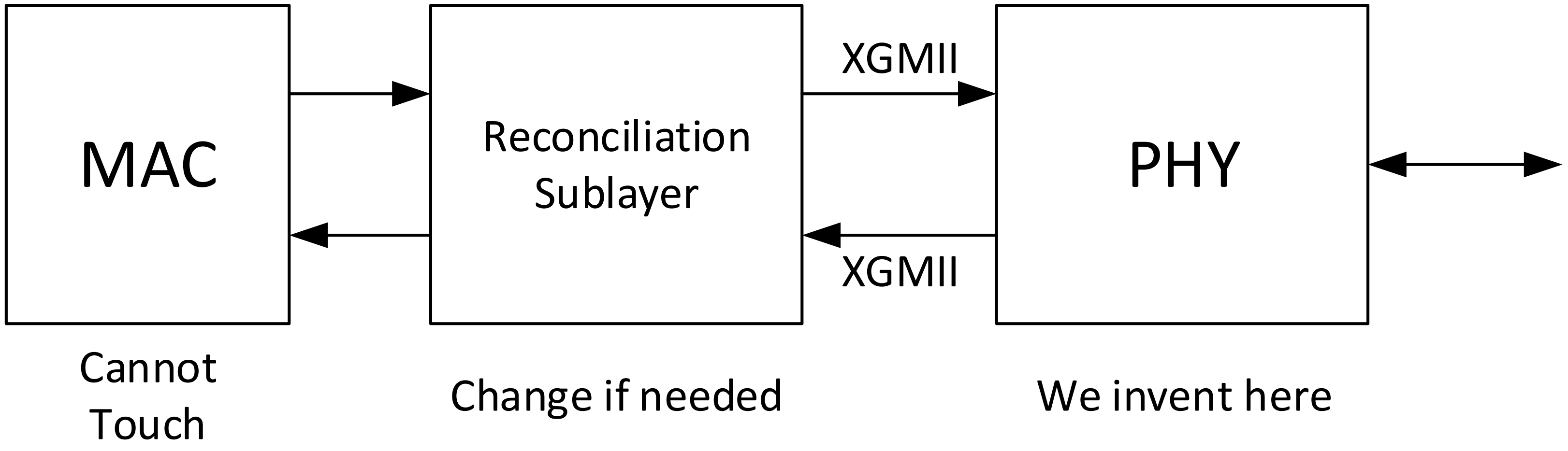
- Target use cases where one direction transmits high data rate while the other direction is very low data rate.
  - i.e. Cameras, Displays, Sensors
- Asymmetric mode should be power efficient
- Cannot change the Ethernet MAC layer
- Can touch the Reconciliation Sublayer
- Ideally no excess latency when there is traffic to send in the low data rate direction
- Ideally no side band signaling between the Reconciliation Sublayer and the PHY

Bursty RS – Slow data transmitted in high speed bursts

- MAC cannot see line activity
  - Cannot ask MAC to sync to burst on line

- Can ask RS to hold off
  - Introduces latency
  - Introduces variable delay

- Slow direction on line
  - Solution can be bursty or
  - Can be slow and steady
  - We define how it operates

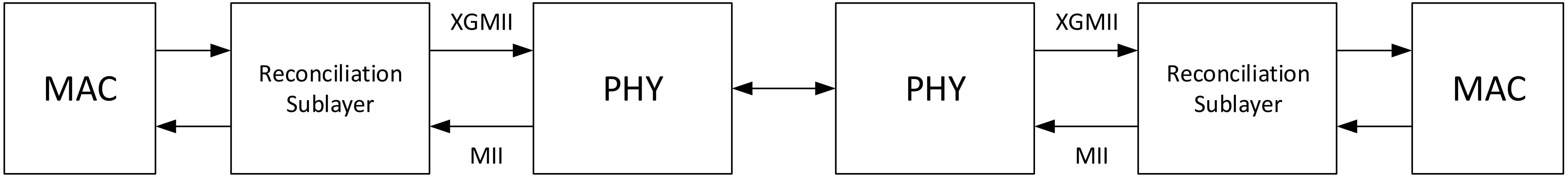


Smooth RS – Slow data transmitted at constant speed

- MAC operates normally
  - Slow data transmitted at constant speed
  - No knowledge of timing of line activity required

- Slow direction on line
  - Solution can be bursty or
  - Can be slow and steady
  - We define how it operates
  - We take care of constant latency in the PHY

- Constant flow in RS
  - No added latency
  - Fixed delay



Bound the Problem

- Pick a standard Ethernet speed in the slow direction
  - i.e. 10M, 100M, 1Gb/s and not some weird speed
  - Things are well understood at standard speeds (timing, MIBs, etc.)
- Pick the slowest standard Ethernet speed that meets 90+% of volume
  - Picking some faster speed may impact power
  - Picking some faster speed may limit the solution space
  - If a faster speed is required (ie. Firmware download) use normal mode
- Slow direction speed is typically control operation (I^2C, SPI like speeds)
- Don’t need both direction to be slow speed
  - Both directions can be fast
  - One fixed direction fast, other fixed direction slow.

- ➔ Pick 10Mb/s in slow direction

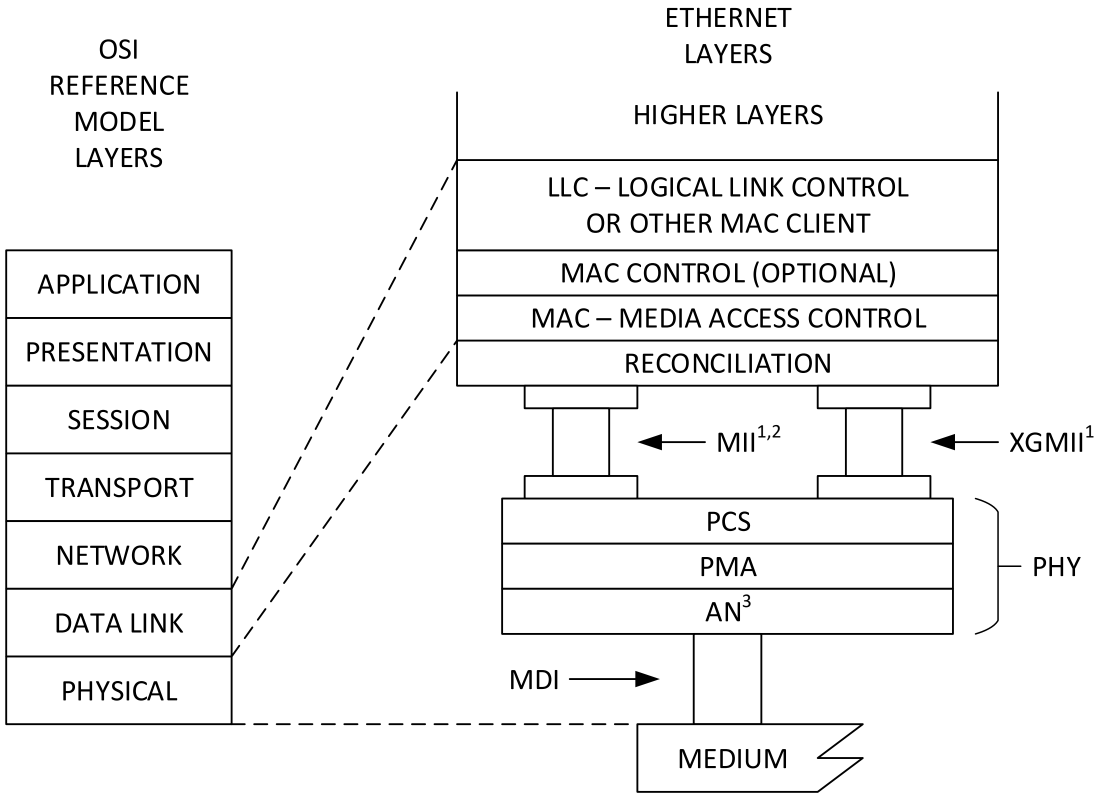
How to Make the Reconciliation Sublayer Fixed Delay

- Option 1:
  - XGMII in the 10Gb/s, 5Gb/s, 2.5Gb/s direction
  - MII in the 10Mb/s direction
  - Precedent for this Clause 76 – EPON. XGMII in one direction, GMII in the other
- Option 2:
  - Overlay MII on the XGMII in the slow direction
- Option 3:
  - Run XGMII 1000x, 500x, 250x slower in the slow direction
- Option 4:
  - Replicate XGMII data 1000x, 500x, 250x in the slow direction
- Other Options?
  - As long as the reconciliation sublayer layer does not introduce variable delays, it is a valid solution

Option 1 – Dual XGMII/MII

- For MGBASE-T1 PHY define both XGMII and MII or its equivalent functionality as the base interface

- MII functionality is required only if asymmetrical modes implemented



OSI REFERENCE MODEL LAYERS

APPLICATION
PRESENTATION
SESSION
TRANSPORT
NETWORK
DATA LINK
PHYSICAL

ETHERNET LAYERS

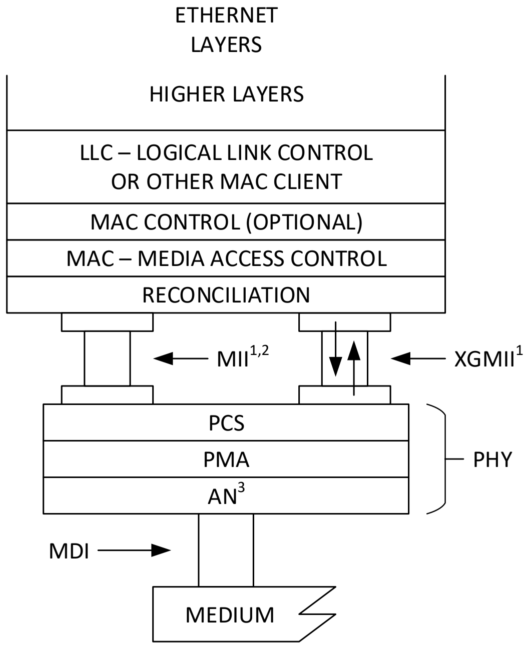
HIGHER LAYERS
LLC – LOGICAL LINK CONTROL OR OTHER MAC CLIENT
MAC CONTROL (OPTIONAL)
MAC – MEDIA ACCESS CONTROL
RECONCILIATION
MII[1,2]
XGMII[1]
PCS
PMA
AN[3]
PHY
MDI
MEDIUM

MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
AN = AUTO-NEGOTIATION

NOTE 1 – Implementation of a physical XGMII and MII is optional
NOTE 2 – MII or equivalent functionality is required only if the optional asymmetrical mode is implemented
NOTE 3 – Auto-Negotiation is optional

Modes of Operation

- Symmetrical Mode



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HIGHER LAYERS

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MAC CONTROL (OPTIONAL)

MAC – MEDIA ACCESS CONTROL

RECONCILIATION

MII[1,2]

XGMII[1]

PCS

PMA

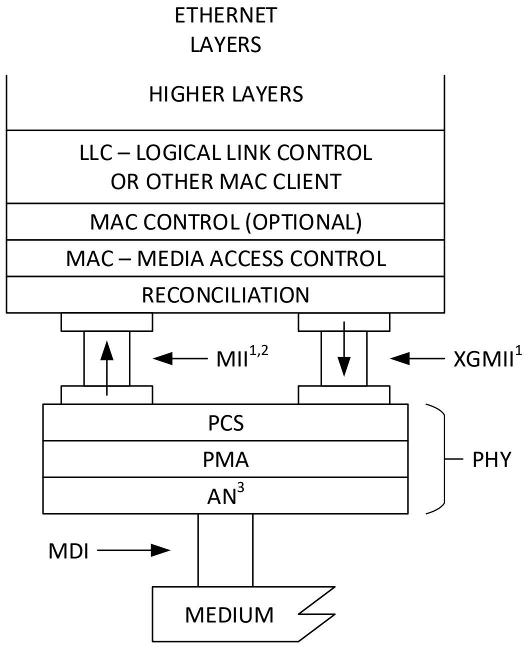
AN[3]

PHY

MDI

MEDIUM

- Slow RX Mode



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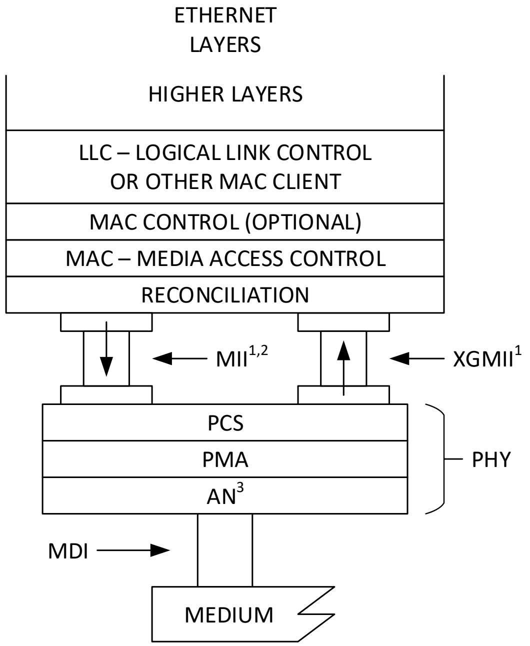
- Slow TX Mode



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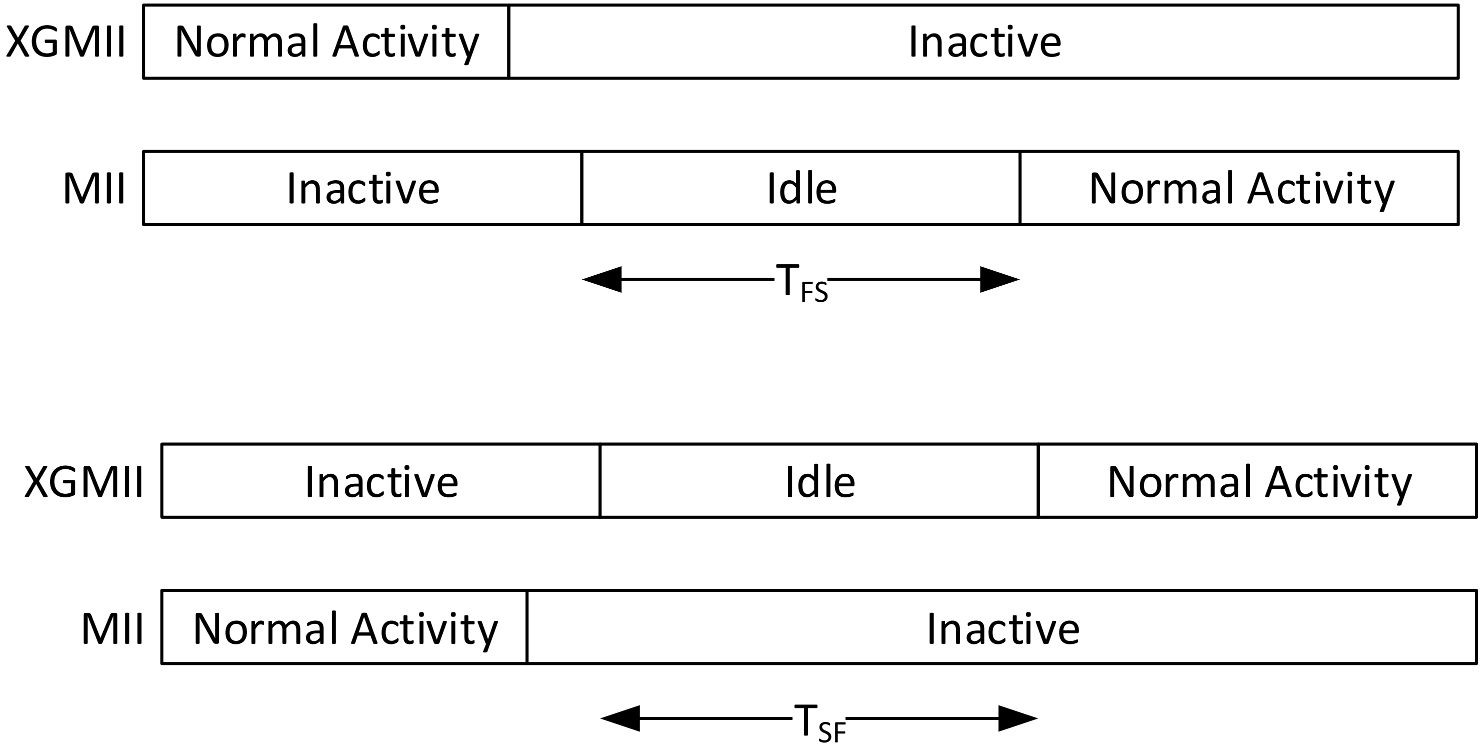
How to Determine XGMII or MII is Active

- Define New Sequence Ordered Set On XGMII
  - /Q/00/00/04/ ➔ Inactive XGMII
- Define New Encoding on MII
  - TX_EN (RX_DV) = 0, TX_ER (RX_ER) = 1, TXD<3:0> (RXD<3:0>) = 0010 ➔ Inactive MII
- If both XGMII and MII are Inactive, the PHY treats it as IDLEs in the mode it is currently operating in

How to Switch Between Modes

- T_{FS} – Time for PHY to transition from fast to slow mode
- T_{SF} – Time for PHY to transition from slow to fast mode



XGMII: Normal Activity | Inactive

MII: Inactive | Idle | Normal Activity

T_{FS}

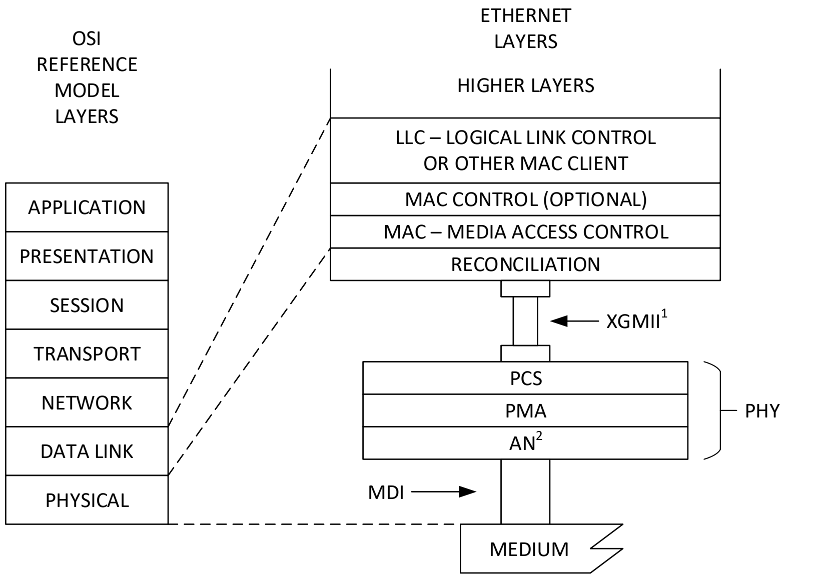
XGMII: Inactive | Idle | Normal Activity

MII: Normal Activity | Inactive

T_{SF}

Option 2 – Overlay MII on XGMII

- Define New Sequence Ordered Set On XGMII
  - /Q/00/mm/04/ ➔ In slow mode. Otherwise in fast mode.
- mm[7:0] definition
  - mm[4] = TX_EN (RX_DV)
  - mm[5] = TX_ER (RX_ER)
  - mm[3:0] = TXD<3:0> (RXD<3:0>)
  - mm[7:6] = 00



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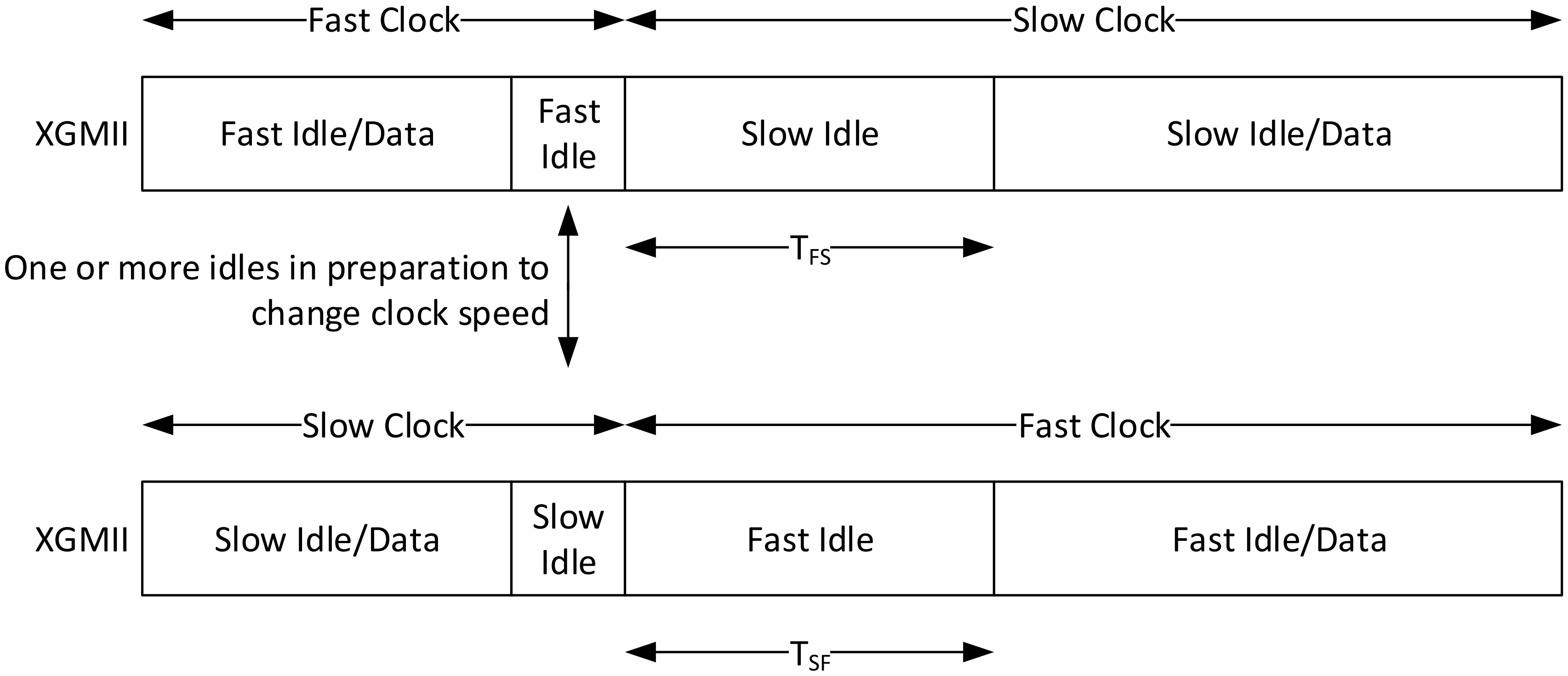
How to Switch Between Modes

- T_{FS} – Time for PHY to transition from fast to slow mode
- T_{SF} – Time for PHY to transition from slow to fast mode
- TX_CLK (RX_CLK) changes speed



One or more idles in preparation to change clock speed

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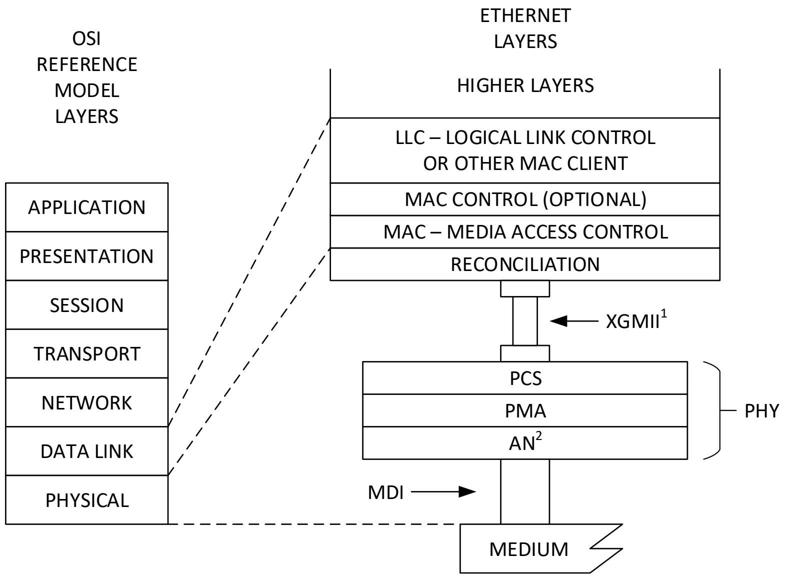
Option 3 – Slow Down XGMII to Match Slow Rate

- Define Slow Idle On XGMII
  - TXC (RXC) = 1, TXD<7:0> (RXD<7:0>) = 0x05 ➔ Slow Idle
- Data passed 4 bytes at a time at slower clock rate (identical to XGMII)



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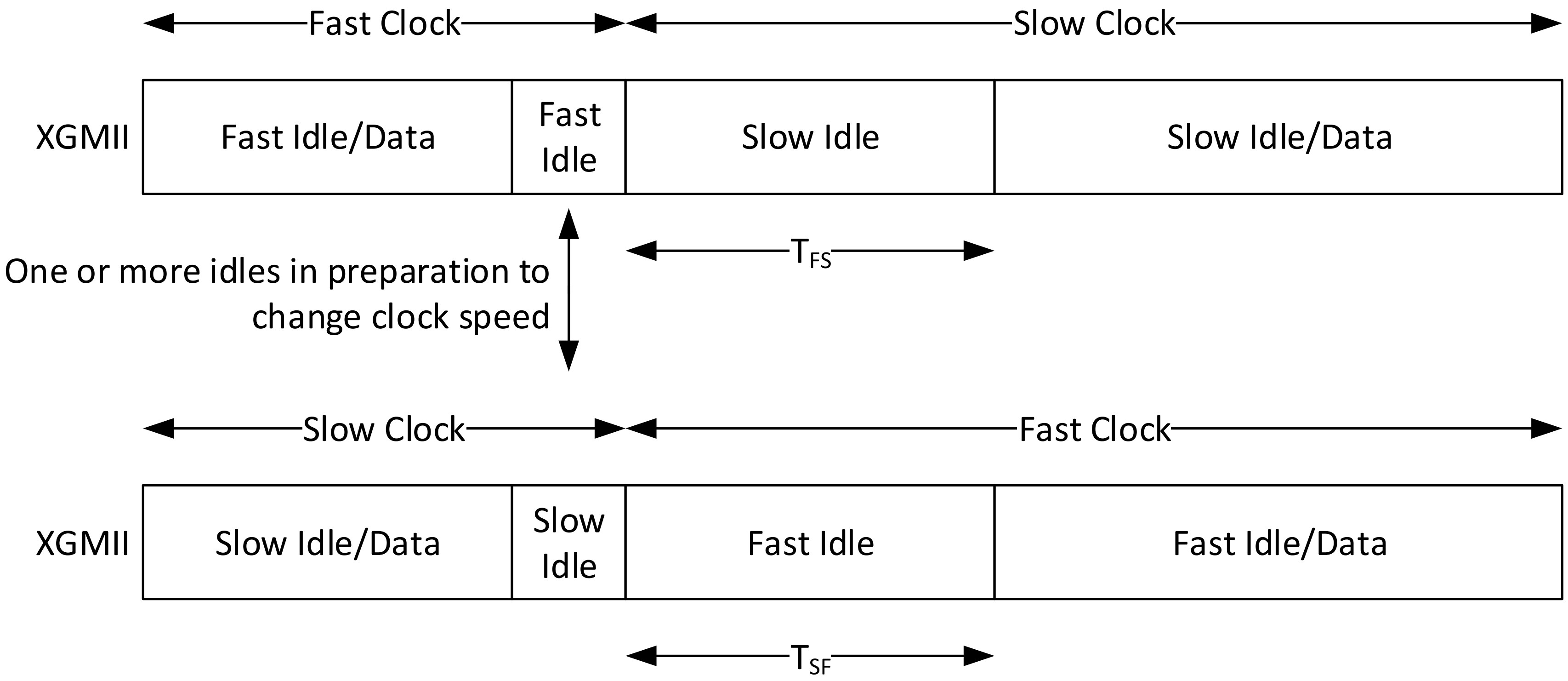

Option 4 – Replicate XGMII Data

- Identical to Option 3 except clock always running at fast rate
- Replicate 1000x, 500x, or 250x at transmitter
- Down sample 1/1000, 1/500, or 1/250 at receiver

Recommendation

- Add an objective to 802.3ch

Define an optional power efficient mode of operation where one direction operates at 2.5Gb/s, 5Gb/s, or 10Gb/s, and the other direction operates at 10Mb/s

THANK YOU