MDI return loss considerations

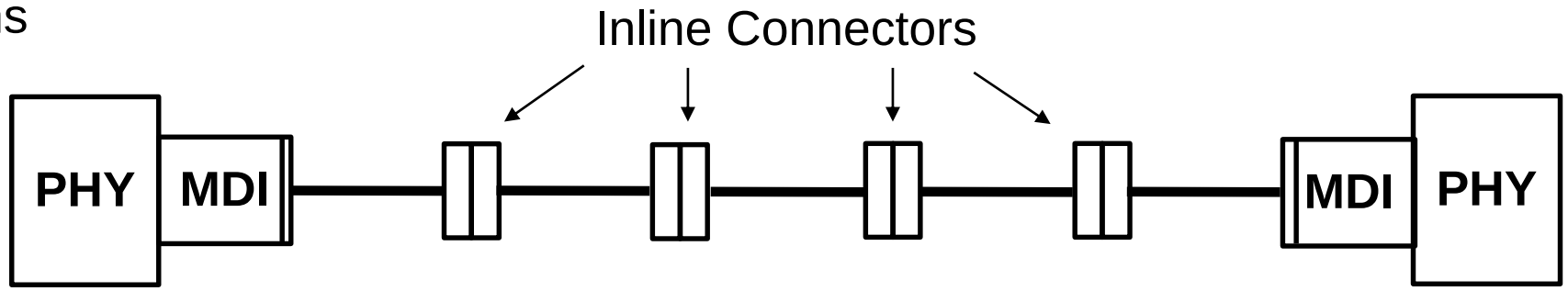
German Feyh

January 2019

BROADCOM®

Return loss and system complexity from Ahmad Chini and Hui Pan http://www.ieee802.org/3/bp/public/jan15/pan_3bp_01_0115.pdf

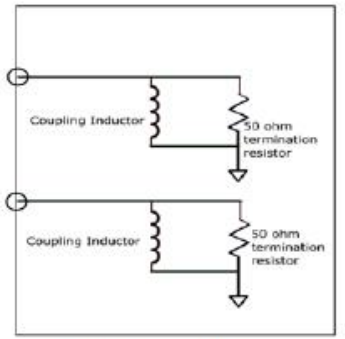
- Finite RL necessitates digital echo cancellation
  - Increased signal processing complexity
- Excessive echo reduces effective ADC dynamic range
  - Lower SNR and shorter cable reach
- High freq. echo amplifies jitter to noise conversion
  - Lower SNR and shorter cable reach
  - Slower timing recovery and longer startup
- Serial reflections cause system resonance
  - Degraded driver stability
  - More DM/CM conversions



BROADCOM

Comparison to adopted MDI return loss mask by http://www.ieee802.org/3/ch/public/nov18/bhagwat_3ch_01a_1118.pdf

- To generate the MDI return loss mask, Bhagwat considers only the parasitic capacitance of the PoDL inductor and termination resistor.
  - Short trace length.
- ESD requirements:
  - Chip handling, HBM (Human Body Model), CDM (charge device model),
  - IEC.
- Parasitic capacitance from:
  - Coupling capacitors,
  - Trace length between connector and chip,
  - Board material and possible vias,
  - Chip, substrate and pads.
- For an implementable system, MDI return loss mask should be amended:
  - At the lower frequency range to allow for smaller PoDL inductors.
  - High frequency range to allow for the parasitic capacitance.



Schematic

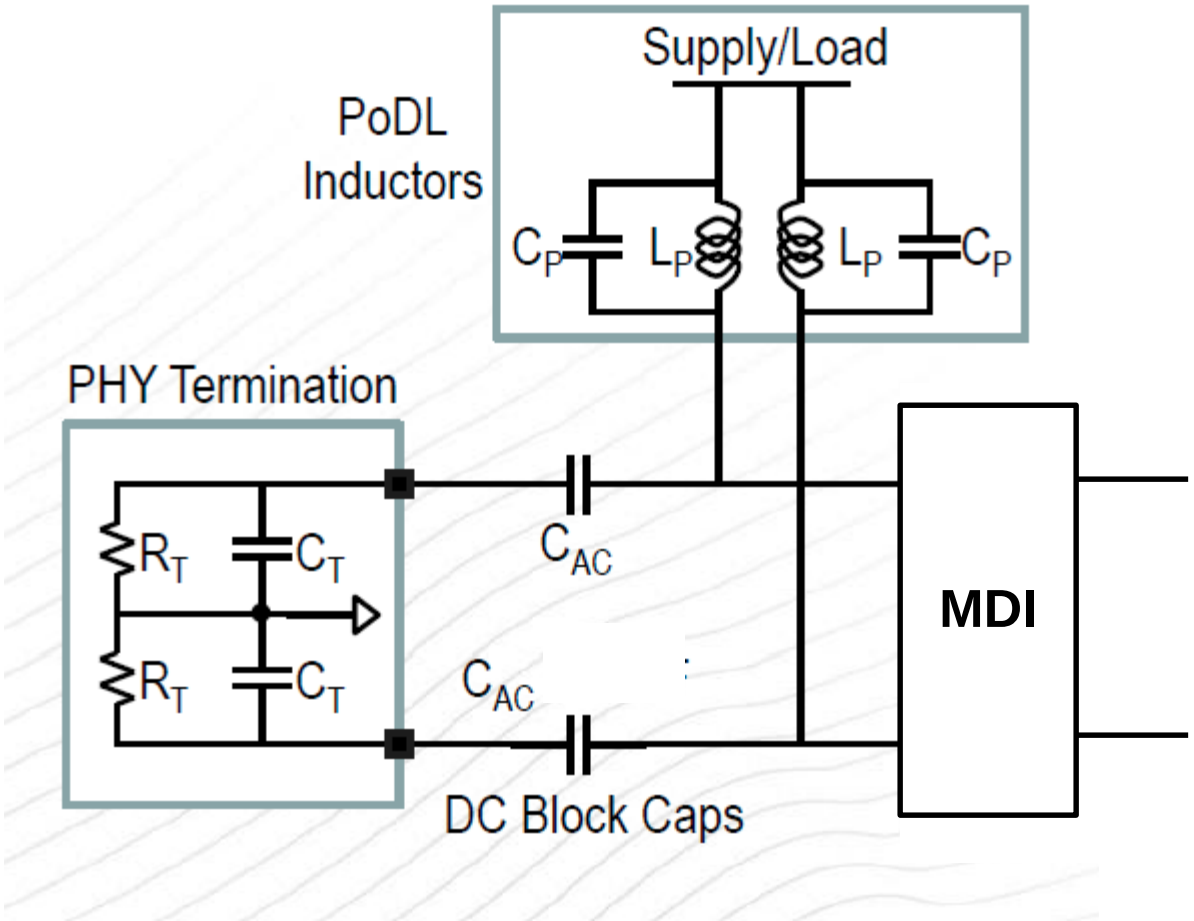

PFL3215-153

BROADCOM

Considered topology and PoDL inductors

- 4 different available inductors
- Inductance lower than the 6.8uH inductance considered by bhagwat_3ch_01a_0918.pdf
- Parasitic capacitance computed from **S**elf-**R**esonant **F**requency
- $SRF = \frac{1}{2\pi\sqrt{CL}}$

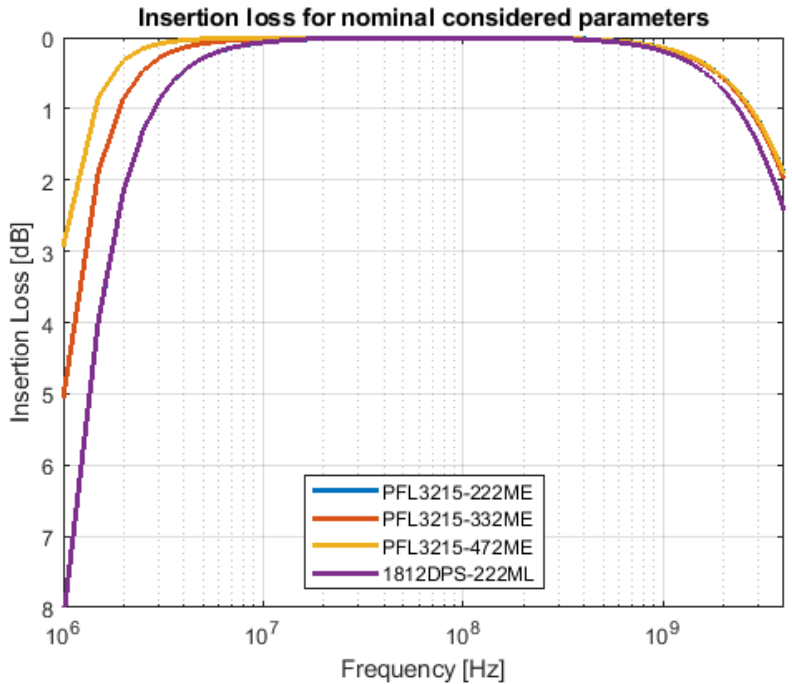
Part Number	Inductance [uH]	Self-Resonant Frequency [MHz]	Parasitic Capacitance [pF]
PFL3215-222ME	2.2	250	0.184
PFL3215-332ME	3.3	190	0.180
PFL3215-472ME	4.7	170	0.184
1812DPS-222ML	2.2	175	0.376

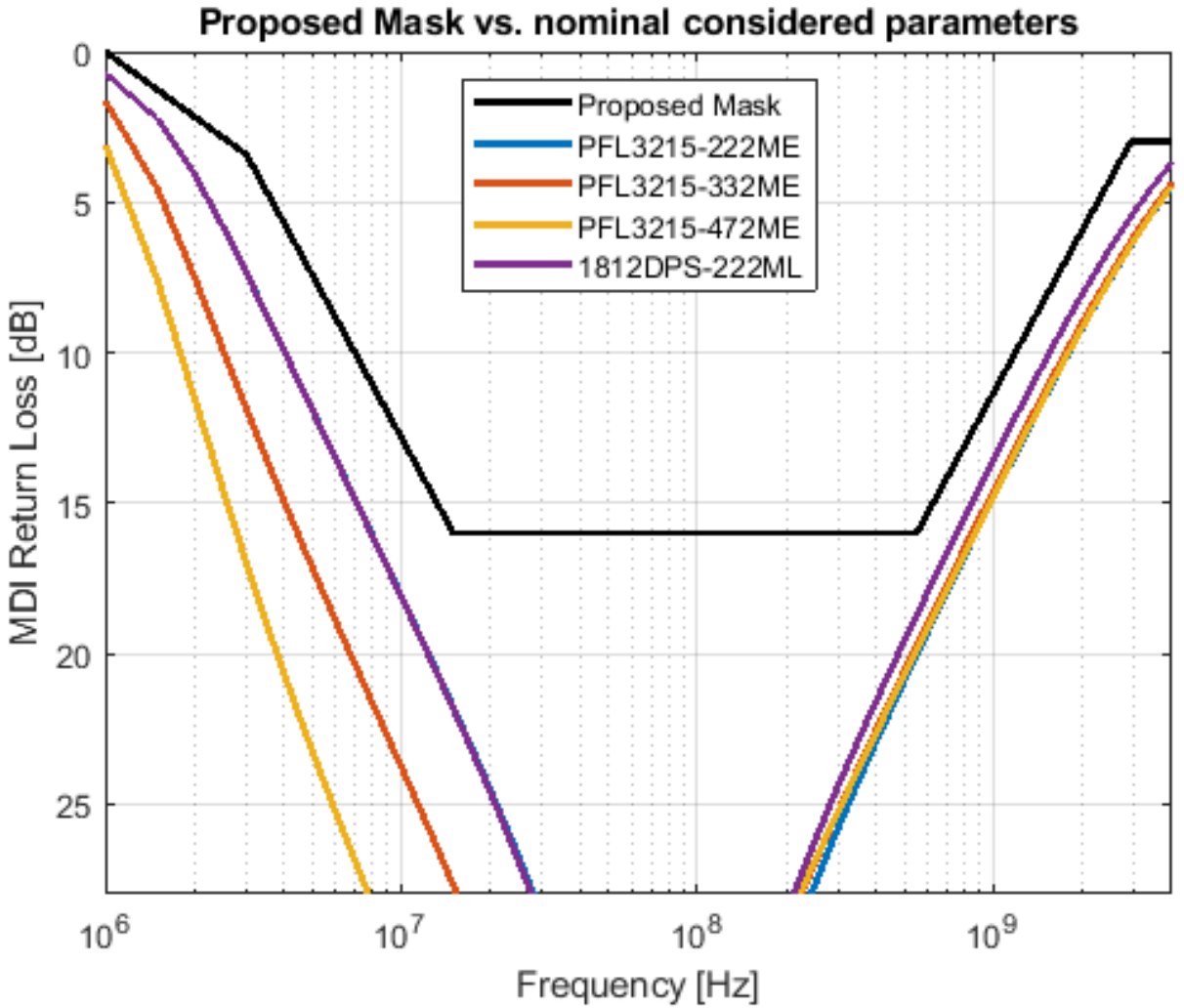


BROADCOM

Single sided parasitic termination capacitance: Cterm 1.0pF to support HBM and IEC 61000-4-2

Part Number	Inductance [uH]	Self-Resonant Frequency [MHz]	Parasitic Capacitance [pF]
PFL3215-222ME	2.2	250	0.184
PFL3215-332ME	3.3	190	0.180
PFL3215-472ME	4.7	170	0.184
1812DPS-222ML	2.2	175	0.376





BROADCOM

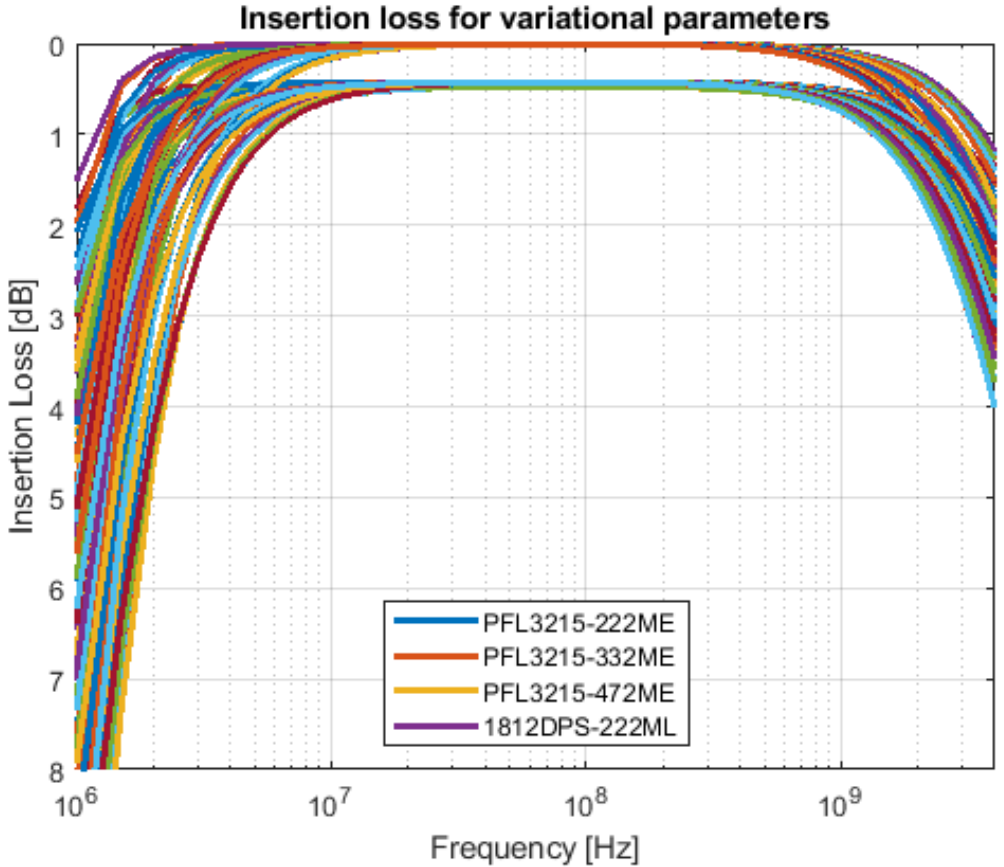
Mask in numerical form considering single sided parasitic termination capacitance Cterm=1.0pF

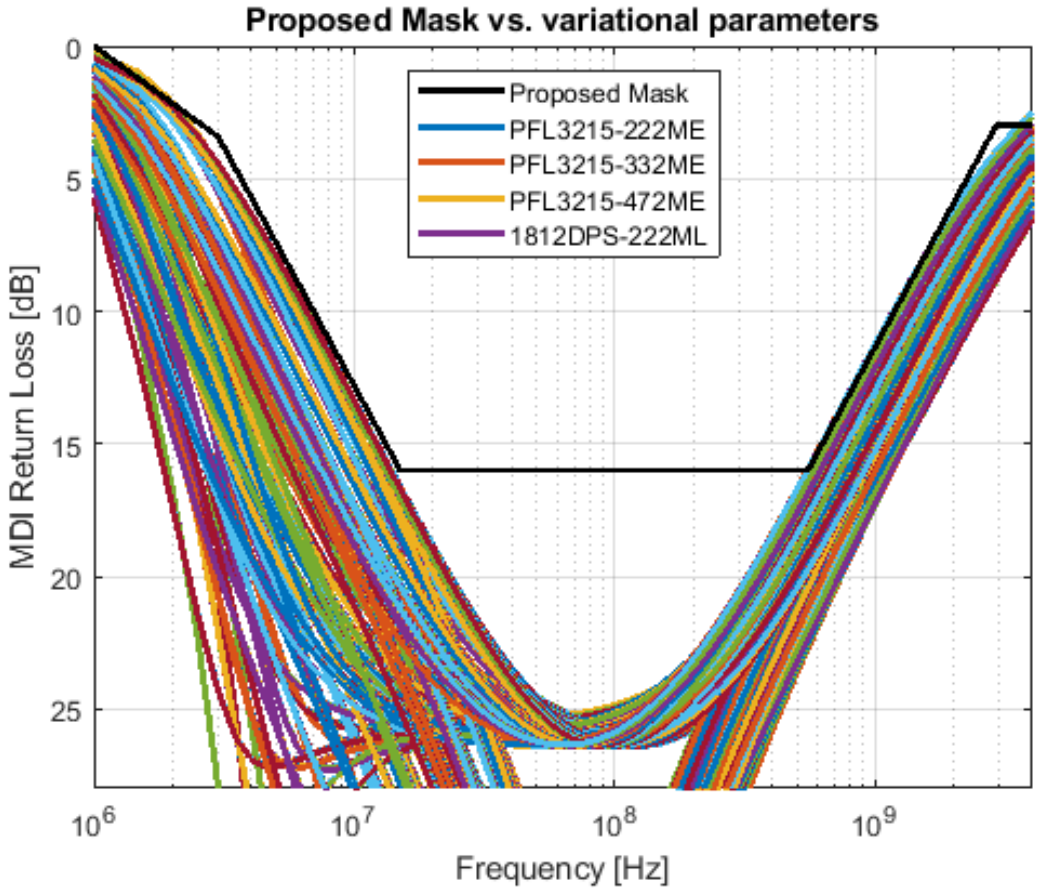
$$\text{MDI return loss} = \begin{cases} 3.42+7.17*\log10(f/3) & 1 \le f<3 \\ 16 + 18*\log10(f/15) & 3 \le f<15 \\ 16 & 15 \le f<550 \\ 16 - 18*\log10(f/550) & 550 \le f<2900 \\ 3 & 2900 \le f<4000 \end{cases}$$

Return loss in dB, frequency in MHz

Parameter variation

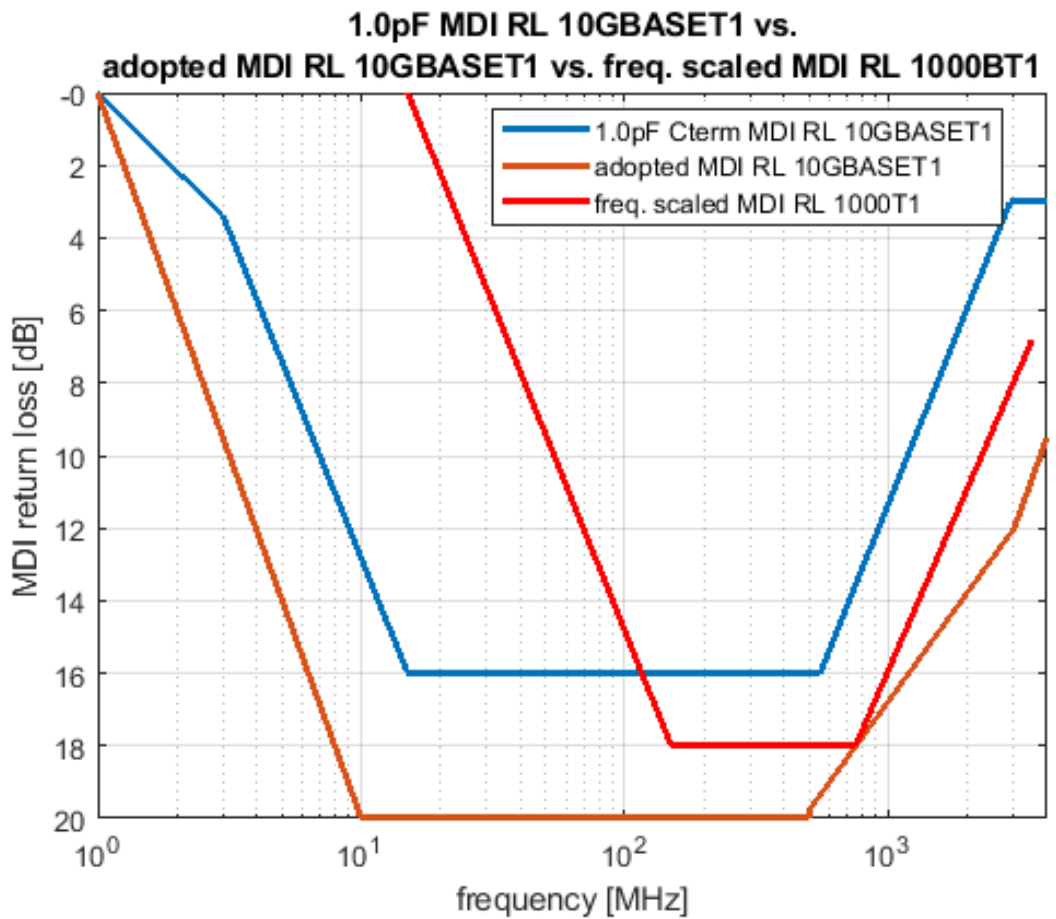
- Low PoDL inductance sets low frequency behavior 1 ≤f<15 [MHz]
- Termination resistor variation sets middle frequency behavior 15 ≤f<550 [MHz]
- Overall capacitance sets upper frequency behavior 550≤f<4000 [MHz]

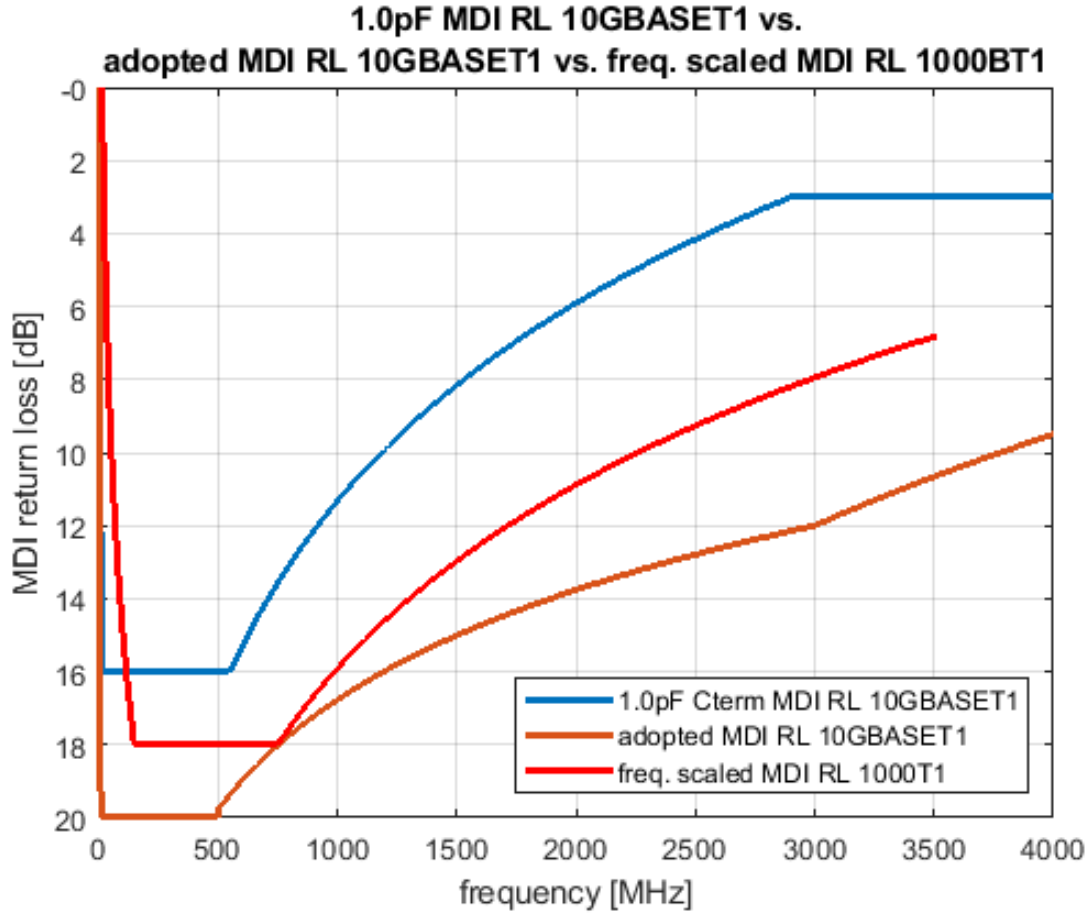




Proposed MDI return loss mask in comparison for Cterm=1.0pF

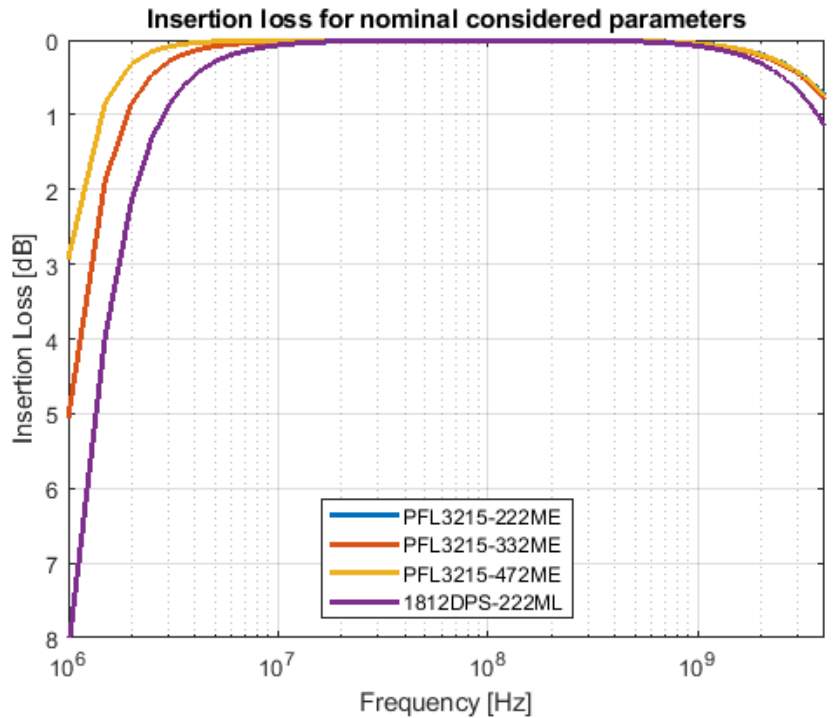
- Lower transition band: 1MHz to 15MHz: allow for smaller inductors.
- Mid frequency: allow for same termination resistor variation as 10GBASET.
- Upper transition band: 550MHz to 4GHz: allow for ESD parasitic capacitance

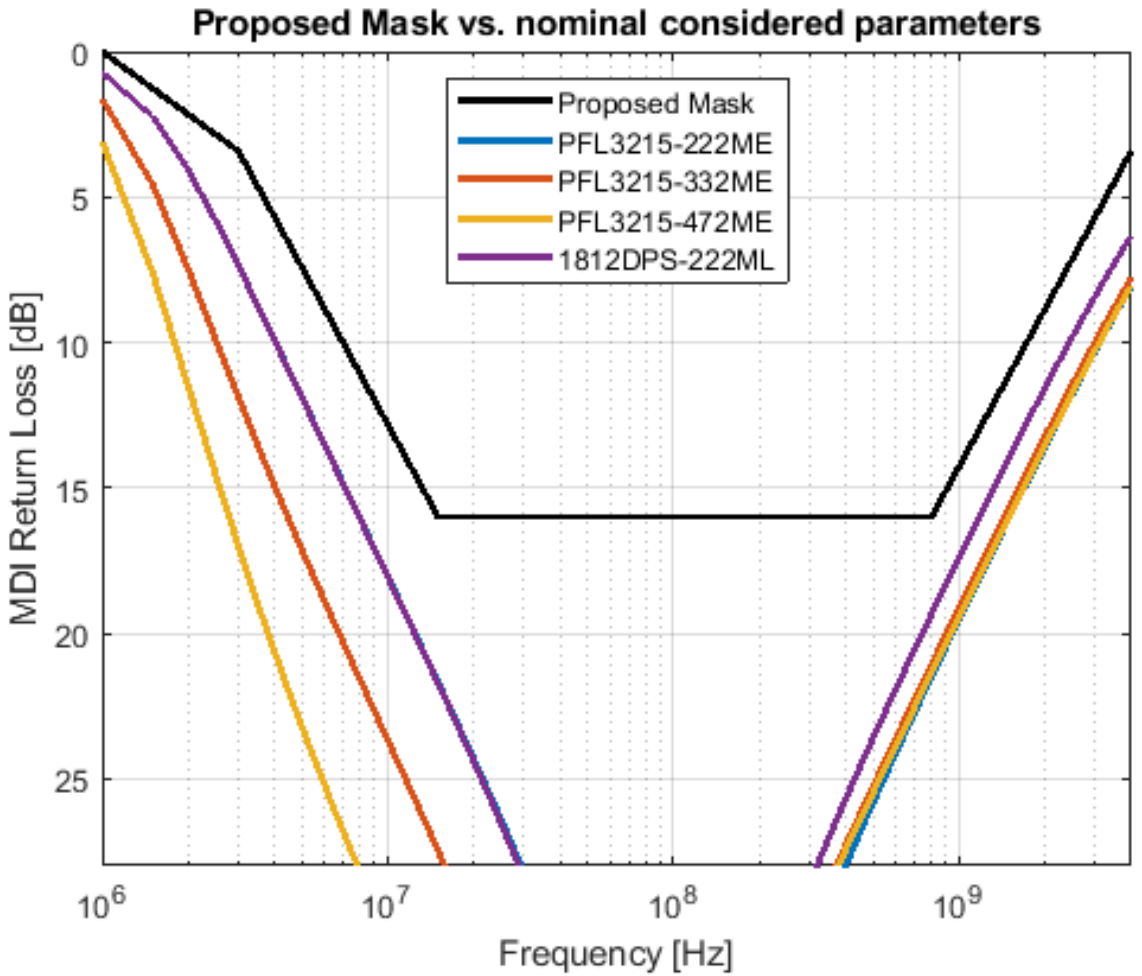




Single sided parasitic termination capacitance: Cterm 0.5pF

Part Number	Inductance [uH]	Self-Resonant Frequency [MHz]	Parasitic Capacitance [pF]
PFL3215-222ME	2.2	250	0.184
PFL3215-332ME	3.3	190	0.180
PFL3215-472ME	4.7	170	0.184
1812DPS-222ML	2.2	175	0.376





BROADCOM

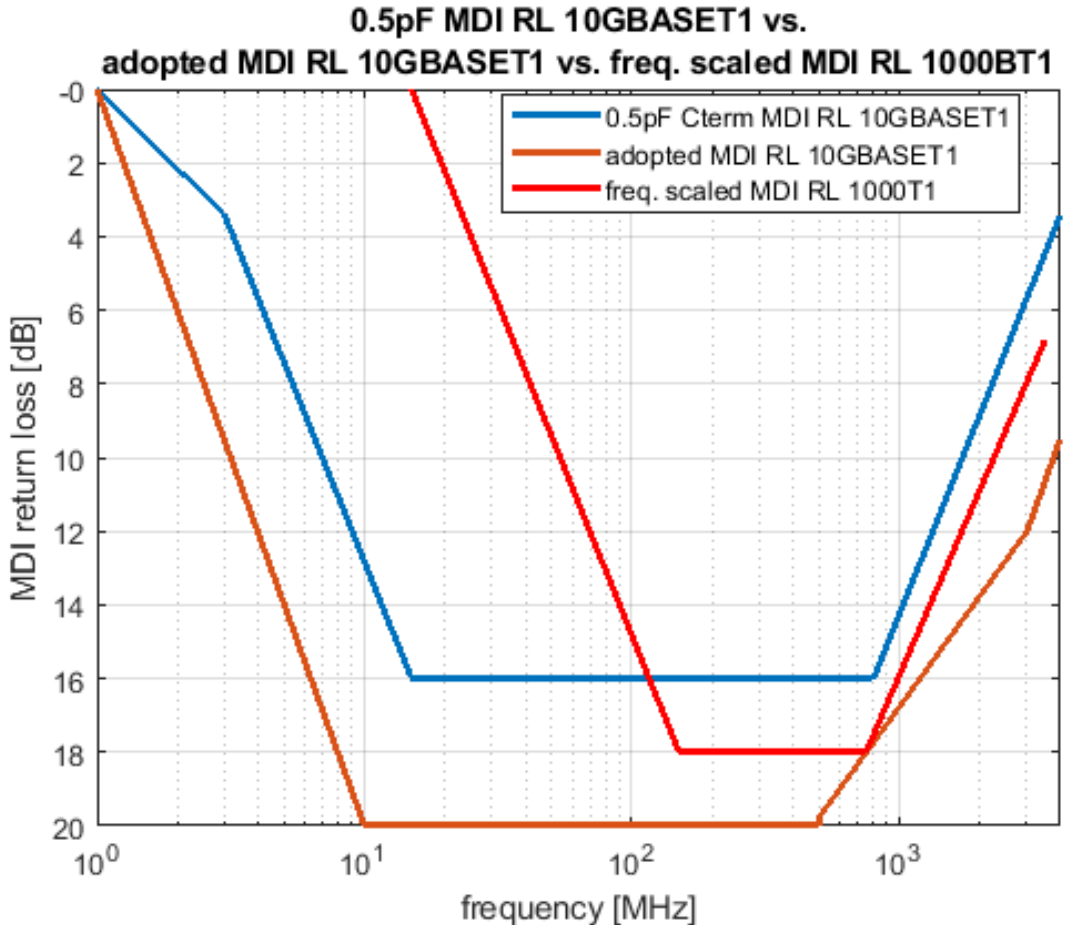
Mask in numerical form considering single sided parasitic termination capacitance Cterm=0.5pF

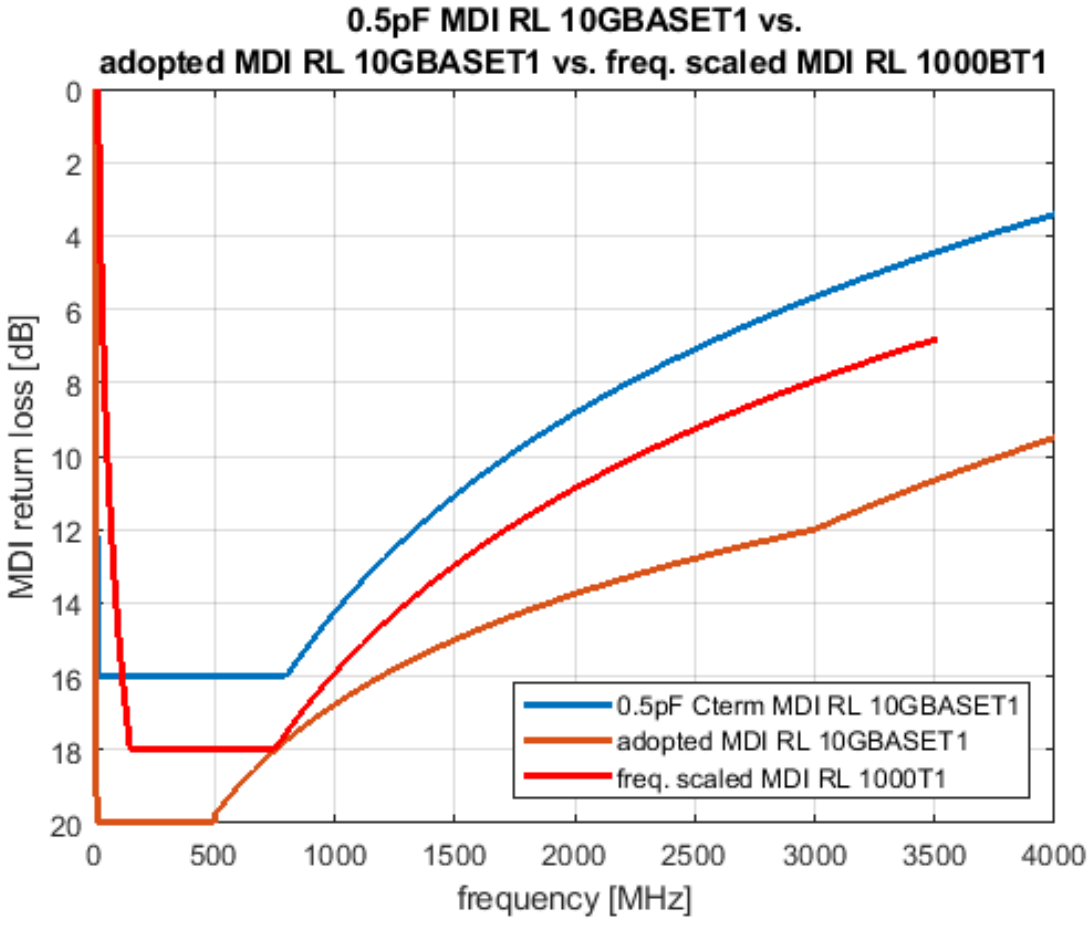
$$\text{MDI return loss} = \begin{cases} 3.42+7.17*\log10(f/3) & 1 \le f<3 \\ 16 + 18*\log10(f/15) & 3 \le f<15 \\ 16 & 15 \le f<800 \\ 16 - 18*\log10(f/800) & 800 \le f<4000 \end{cases}$$

Return loss in dB, frequency in MHz

Proposed MDI return loss mask in comparison for Cterm=0.5pF

- Low PoDL inductance sets low frequency behavior 1 ≤f<15 [MHz]
- Termination resistor variation sets middle frequency behavior 15 ≤f<800 [MHz]
- Overall capacitance sets upper frequency behavior 800≤f<4000 [MHz]

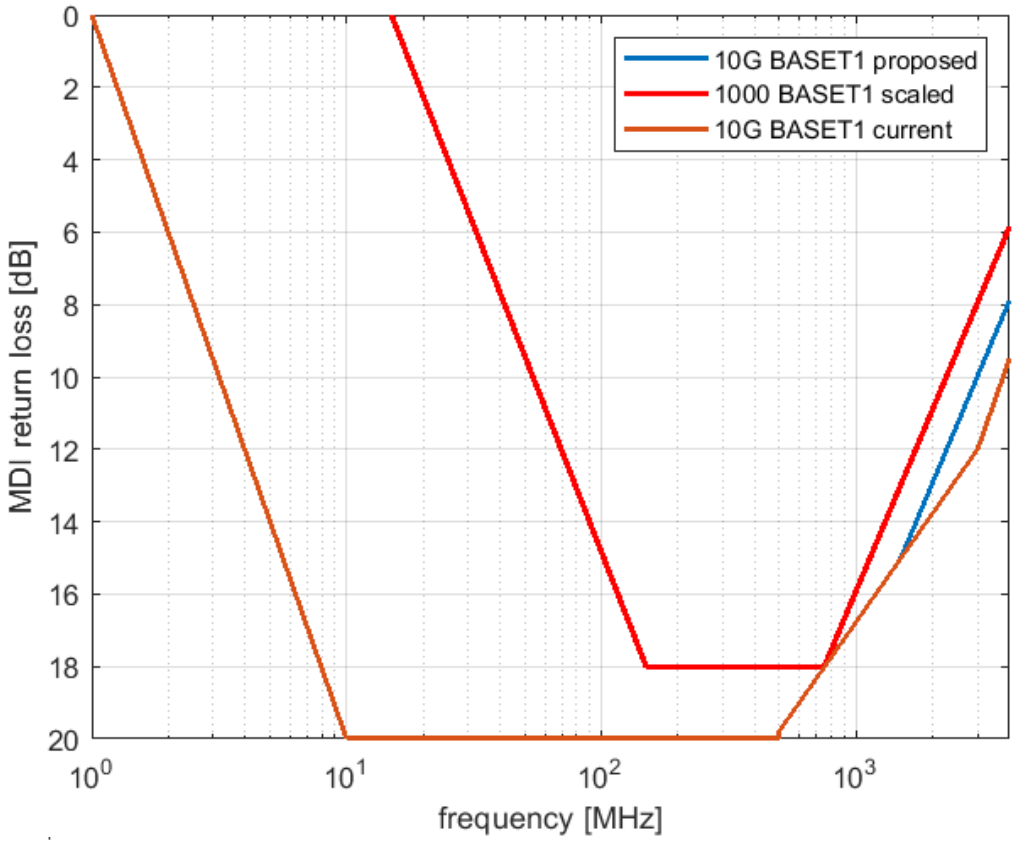


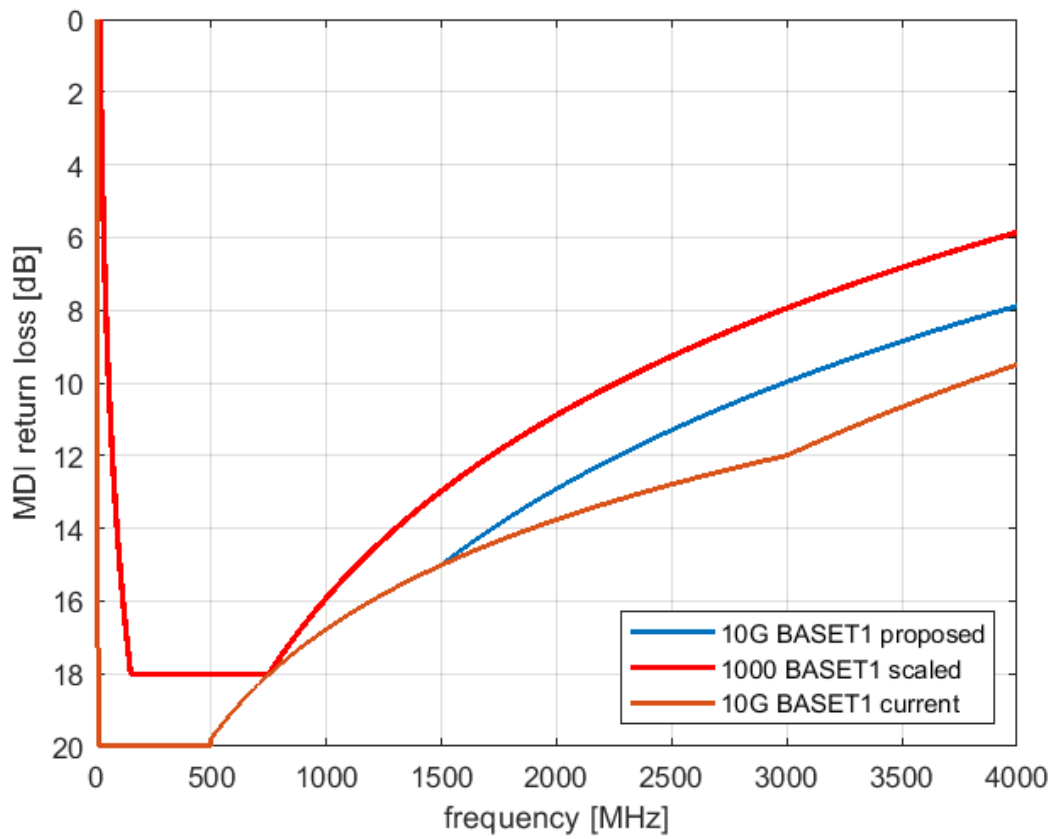


Minimal change

- Use mostly the current standard
- Move upper frequency corner down from 3Ghz to 1.5GHz
- Match the 1000BASET1 slope (16.7), which is lower than the upper frequency slope (20) of the current MDI RL spec.
- More stringent than the 1000BASET1 standard

	1000BASET1	2.5/5/10GBASET1
Lower freq. corner	20MHz	10MHz or 15X lower compared to Nyquist
Max. MDI RL	18dB	20dB
MDI RL at Nyquist	8.4dB	10.4dB





Minimal change from current standard
upper frequency knee moved from 3GHz to 1.5GHz

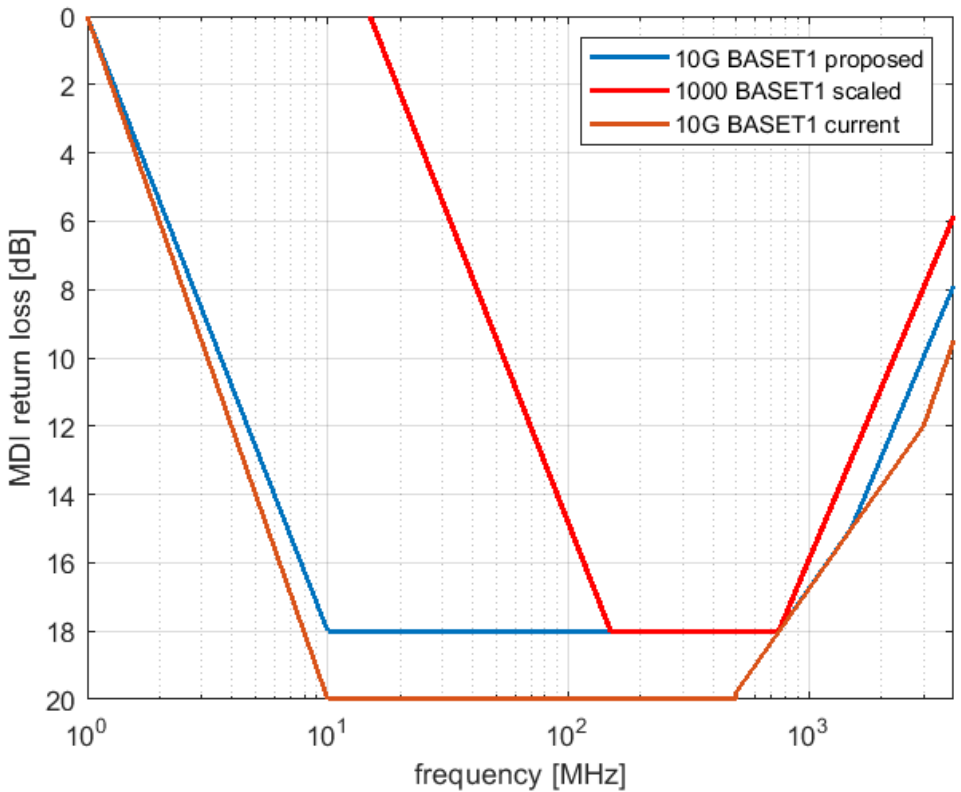
$$\text{MDI return loss} = \begin{cases} 20+20*\log10(f/10) & 1 \le f<10 \\ 20 & 10 \le f<500 \\ 12 - 10*\log10(f/3000) & 500 \le f<1500 \\ 15 - 16.7*\log10(f/1500) & 1500 \le f<4000 \end{cases}$$

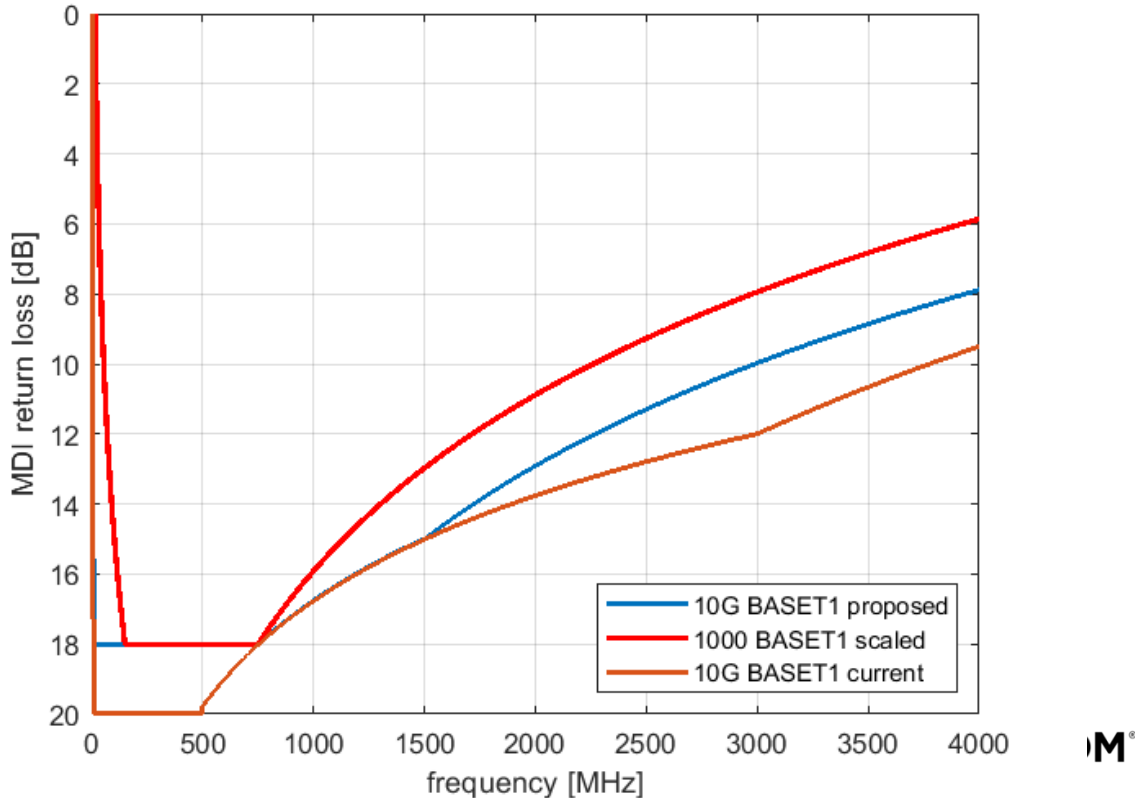
Return loss in dB, frequency in MHz

Allow for higher Rterm variation for design freedom of the TX and termination resistor variation

- Use mostly the current standard
- Lower max MDI RL from 20dB to 18dB
- Move upper frequency corner down from 3Ghz to 1.5GHz
- Match the 1000BASET1 slope (16.7), which is lower than the upper frequency slope (20) of the current MDI RL spec.
- Always better or the same as the 1000BASET1 standard

	1000BASET1	2.5/5/10GBASET1
Lower freq. corner	20MHz	10MHz or 15X lower
MDI RL at Nyquist	8.4dB	10.4dB





Allow for higher Rterm variation for design freedom of the TX, upper frequency knee moved down from 3GHz to 1.5GHz

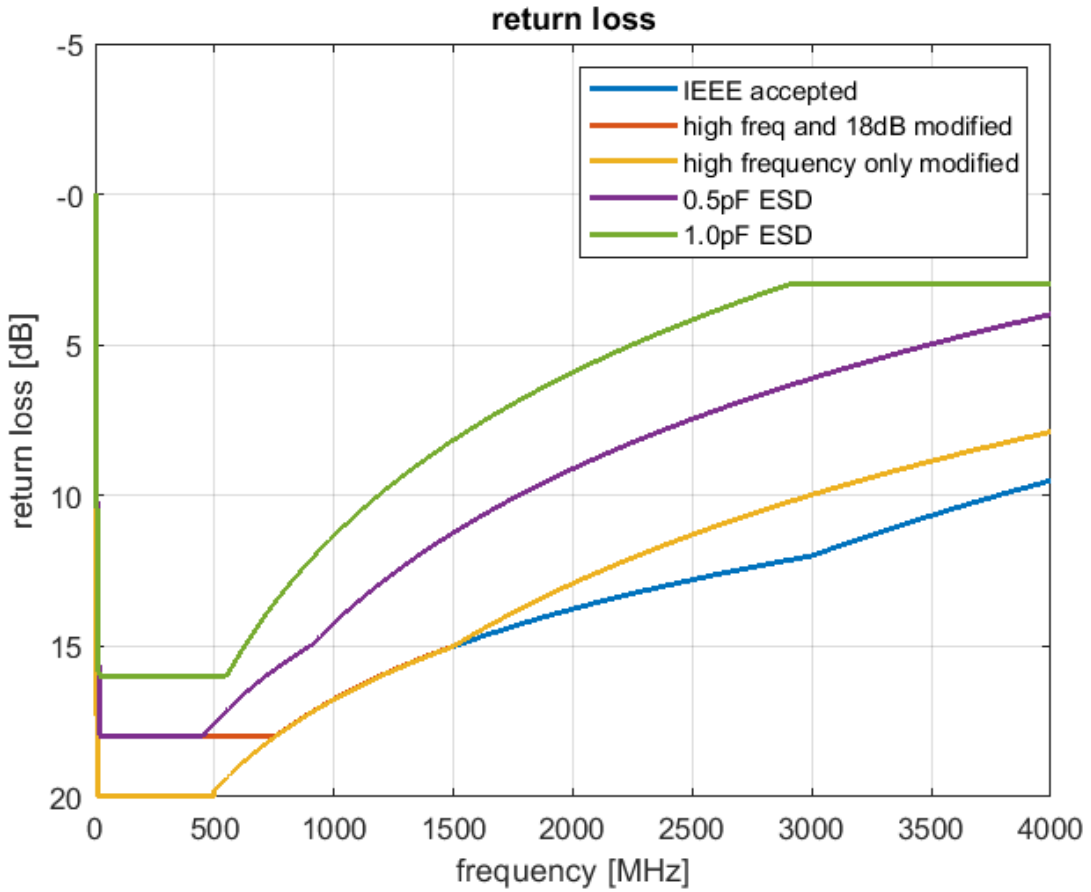
$$\text{MDI return loss} = \begin{cases} 18+18*\log10(f/10) & 1 \le f<10 \\ 18 & 10 \le f<750 \\ 18 - 10*\log10(f/750) & 750 \le f<1500 \\ 15 - 16.7*\log10(f/1500) & 1500 \le f<4000 \end{cases}$$

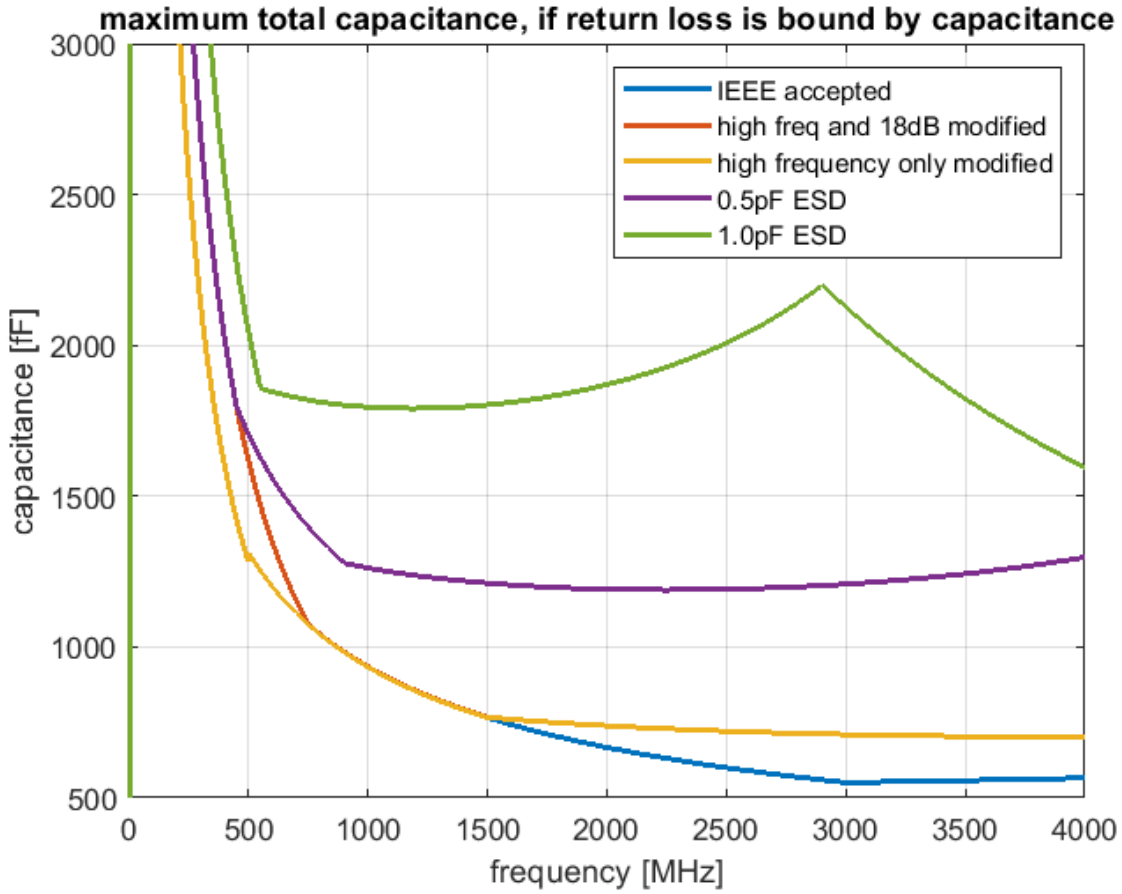
Return loss in dB, frequency in MHz

If the return loss is set by the total capacitance

- C=2*(10.^(-RL/20))./((2*pi*f'*50).*sqrt(1-(10.^(-RL/10))));
- Currently adopted: total single sided capacitance is 550 fF, which may be enough for HBM/CDM, but not for additional PoDL.
- High freq. return loss change accommodates single sided capacitance 700 fF.
- Last proposal accommodates single sided capacitance 1190 fF.

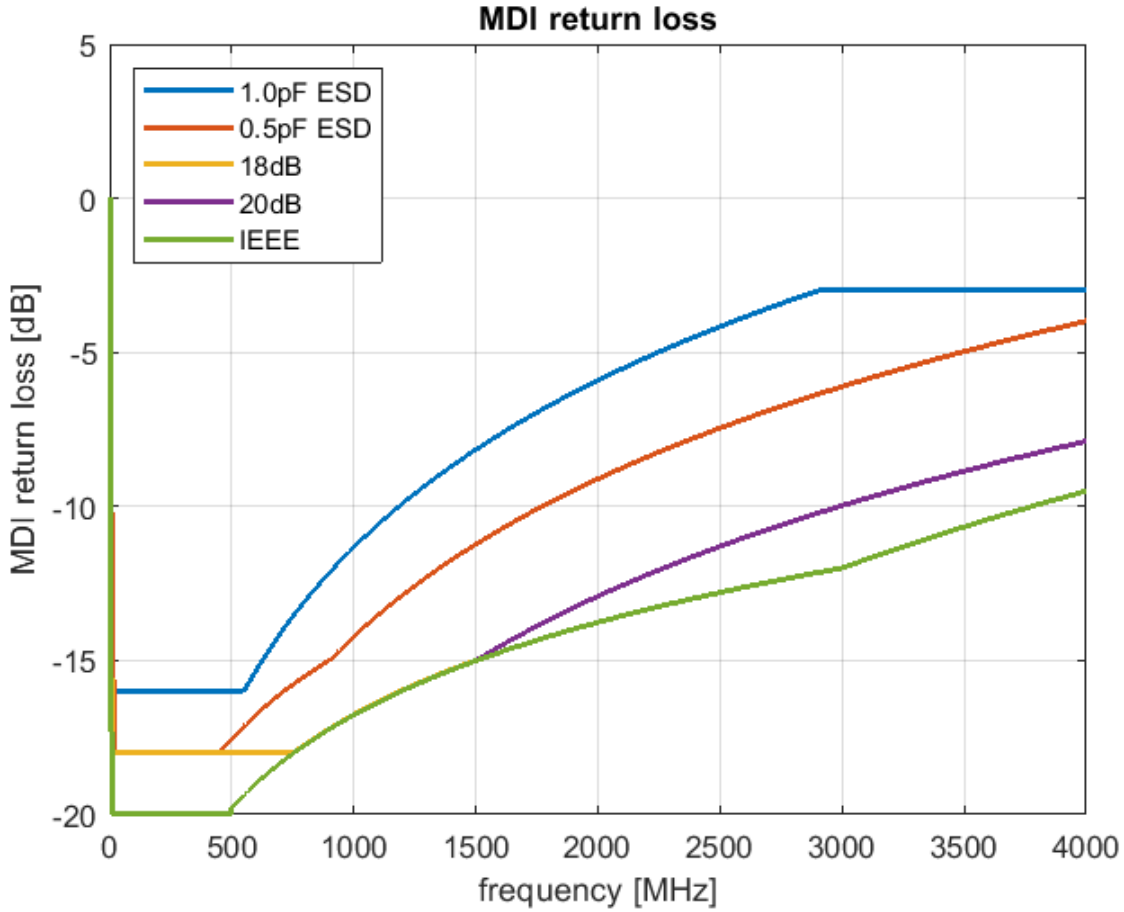
Return loss	Max. cap.
Current IEEE	550 fF
High freq. modified	700 fF
18dB+high freq. mod.	700 fF
0.5pF ESD	1.2 pF
1.0pF ESD	1.6 pF

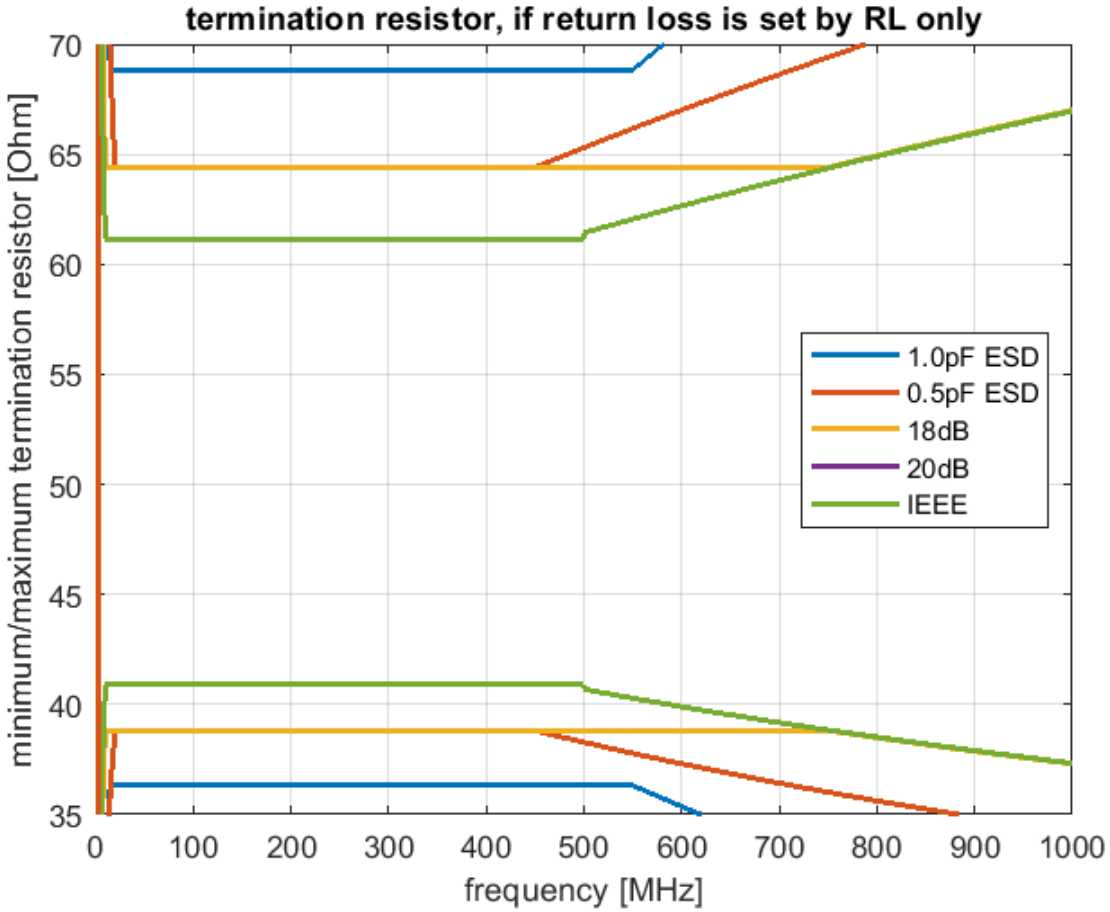




If the return loss was set by the resistance only

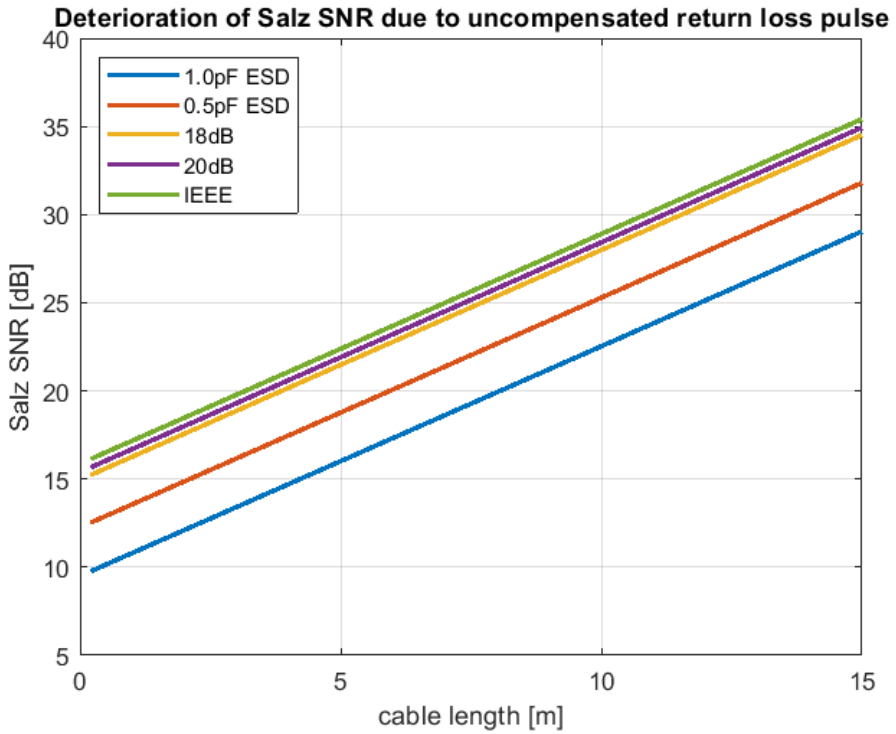
- RL=20*log10(abs((Z0-R)/(Z0+R))), solve for R
- Relaxed MDI return loss spec for design freedom of the TX and variations of the termination resistor.

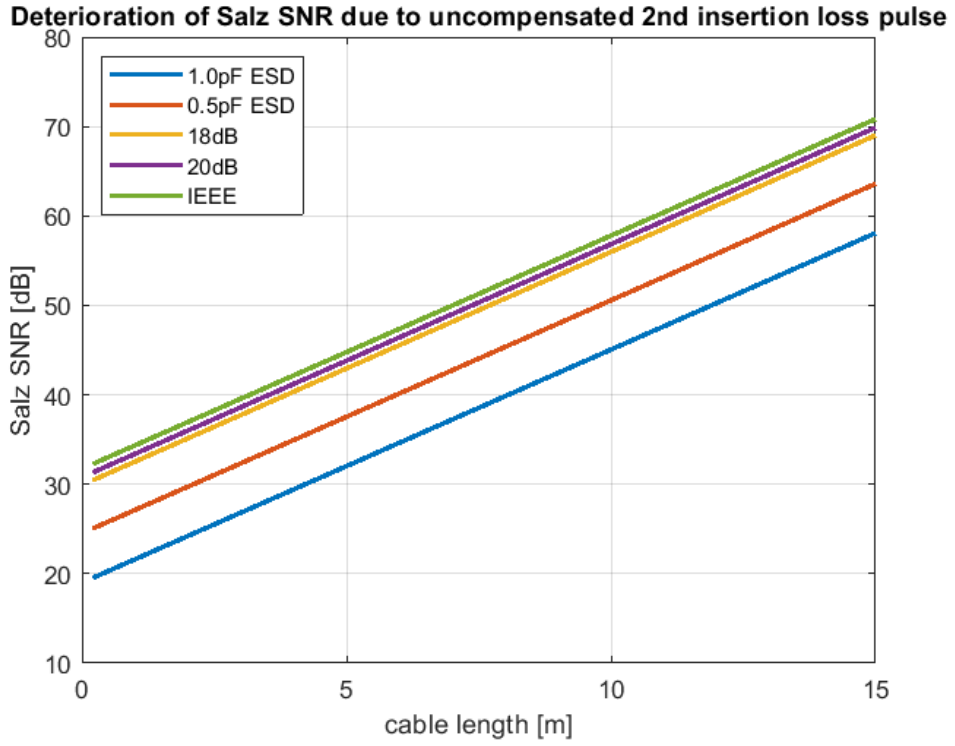




Salz SNR deterioration due to uncompensated pulses

- 2nd pulse of the insertion loss clears 30dB. This means the signal is 30dB higher than the mis-equalization noise from not compensating the 2nd IL pulse.
- Salz SNR from disturbance is calculated as
  - Salz SNR: (transmission signal – disturbance) in dB
  - Echo: (MDI return loss + per length prorated insertion loss)
  - 2nd insertion loss pulse: 2*(MDI return loss + per length prorated insertion loss)





BROADCOM

Salz SNR deterioration due to uncompensated pulses (expanded)

- Number of echo taps increases with relaxing the MDI return loss specification
- Current MDI return loss spec can be relaxed, till 2nd pulse of the insertion loss needs to be compensated.

proposal	capacitance	Supports	Relative extra return loss suppression	Cable length to compensate RL for 30dB	Estimated # of echo taps, assumed: 200e6m/s	Relative extra return loss suppression 2nd insertion loss	Cable length to compensate RL for 30dB	Estimated # of echo taps, assumed: 200e6m/s
1) 1.0pF ESD	1.6pF	IEC/HBM/CDM/PoDL	6.4dB	>15m	844	12.7dB	4.22m	238
2) 0.5pF ESD	1.2pF	IEC/HBM/CDM/PoDL	3.6dB	13.6m	766	7.2dB	2.1m	118
3) 18dB max RL	700fF	HBM/CDM/PoDL	0.91dB	11.5m	650	1.8dB	0.03m	2
4) 20dB max RL	700fF	HBM/CDM/PoDL	0.48dB	11.2m	632	0.95dB		
5) Current IEEE	550fF	HBM/CDM PoDL?	0dB	10.8m	611	0dB		

Conclusion

- Analytical result:
  - The parasitic capacitance has a major influence on the MDI return loss.
  - Higher frequencies for mGig automotive compared to 1000BASET1 increases the severity.
  - Trade-off: Higher allowance for the parasitic capacitance for implementation and ESD protection results in higher complexity in the DSP
    - Longer echo compensation.
    - Compensation of the second insertion loss pulse due to reflections on relatively short cables.
- Suggest to weigh:
  - Technology constraints and ESD requirements.
  - DSP implementation.
- To Do: Experimental results using available board material and varying trace length on the board.

In the current technology PoDL and IEC cannot be supported, if the current MDI return loss specification is not amended.

Thank you.

IEC 61000-4-2

- IEEE standard specifications should not preclude that the device can pass other e.g. ESD protection standards.
- Assumption: for connectors using a metallic connector shell, direct application of discharges to the pins is excluded:
  - IEC 61000-4-2, paragraph 8.3.2 Direct application of discharges to the EUT
    - The following exclusions apply:

    d) the contacts of coaxial and multi-pin connectors which are provided with a metallic connector shell. In this case, contact discharges shall only be applied to the metallic shell of these connectors.