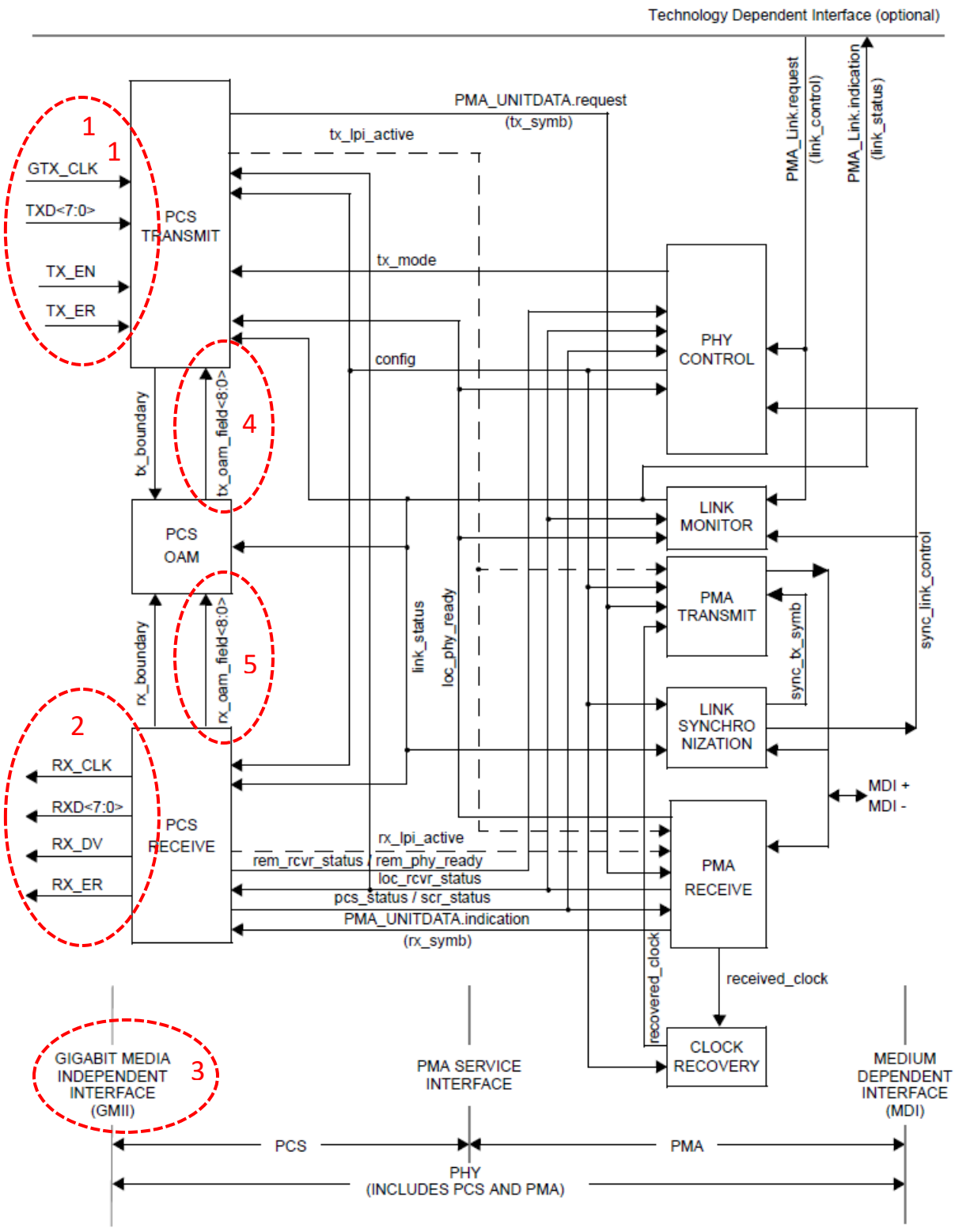
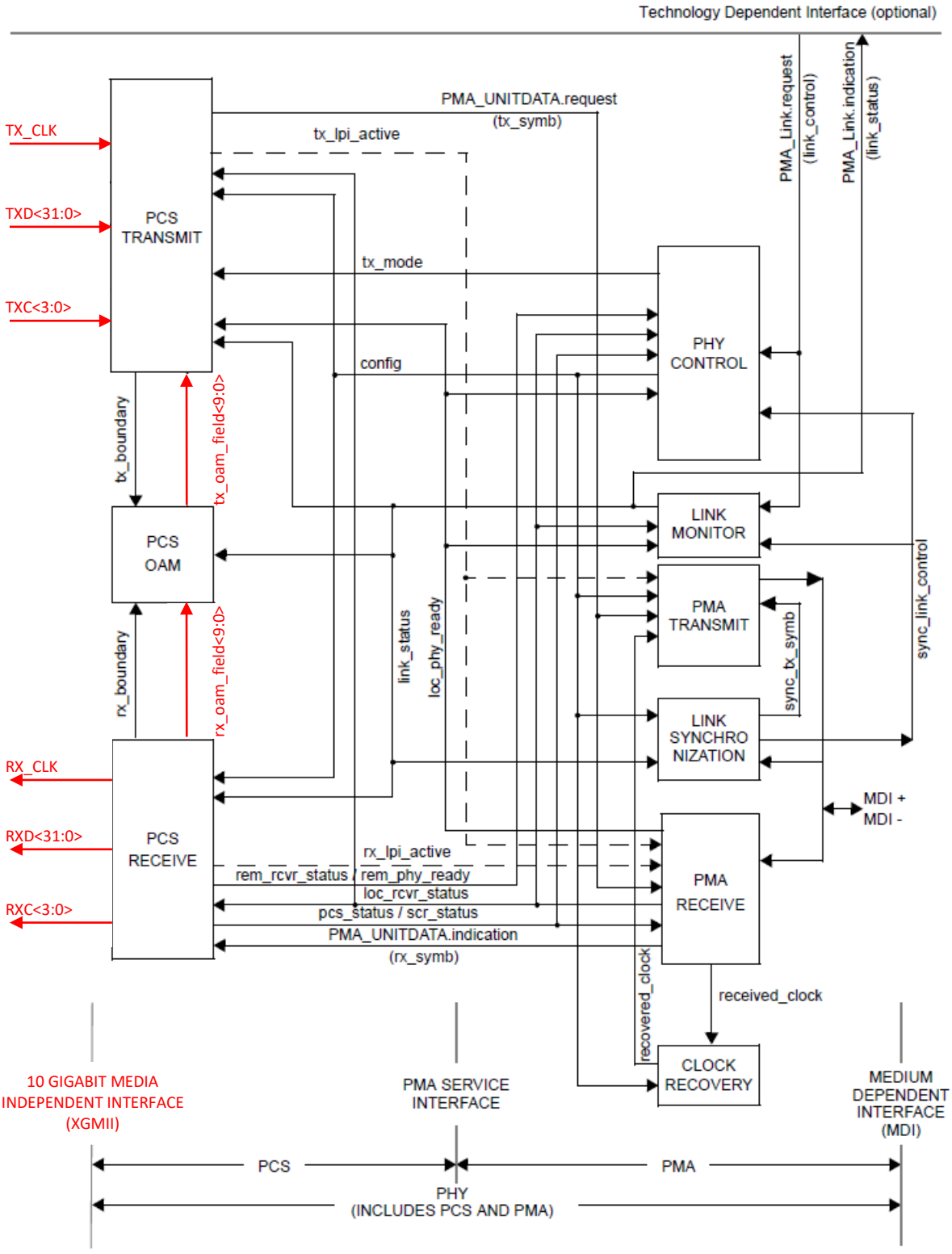


NOTE 1—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing.

NOTE 2—Signals and functions shown with dashed lines are optional.

Figure 97–2—Functional block diagram



NOTE 1—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing.

NOTE 2—Signals and functions shown with dashed lines are optional.

Figure 149-2—Functional block diagram

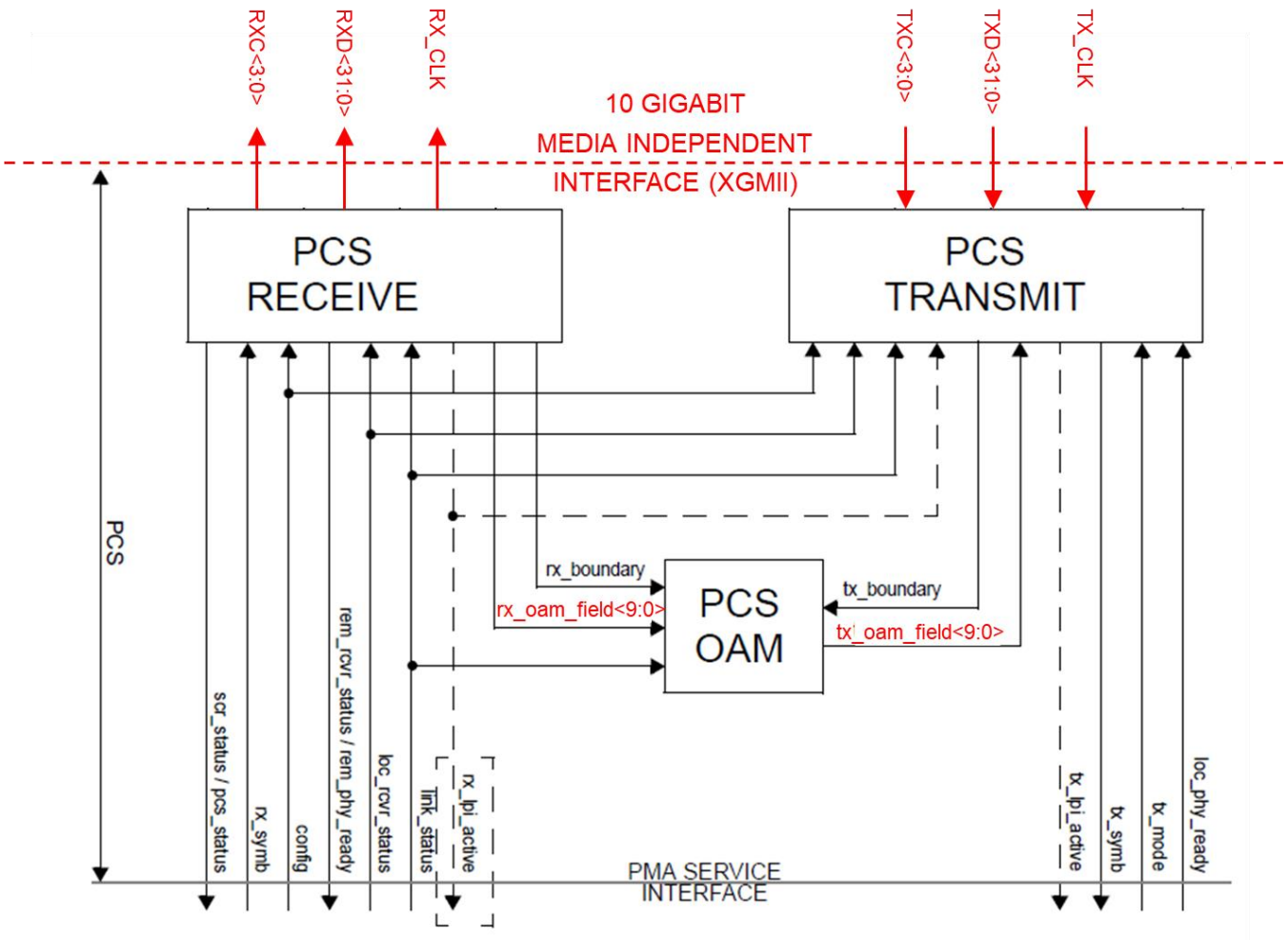


Figure 149-3—PCS reference diagram

149.3.4.1 Generation of Sn

During PMA training, the training pattern is embedded with indicators to establish alignment to the RS-FEC block and the 16 partial PHY frames that comprise the block. The last partial PHY frame is embedded with an information field used to exchange messages between link partners. PMA training signal encoding is based on the generation, at time n, of the bit Sn. The first bit is inverted in the first 15 partial PHY frames of each RS-FEC block. The first 96 bits of the 16th partial PHY frame is XORed with the contents of the InfoField. Each partial PHY frame is 450 bits long, beginning at Sn where (n mod 450) = 0. See Equation (149–8).

$$S_n = \begin{cases} Scr_n[0] \oplus InfoField_{(n \bmod 450)} & 6750 \le (n \bmod 7200) \le 6845 \\ Scr_n[0] \oplus 1 & \text{else if } (n \bmod 450) = 0 \\ Scr_n[0] & \text{otherwise} \end{cases} \quad \text{(149-8)}$$

149.4.2.4 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram description given in Figure 149-20.

During PMA training (TRAINING and COUNTDOWN states in Figure 149-20), PHY Control information is exchanged between link partners with a 12-octet InfoField, which is XORed with the first 96 bits of the 16th partial PHY frame (bits 6750 to 6845) of the PHY frame. The InfoField is also denoted IF. The link partner is not required to decode every IF transmitted but is required to decode IFs at a rate that enables the correct actions prior to the PAM2 to PAM4 transition.

The 12-octet InfoField shall include the fields in 149.4.2.4.2 through 149.4.2.4.8, also shown in the overview Figure 149-nn1, and the more detailed Figure 149-nn2 and Figure 149-nn3. Each InfoField shall be transmitted at least 256 times to ensure detection at link partner.

octet 1	octet 2	octet 3	octet 4/5/6	octet 7	octet 8/9/10	octet 11/12
0xBB	0xA7	0x00	PFC24	Message	MSG24	CRC16

Figure 149-nn1—InfoField format

octet 1	octet 2	octet 3	octet 4/5/6	octet 7	octet 8/9/10	octet 11/12
0xBB	0xA7	0x00	PFC24	Message	UsrCfgCap	CRC16

Figure 149-nn2—InfoField TRAINING format

octet 1	octet 2	octet 3	octet 4/5/6	octet 7	octet 8/9/10	octet 11/12
0xBB	0xA7	0x00	PFC24	Message	DataSwPFC24	CRC16

Figure 149-nn3—InfoField COUNTDOWN format

149.4.2.4.1 InfoField notation

For all the InfoField notations in the following subclauses, Reserved<bit location> represents any unused values and shall be set to zero on transmit and ignored when received by the link partner. The InfoField is transmitted following the notation where the LSB of each octet is sent first and the octets are sent in increasing number order (that is, the LSB of Oct1 is sent first).

149.4.2.4.2 Start of Frame Delimiter

The start of Frame Delimiter consists of 3 octets [Oct1<7:0>, Oct2<7:0>, Oct3<7:0>] and shall use the hexadecimal value 0xBBA700. 0xBB corresponds to Oct1<7:0> and so forth.

149.4.2.4.3 Partial PHY frame Count (PFC24)

The start of partial PHY frame Count consists of 3 octets [Oct4<7:0>, Oct5<7:0>, Oct6<7:0>] and indicates the running count of partial PHY frames sent LSB first. There are 16 partial PHY frames per PHY frame and the InfoField is embedded within the 16th partial PHY frame. The first partial PHY frame is zero, thus the first partial PHY frame count field after a reset is 15.

149.4.2.4.4 Message Field

Message Field (1 octet). For the MASTER, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, en_slave_tx<4>, reserved<3:0>}. For the SLAVE, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, timing_lock_OK<4>, reserved<3:0>}.

The two state-indicator bits PMA_state<7:6> shall communicate the state of the transmitting transceiver to the link partner. PMA_state<7:6> = 00 indicates TRAINING, and PMA_state<7:6> = 01 indicates COUNTDOWN.

All possible Message Field settings are listed in Table 149-tt1 for the MASTER and Table 149-tt2 for the SLAVE. Any other value shall not be transmitted and shall be ignored at the receiver. The Message Field setting for the first transmitted PMA frame shall be the first row of Table 149-tt1 for the MASTER and the first or second row of Table 149-tt2 for the SLAVE. Moreover, for a given Message Field setting, the next Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the current setting. When loc_rcvr_status = OK the InfoField variable is set to loc_rcvr_status<5> = 1 and set to 0 otherwise.

[To Editor: please copy Table 97-7 as Table 149-tt1, and copy Table 97-8 as Table 149-tt2.]

Table 149-tt1 – InfoField message field valid MASTER settings

PMA_state<7:6>	loc_rcvr_status	en_slave_tx	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

Table 149-tt2 – InfoField message field valid SLAVE settings

PMA_state<7:6>	loc_rcvr_status	timing_lock_OK	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

149.4.2.4.5 PHY Capability Bits

When PMA_state<7:6> = 00, then [0ct8<7:0>, 0ct9<7:0>, 0ct10<7:0>] contains the PHY capability bits. Each octet is sent LSB first. See Table 149-tt3 for the details.

Table 149-tt3 – PHY Capability Bits

octet 8								octet 9								octet 10							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
Reserved															EEEen	OAMen	Depth Interleaver			PrecodeSel	Reserved	Reserved	Reserved

The format of PHY capability bits is Oct9<7> = EEEen, Oct10<0> = OAMen, Oct10<2:1> = InterleaverDepth, and Oct10<4:3> = PrecodeSel. EEEen and OAMen indicate EEE and 1000BASE-T1 OAM capability enable, respectively. The PHY shall indicate the support of these two optional capabilities by setting the corresponding capability bits.

InterleaverDpeth indicates the requested data mode interleaving depth and PrecodeSel indicates the requested data mode precoder.

The remaining bits shall be reserved and set to 0.

149.4.2.4.6 Data Switch partial PHY frame Count

When PMA_state<7:6> = 01, then [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains the data switch partial PHY frame count (DataSwPFC24) sent LSB first. DataSwPFC24 indicates the partial PHY frame count when the transmitter switches from PAM2 to PAM4, which occurs at the start of an RS-FEC superframe. The last value of PFC24 prior to the transition is DataSwPFC24 - 1. DataSwPFC24 shall be set to an integer multiple of 16. This value of DataSwPFC24 guarantees that the switch from PAM2 to PAM4 occurs on a PHY frame boundary.

149.4.2.4.7 Reserved Fields

When PMA_state<7:6> is greater than 01, then [Oct8<1:0>, Oct9<1:0>, Oct10<7:0>] contains a reserved field. All InfoField fields denoted Reserved are reserved for future use.

149.4.2.4.8 CRC16

CRC16 (2 octets) shall implement the CRC16 polynomial (x+1)(x15+x+1) of the previous 7 octets, Oct4<7:0>, Oct5<7:0>, Oct6<7:0>, Oct7<7:0>, Oct8<7:0>, Oct9<7:0>, and Oct10<7:0>. The CRC16 shall produce the same result as the implementation shown in Figure 149–nn4. In Figure 149–nn4 the 16 delay elements S0,..., S15, shall be initialized to zero. Afterwards Oct4 through Oct10 are used to compute the CRC16 with the switch connected, which is setting

CRCgen in Figure 149–nn4. After all the 7 octets have been processed, the switch is disconnected (setting CRCout) and the 16 values stored in the delay elements are transmitted in the order illustrated, first S15, followed by S14, and so on, until the final value S0.

[To Editor: please copy Figure 97-23 as Figure 149-nn4.]

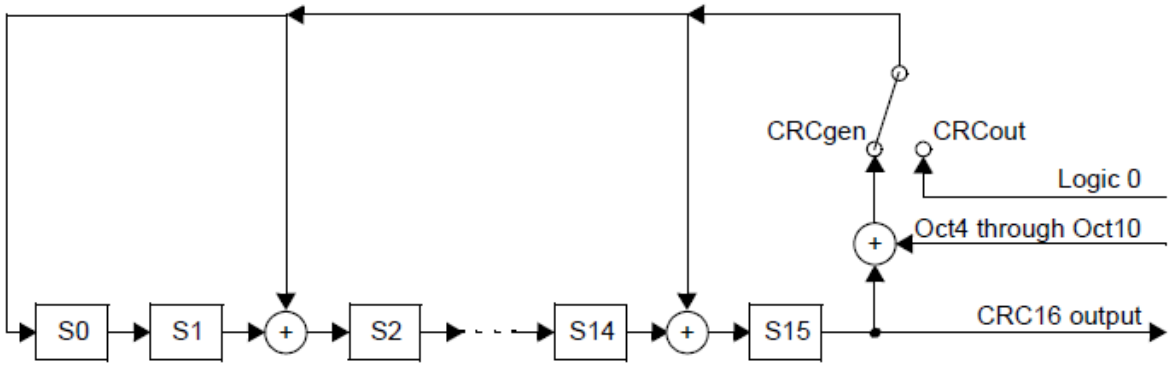


Figure 149-nn4 – CRC16

149.4.2.4.9 PMA MDIO function mapping

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA. Mapping of MDIO control variables to PMA control variables is shown in Table 149–tt4. Mapping of MDIO status variables to PMA status variables is shown in Table 149–tt5.

[To Editor: please copy Table 97-9 as Table 149-tt4 and copy Table 97-10 as Table 149-tt5. Please update the register/bit number and register name accordingly.]

Table 149-tt4—MDIO/PMA control variable mapping

MDIO control variable	PMA register name	Register/bit number	PMA control variable
Reset	Control register 1 / 1000BASE-T1 PMA control register	1.0.15 / 1.2304.15	pma_reset
Transmit disable	1000BASE-T1 PMA control register	1.2304.14	PMA_transmit_disable

Table 149-tt5—MDIO/PMA status variable mapping

MDIO status variable	PMA register name	Register/bit number	PMA status variable
Receive fault	1000BASE-T1 PMA status register	1.2305.1	PMA_receive_fault