149.3.7 Register Update per Comment #74

Natalie Wienckowski, GM

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IEEE802.3ch Interim

149.3.7.1 Status

PCS_status:
Indicates whether the PCS is in a fully operational state. It is only true if block_lock is true and hi_rfer is false. This status is reflected in MDIO register 3.232406.10. A latch low view of this status is reflected in MDIO register 3.2305.2 and the inverse of this status is reflected in MDIO register 3.2305.7.

block_lock:
Indicates the state of the block_lock variable. This status is reflected in MDIO register 3.232406.8. A latch low view of this status is reflected in MDIO register 3.232406.6.

hi_rfer:
Indicates the state of the hi_rfer variable. This status is reflected in MDIO register 3.232406.9. A latch high view of this status is reflected in MDIO register 3.232406.7.

149.3.7.1 Status - continued

Rx LPI indication:
For EEE capability, this variable indicates the current state of the receive LPI function. This flag is set to true (register bit set to one) when the PCS Receive state diagram (Figure TBD) is in the RECEIVE_LPI or RECEIVE_WAKE states. This status is reflected in MDIO register 3.232305.8. A latch high view of this status is reflected in MDIO register 3.232305.10 (Rx LPI received).

Tx LPI indication:
For EEE capability, this variable indicates the current state of the transmit LPI function. This flag is set to true (register bit set to one) when the PCS Transmit state diagram (Figure TBD) is in the SEND_LPI or SEND_WAKE states. This status is reflected in MDIO register 3.232305.9. A latch high view of this status is reflected in MDIO register 3.232305.11 (Tx LPI received).

149.3.7.2 Counter

The following counter is reset to zero upon read and upon reset of the PCS. When it reaches all ones, it stops counting. Its purpose is to help monitor the quality of the link.

RFER_count:

X-bit counter that counts each time RFER_BAD_RF of the RFER monitor state diagram (see Figure TBD) is entered. This counter is reflected in MDIO register bits 3.232406.5:0. The counter is reset when register 3.232406 is read by management. Note that this counter counts a maximum of RFER_CNT_LIMIT counts per RFRX_CNT_LIMIT period since the RFER_BAD_RF state can be entered a maximum of RFER_CNT_LIMIT times per RFRX_CNT_LIMIT window.

149.3.7.3 Loopback

The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.~~0~~2322.14 is set to a one. In this mode, the PCS shall accept data on the transmit path from the XGMII and return it on the receive path to the XGMII. In addition, the PCS shall transmit a continuous stream of TBD encoded PAM4 symbols to the PMA sublayer, and shall ignore all data presented to it by the PMA sublayer.

149.5.1 Test Modes

The test modes described as follows shall be provided to allow for testing of the transmitter jitter, transmitter distortion, transmitter PSD, transmitter droop, and BER testing.

These test modes shall be enabled by setting a control register 1.231508.15:13 as shown in Table 149–9. The test modes shall only change the data symbols provided to the transmitter circuitry and do not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.