

Informative PCS Receive Function overview text.

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Summary:

This text is provided to fill in the informative overview paragraphs of the draft. There is one item which is still dependent on decisions in the PHY control (reference to the alignment markers in PMA training) which remains TBD. There should be no technical decisions or new requirements in this text. (the only shall's are references to the state diagrams which are normative anyways).

Proposed Text

149.3.2.3 PCS Receive function

Insert the following text as the first 5 paragraphs for the PCS Receive function to replace the highlighted "Normal PCS Receive function operation TBD." On page 92 line 8 of d1.0a. Highlighted text below should remain highlighted.

The PCS Receive function shall conform to the PCS 64B/65B receive state diagram in Figure 149–xx and the PCS Receive bit ordering in Figure 149–5 including compliance with the associated state variables as specified in 149.3.6.2.2.

The PCS Receive function accepts received code-groups provided by the PMA Receive function via the parameter `rx_symb`. The PCS receiver uses knowledge of the encoding rules and PMA training alignment to correctly align the 65B-RS-FEC frames. The received PAM4 symbols are demapped and descrambling is performed. The 65B-RS-FEC frames are then decoded with Reed-Solomon error correction. The RS-FEC decoded frame is then separated into a 10-bit OAM field, separated from the 64B/65B blocks, and 50 64B/65B blocks. This process generates the 64B/65B block vector `rx_coded<64:0>`, which is then decoded to form the XGMII signals `RXD<31:0>` and `RXC<3:0>` as specified in the PCS 64B/65B Receive state diagram (see Figure 149–TBD and Figure 149–TBD). Two XGMII data transfers are decoded from each block. Where the XGMII and PMA sublayer data rates are not synchronized, the receive process inserts idles, deletes idles, or deletes sequence ordered sets to adapt between rates.

During PMA training mode, PCS Receive checks the received PAM2 framing and signals the reliable acquisition of the descrambler state by setting the `scr_status` parameter of the `PMA_SCRSTATUS.request` primitive to OK.

When the PCS Synchronization process has obtained synchronization, the RS-FEC frame error ratio (RFER) monitor process monitors the signal quality asserting `hi_rfer` if excessive RS-FEC frame errors are detected. If 40 consecutive RS-FEC frame errors are detected, the `block_lock` flag is de-asserted. When `block_lock` is asserted and `hi_rfer` is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates `RXD <31:0>` and `RXC <3:0>` on the XGMII.

When the receive channel is in training mode, the PCS Synchronization process continuously monitors PMA_RXSTATUS.indication (loc_rcvr_status). When loc_rcvr_status indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA.indication primitive. It attains frame and block synchronization based on the PMA training frames and conveys received blocks to the PCS Receive process. The PCS Synchronization process sets the block_lock flag to indicate whether the PCS has obtained synchronization. The PMA training sequence includes 1 bit pattern every 180 PAM2 symbols, which is aligned with the PCS partial PHY frame boundary, as well as an InfoField, which is inserted in the 15th PCS partial PHY frame. When the PCS Synchronization process is synchronized to this pattern, block_lock is asserted.

Editor's Note (to be removed prior to d2.0) : The PMA training sequence and alignment markers needs to be determined and would be found in the PHY control section of the draft (149.4.2.4 and subclauses) section of the draft. When that section is finalized, this statement should be checked and aligned to it.