PCS Changes For Asymmetrical Data Transmission

September 10, 2018

Jim Graba
Tom Souvignier
Mike Tu

Introduction

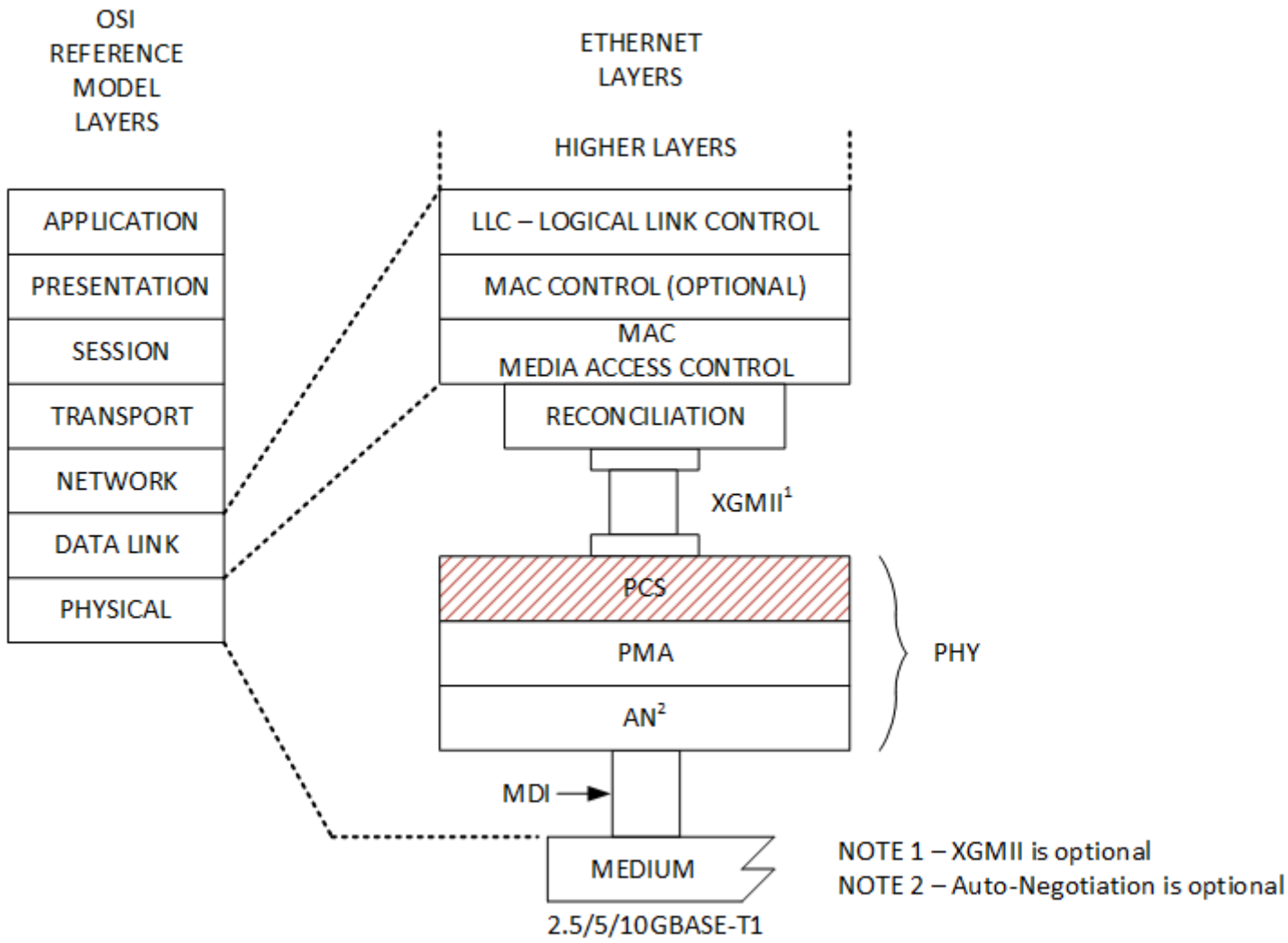
- Need to specify dual speed support in the PCS
  - To support asymmetrical data transmission (see souvignier_3ch_01a_0718.pdf)
- No precedent in BASE-T for asymmetrical data transfer
- Goal is to keep the XGMII
  - Consistent with Options page in Souvignier's presentation
- Leave MAC unchanged

TX Rate	RX Rate
High	High
Low	High
High	Low

- Low – 100 Mb/s average data rate
- High – 2.5/5/10G data rate
  - If both TX and RX are High then both must be at the same data rate

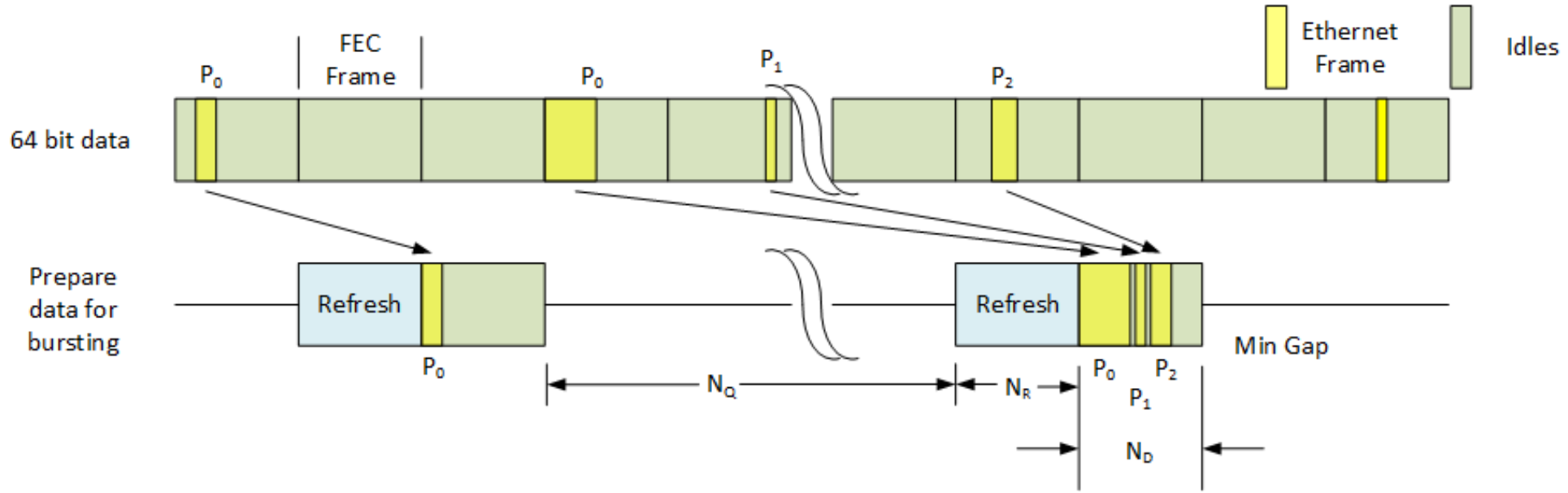
OSI layer diagram

- For reference, combination of draft D0.5 Figures 149-1 and 150-1
- This presentation only discusses PCS



PCS TX – pt 1/2

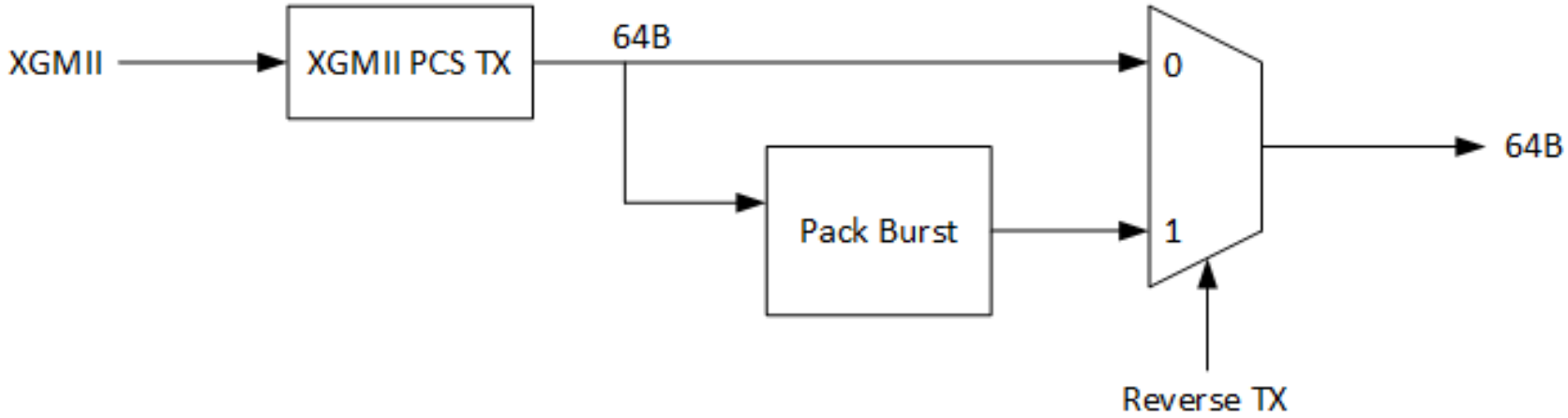
- Concept from souvignier_3ch_01_0718 page 11
- Aggregate Ethernet frames prior to 64/65 bit conversion
- Burst data over one of the reverse FEC frames
- One example below: N_Q = 98, N_R = 1, N_D = 1, Decimate by 1/100
- Essentially LPI mode



BROADCOM

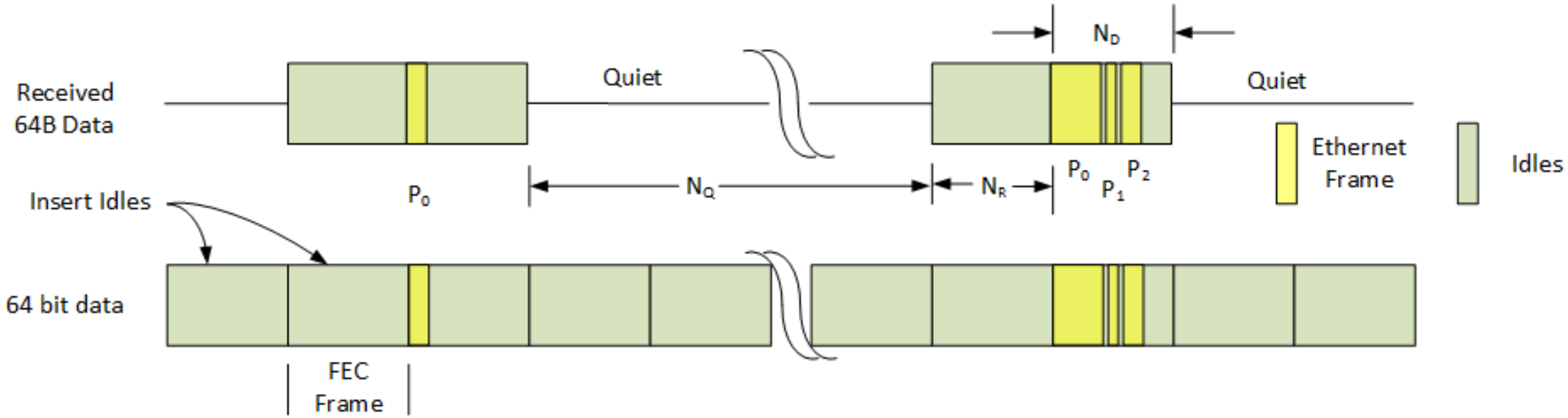
PCS TX – pt 2/2

- Simple addition
- Burst packing controlled by Q/R state machine
- MAC transmits data at the appropriate rate



PCS RX – pt 1/2

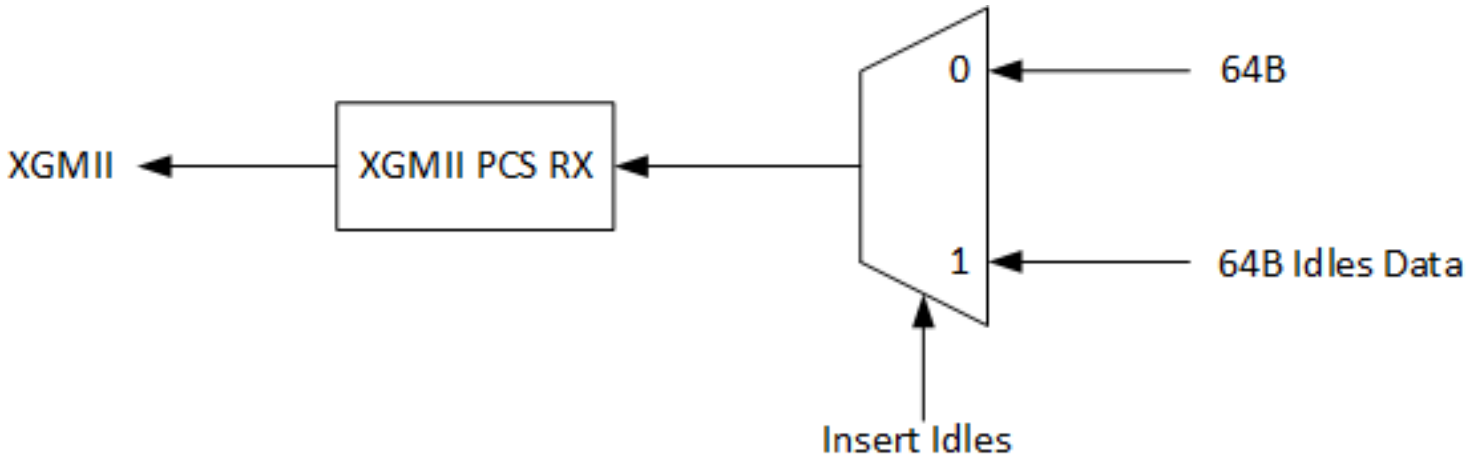
- Quiets are normal inter-frame gaps
- Note minimum gaps in data sent to the MAC
- Minimum latency
- Variable latency
  - 802.3az injects a latency via insertion of Alert and Wake



BROADCOM

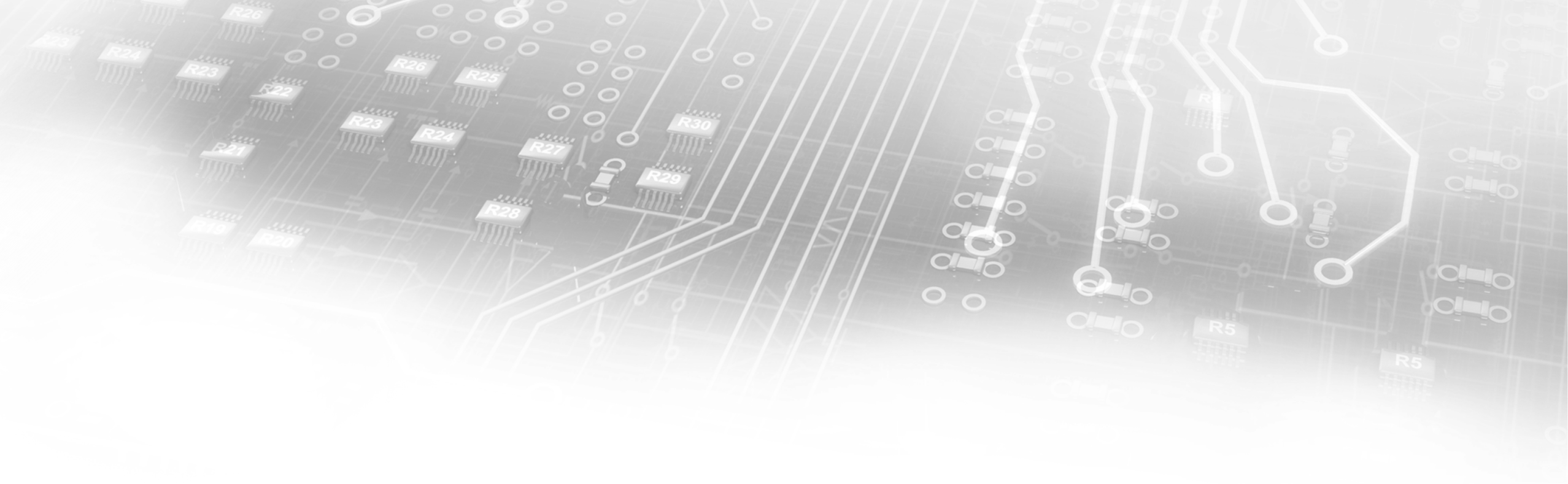
PCS RX – pt 2/2

- Insert Idles during Quiet driven by Q/R state machine
  - Precedent in 802.3az. During RX LPI mode the PCS sends /LI/s over the XGMII
- Burst/Continuous mode transparent to MAC



Summary

- Pack frames by reducing gaps
- Simple modifications to the PCS will support asymmetrical data transmission



THANK YOU