**Interpretation Number:**        2-07/03 (XGXS align status register bits)
Topic:                      XGXS align status register bits
Relevant Clause:        Table 48-7 and 45-49
Classification:           Unambiguous

**Interpretation Request**

1. Related Standard: IEEE Std 802.3ae-2002, clause 45.2.4 and clause 48

It appears that there seems to be a contradiction in the control bit description when using the terms "receive" and "transmit" in clause 45 and clause 48.

In general, clause 48 refers to "transmit" as the direction in which data is sent to XAUI, while "receive" is the direction in which incoming data from XAUI is accepted, synchronized and deskewed. This is clearly stated in Figure 48-2. Additionally, Table 48-7 assigns the state "align_status" to the Management Register Bit "4.8.10 Receive local fault".

In subclause 45.2.4.8.1, the definition of register bit "4.24.12 PHY XGXS lane alignment status" describes this bit as "PHY XGXS <u>transmit</u> lane alignment status". This is a contradiction to the definition given in clause 48. It should better read "PHY XGXS <u>receive</u> lane alignment status", because lane alignment is only done in receive direction and there is no data alignment in transmit direction. Consequently, bit 4.1.2 should be renamed because it is the latched status of bit 4.24.12.

We suggest to change the text in clause 45 to read as:

**45.2.4.2.2 PHY XS <u>receive</u> link status (4.1.2)**

When read as a one, bit 4.1.2 indicates that the PHY XS <u>receive</u> link is aligned. When read as a zero, bit 4.1.2 indicates that the PHY XS <u>receive</u> link is not aligned. The <u>receive</u> link status bit shall be implemented with latching low behavior.

**45.2.4.8.1 PHY XGXS <u>receive</u> lane alignment status (4.24.12)**

When read as a one, bit 4.24.12 indicates that the PHY XGXS has synchronized and aligned all four <u>receive</u> lanes. When read as a zero, bit 4.24.12 indicates that the PHY XGXS has not synchronized and aligned all four <u>receive</u> lanes.

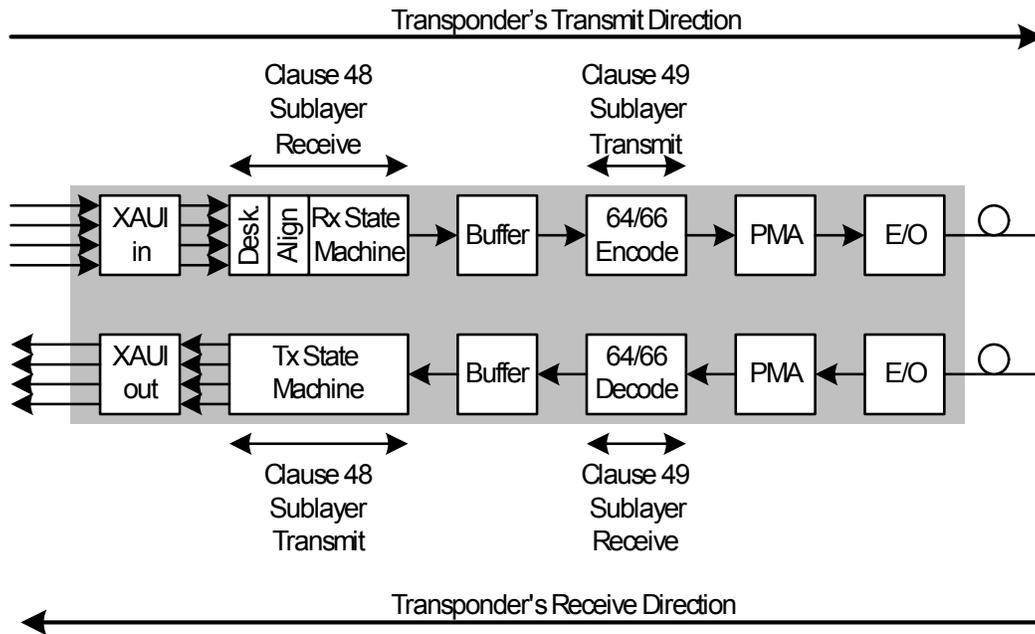**Table 45–46—10G PHY XS status 1 register bit definitions**

| 4.1.2 | PHY XS <u>receive</u> link status | 1 = PHY XS <u>receive</u> link is up<br><br>0 = PHY XS <u>receive</u> link is down | RO/LL |
|---|---|---|---|

**Table 45–50—10G PHY XGXS lane status register bit definitions**

| 4.24.12 | PHY XGXS lane alignment status | 1 = PHY XGXS <u>receive</u> lanes aligned<br><br>0 = PHY XGXS <u>receive</u> lanes not aligned | RO |
|---|---|---|---|

2. Related Standard: IEEE Std 802.3ae-2002, clause 45.2.4 and clause 48

It appears that the description of how to use the terms "receive" and "transmit" is ambiguous, when using the specified sublayer in the following kind of 10GE transceiver application:



It should be made clear that clause 48 "receive" direction always corresponds to data <u>incoming</u> from XAUI (although might be called the transponder's transmit direction) while the "transmit" direction corresponds to data <u>sent</u> to XAUI (which might be called the transponder's receive direction).

This consequently leads to the following interpretation of status bits defined in clause 45.2.4:

Bit 4.8.11 ("Transmit Fault") indicates a fault in the transponder's <u>receive</u> direction.

Bit 4.8.10 ("Receive Fault") indicates a fault in the transponder's <u>transmit</u> direction.

We suggest to change the text in clause 45 to read as:

**45.2.4.6.2 Transmit fault (4.8.11)**

When read as a one, bit 4.8.11 indicates that the PHY XS has detected a fault condition on the transmit path <u>(outgoing data to XAUI)</u>. When read as a zero, bit 4.8.11 indicates that the PHY XS has not detected a fault condition on the transmit path. The transmit fault bit shall be implemented with latching high behavior. The default value for bit 4.8.11 is zero.

**45.2.4.6.3 Receive fault (4.8.10)**

When read as a one, bit 4.8.10 indicates that the PHY XS has detected a fault condition on the receive path <u>(incoming data from XAUI)</u>. When read as a zero, bit 4.8.10 indicates that the PHY XS has not detected a fault condition on the receive path. The receive fault bit shall be implemented with latching high behavior. The default value of bit 4.8.10 is zero.

## Interpretation for IEEE Std 802.3ae-2002

Clause 48 specifies the 10GBASE-X PMA and PCS and does not specify XAUI which, while built upon the 10GBASE-X PMA and PCS specification, is specified in Clause 47. In particular Figure 48-2 illustrates a 10GBASE-X PHY as stated in subclause 48.1.7, and not XAUI.

Within the Clause 47 XAUI specification, subclause 47.2.1 states 'Since the PHY XGXS operates with the XGMII below the XAUI, the transmit requirements of 48.2 and 48.3 apply to the PHY XGXS receive requirements and the receive requirements apply to the PHY XGXS transmit functionality.' As an example of this the PHY XGXS transmit function includes a lane alignment and therefore a PHY XGXS transmit lane alignment status bit is provided in subclause 45.2.4.8.1.

Based on this reversal defined in subclause 47.2.1 the bit definitions related to the PHY XGXS in Clause 45 are correct.