# IEEE802.3at Task Force
# Vport Ad Hoc

## Derivation of minimum TLIM

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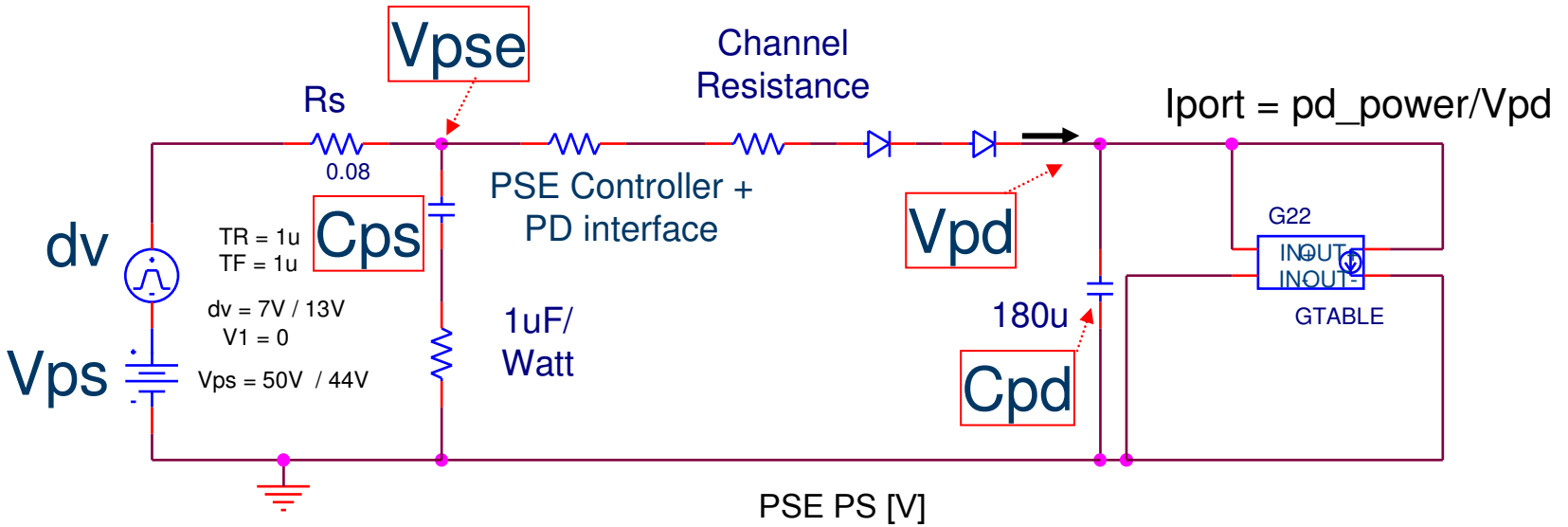
# Objectives

- To analytically determine worst case Minimum $T_{LIM}$.
- Derive Spice Model and simulation results to confirm the analytical calculations.
- Setting Minimum $T_{LIM}$ requirements.

# Who Affects $T_{LIM\_MIN}$ – Simplified Model




From Vport Ad hoc data[1]:

Rs=60 – 80m Ω

PSE controller= 0.9 – 3.2 Ω

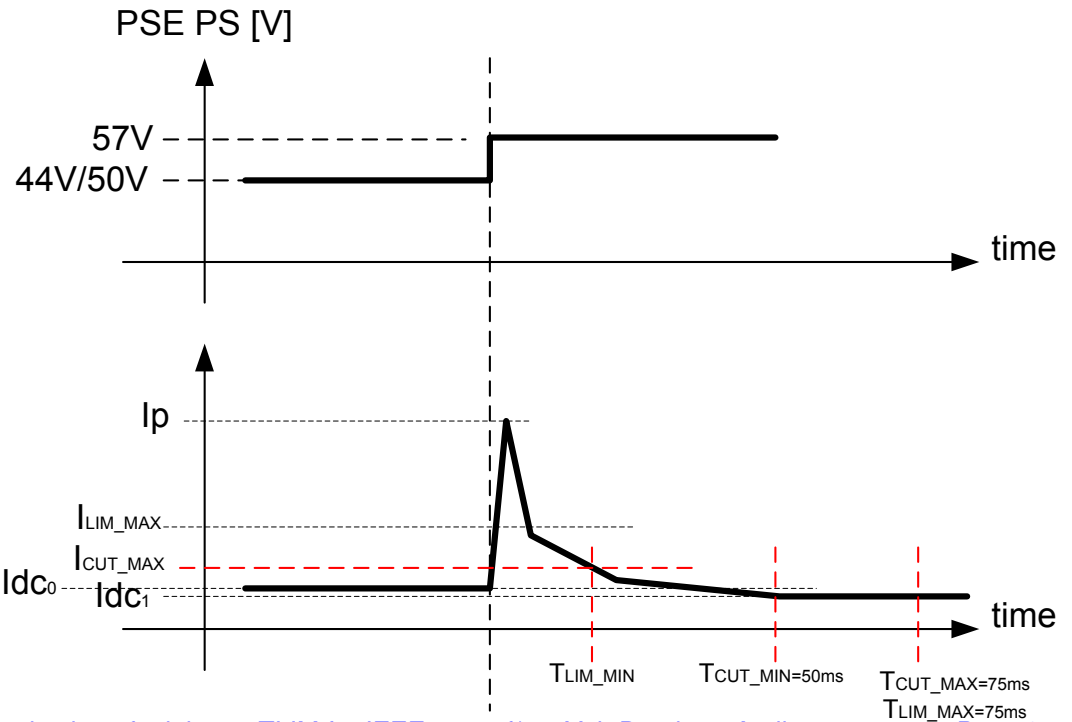
Channel Resistance=0.8 - 12Ω

Cpd=5 -180uF

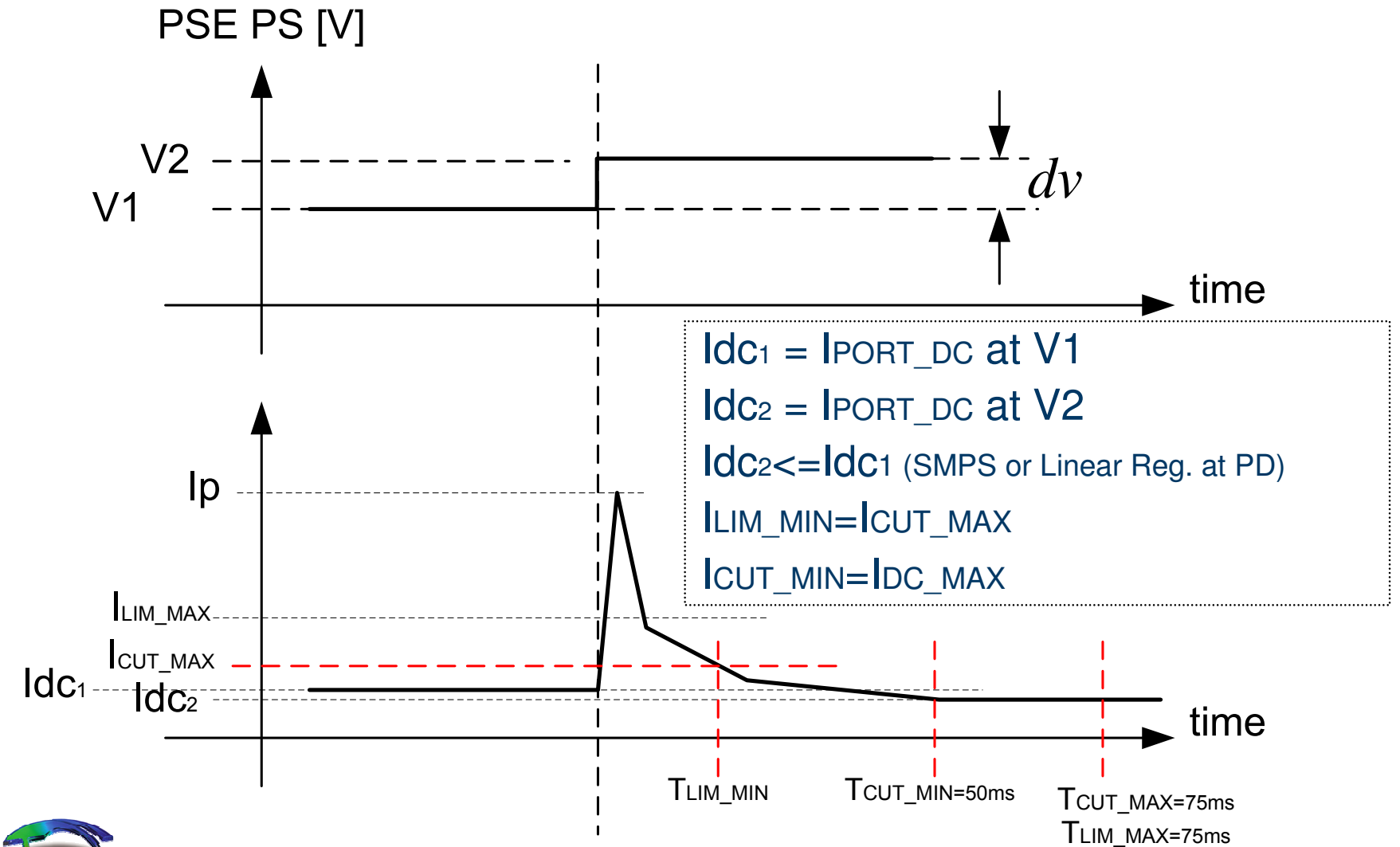
Additional data:

PD Interface: 0.5 – 1Ω

Cps=1uF/Watt=300uF/300Watts



# Who Affects $T_{LIM\_MIN}$ – Simplified Model



# Analytical Derivation of TLIM

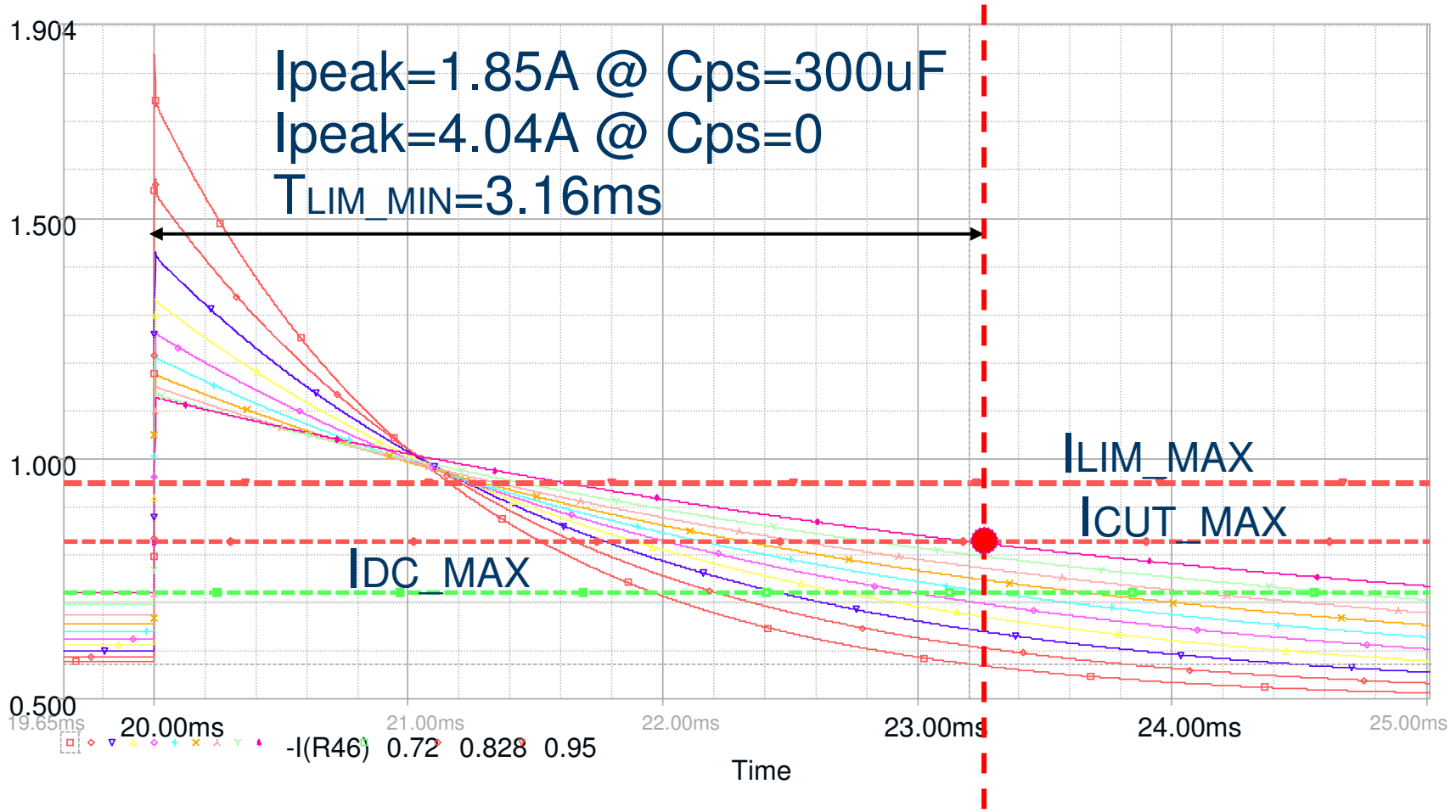
Equation is based on solving differential equation in the current domain and not energy equation.

The energy equation used in last ad-hoc reports is wrong due to the following reasons:

1. The dynamics of the system is differential in two domains: In time and in negative resistance closed loop behavior. The energy equation doesn't address these two domains and creates errors.
2. The energy equation assumes that all energy is transferred to stabilize the new dc voltage at normal operating range which is not true. The operating range that we care is in the boundary between ILIM and ICUT.
3. The above were confirmed by comparing simulation results ("=real hardware") to analytical derivation of TLIM with good match
4. Detailed equation derivation will be presented later.

# Simulation Results:

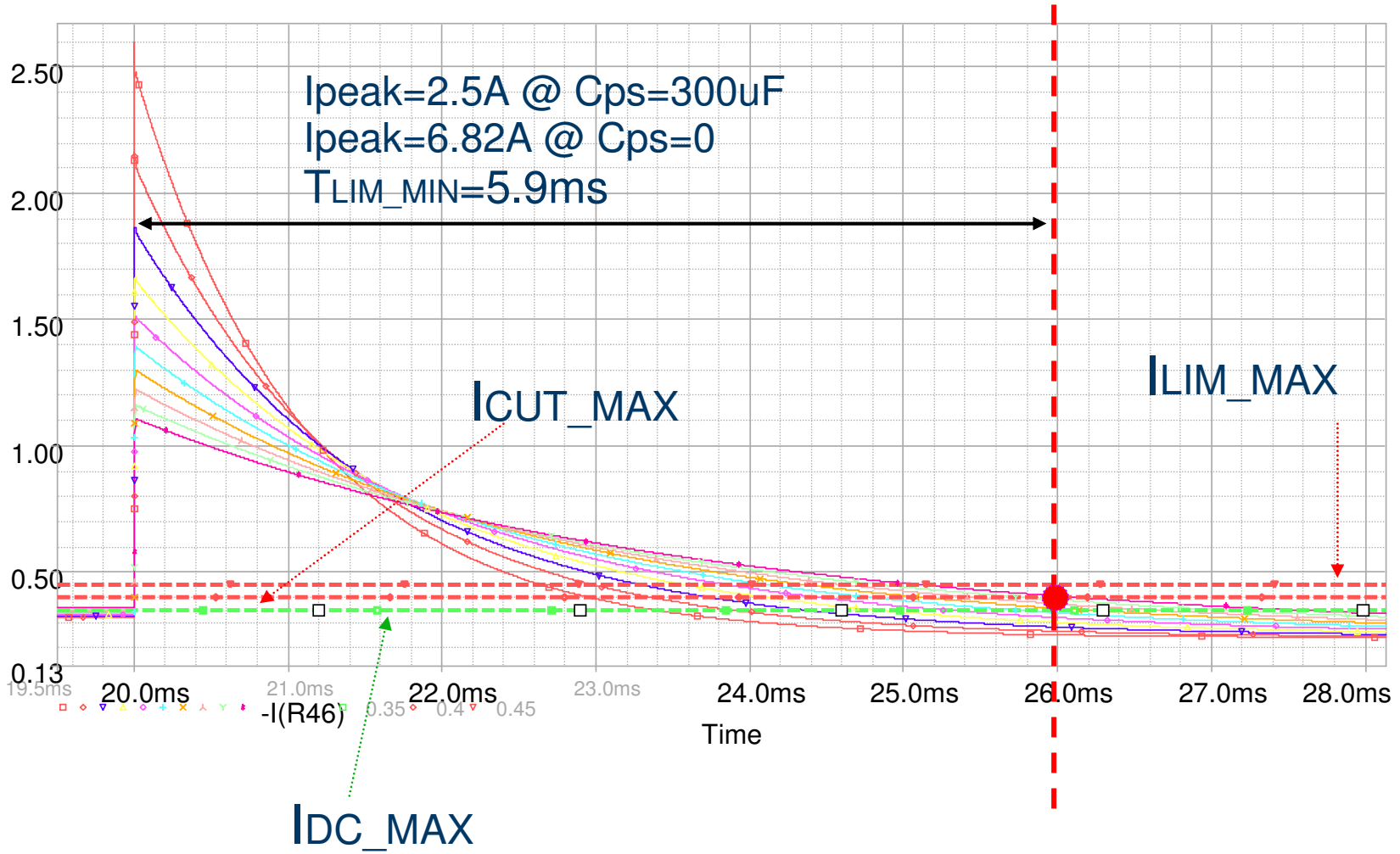
Cpd=180uF, dv=57V-50V=7V, PSE/PD interface at max. Resistance, Channel length varies 0 to 100m




(Tlim_min=2.7ms in analytical derivation)

# Simulation Results:

Cpd=180uF, dv=57V-44V=13V, PSE/PD interface at max. Resistance, Channel length varies 0 to 100m




(Tlim_min=6ms in analytical derivation)

# Worst Case Analytical/Simulation Results – Summary (Cps=0)

| | 802.3at | | 802.3af | |
|---|---|---|---|---|
| **Calculated Results** | $\sum R \rightarrow \min$ . | $\sum R \rightarrow \max$ . | $\sum R \rightarrow \min$ . | $\sum R \rightarrow \max$ . |
| Idc at Vpse_min [A] | 0.560 | 0.722 | 0.292 | 0.330 |
| Idc at Vpse_max [A] | 0.489 | 0.579 | 0.224 | 0.240 |
| di [A] | 3.474 | 0.395 | 6.753 | 0.768 |
| Ipeak [A] | 4.034 | 1.117 | 7.045 | 1.098 |
| Tlim_min [sec] | 0.00084 | 0.0027 | 0.0013 | 0.0060 |
| | | | | |
| **Simulation Results** | | | | |
| Idc at Vpse_min [A] | 0.552 | 0.72 | 0.304 | 0.349 |
| Idc at Vpse_max [A] | 0.479 | 0.569 | 0.231 | 0.248 |
| di [A] | 3.487 | 0.416 | 6.522 | 0.774 |
| Ipeak [A] | 4.039 | 1.136 | 6.827 | 1.122 |
| Tlim_min [sec] | 0.000865 | 0.00316 | 0.00138 | 0.0059 |
| | | | | |
| **Simulation/Calculation Ratio** | | | | |
| Idc at Vpse_min [A] | 0.986 | 0.997 | 1.040 | 1.058 |
| Idc at Vpse_max [A] | 0.980 | 0.983 | 1.029 | 1.035 |
| di [A] | 1.004 | 1.053 | 0.966 | 1.007 |
| Ipeak [A] | 1.001 | 1.017 | 0.969 | 1.022 |
| Tlim_min [sec] | 1.035 | 1.182 | 1.036 | 0.991 |

# Proposal

- TLIM_MIN = 5.9ms. If t<5.9ms port is still ON as long as PD is within operating voltage range. If not, Port can be OFF at any time but not later then 75ms.

- No need for margin.
- Supports worst case PSE PS voltage changes of 13V.
- Covers both 802.3af and 802.3at

# Possible Ilim Curve - example

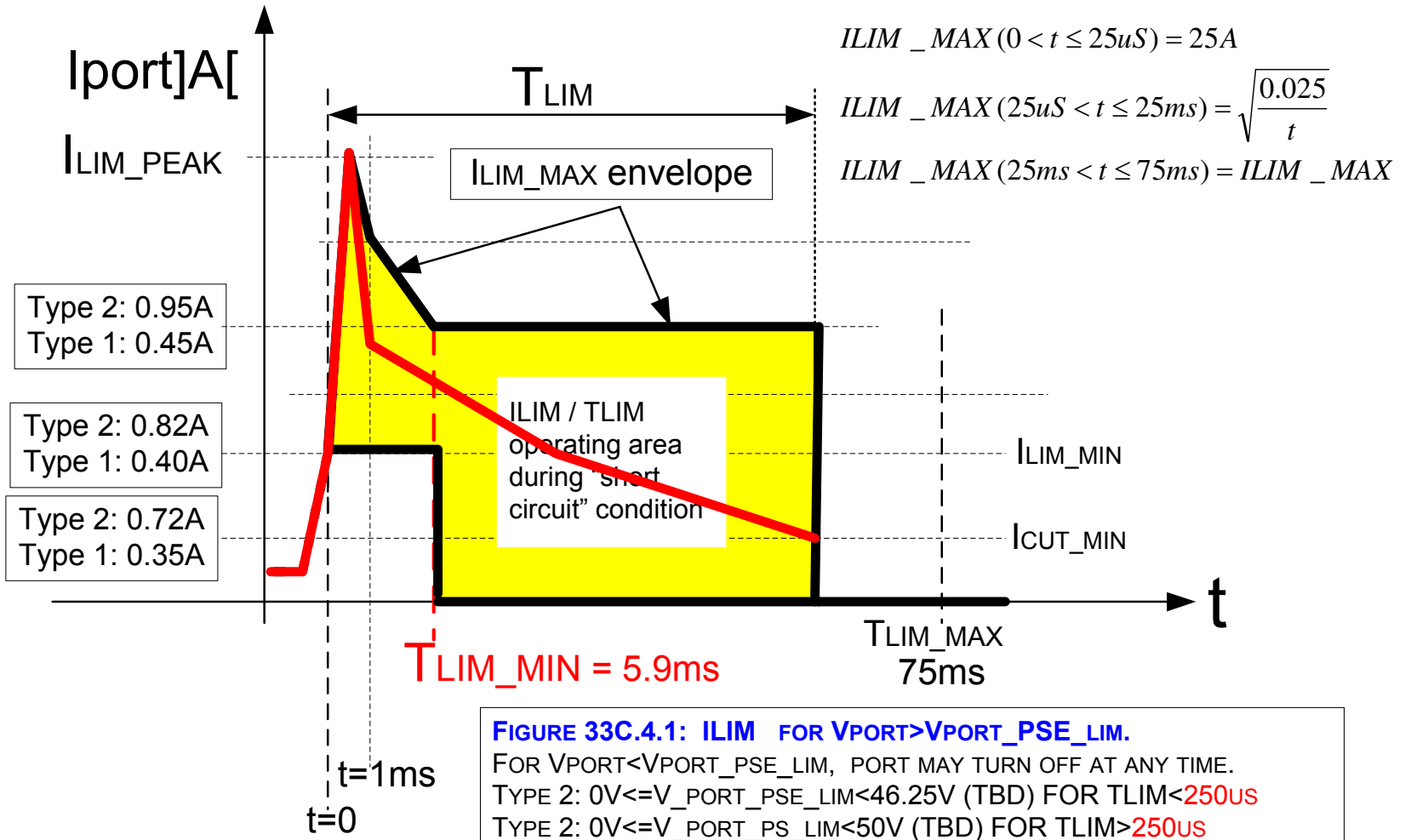



**FIGURE 33C.4.1: ILIM FOR VPORT>VPORT_PSE_LIM.**
FOR VPORT<VPORT_PSE_LIM, PORT MAY TURN OFF AT ANY TIME.
TYPE 2: 0V<=V_PORT_PSE_LIM<46.25V (TBD) FOR TLIM<250US
TYPE 2: 0V<=V_PORT_PS_LIM<50V (TBD) FOR TLIM>250US
TYPE 1: 0V<=VPORT_PSE_LIM<44V (TBD)
SEE SEPARATE DRAWING FOR IINRUSH

# Effects of transient Current on 1206 resistor – Discussion

- Work is not done yet.
- It looks that 1206 can work under the limitations of 33C.4.
- Starting point (from 1206 data sheet):

At 6ms, Ppeak=5W. ➔ I=(5W/1Ω)^0.5

Ipeak =~ 2*I (average of transient)

Using 2 resistors in parallel allows 4*I=8.9A

According to 33C.4:

I=(0.025/0.006)^0.5=2.04A < 8.9A ➔ we are good.

Up to 25us we need to limit peak power to 40W. We need more work to verify it.

Do we have info regarding damaged 1206 in PDs?