Key Assumptions

- **PD current limiting only needs to be done by PDs that go outside the green interoperability zone.**
- **The IEEE specification complaince ensures interoperability.**
- **IEC 60950 compliance ensures safety.**
- **The design space should be opened up.**
- **Requirements should support real systems.**
- **One curve set should support legacy and PoE plus.**

Agreement Areas

- **PSE SOA**
- **Need for PD current threshold tolerance.**
- **Need for PD ripple current.**

Key Difference: How to support PD current ripple

- **PoE plus need for I_{CUT_MAX} for T_{LIM_MIN}?**
  No PD tested for ad hoc work exceed I_{CUT}.
- **The shape of the system interoperability curve for t < 3 ms.**

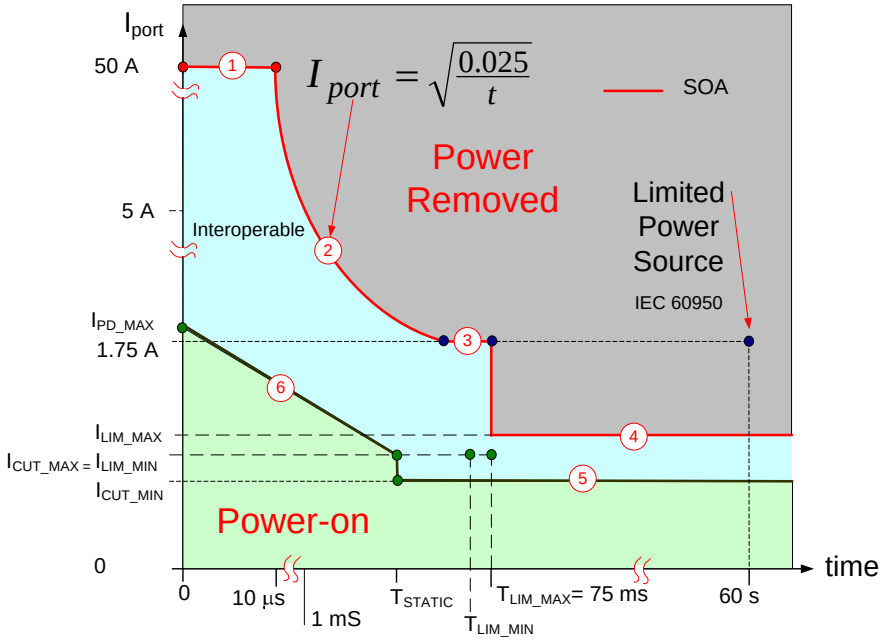
  A square region requires PD current limiting or PSE over design for a generic PD.

  A triangular region allows most PDs to omit current limiting but does not prevent current limiting from being used.

Creating the PSE SOA

(4) Average Current

- **There are no controls on how often a PSE voltage may change due to PD load changes.**
- **The repetition of the worst-case event is unlikely. Therefore, removing power when a PD exceeds P_{CLASS} for at least 1 s is acceptable.**
- **Preserve existing system tolerances,**
  I_{LIM_MAX}/I_{CUT_MIN} = 450/350
  I_{LIM_MIN}/I_{CUT_MIN} = 400/350
- **The long term system cable average is I_{CUT_MIN}.**



I_{LIM_MAX} = 720 x 450/350 = 920 mA

I_{CUT_MIN} = I_{CABLE} = 720 mA

T_{LIM_MIN} = f(I_{LIM})

Creating the PSE SOA

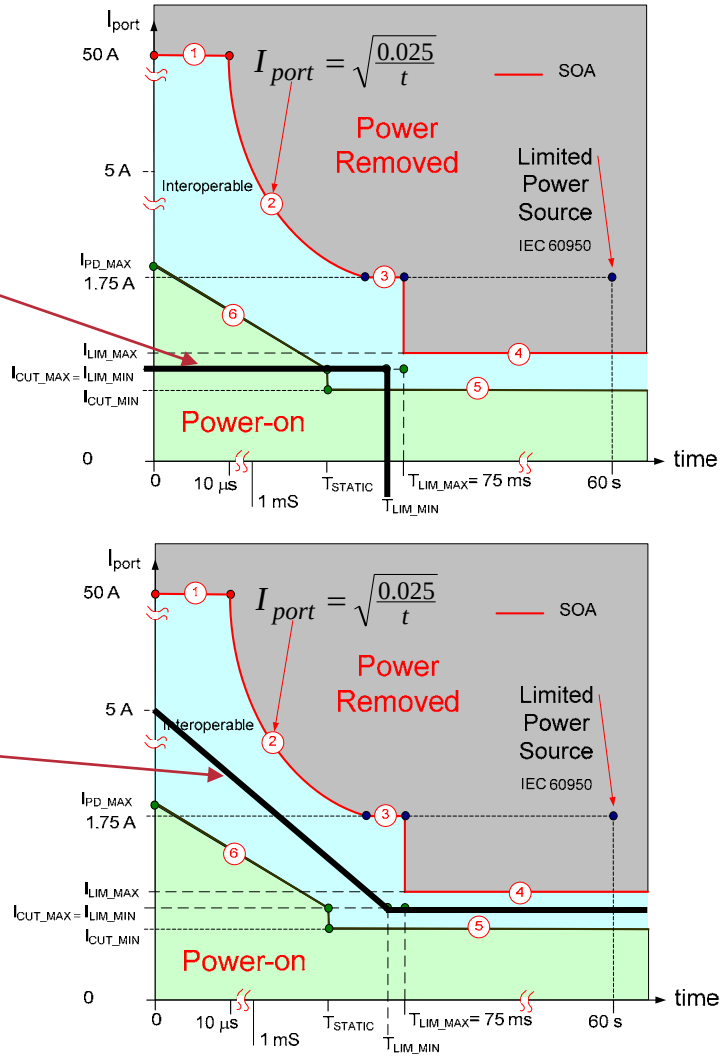
- **A current limiting PSE**

  Provides I_{LIM} for T_{LIM}

  PD power is removed above T_{LIM} or when Pclass has been exceed for 1 s.

- **An energy limiting PSE**

  Provides enough power to ensure the system can operate within the green zone. PD power is removed above the energy base limit.

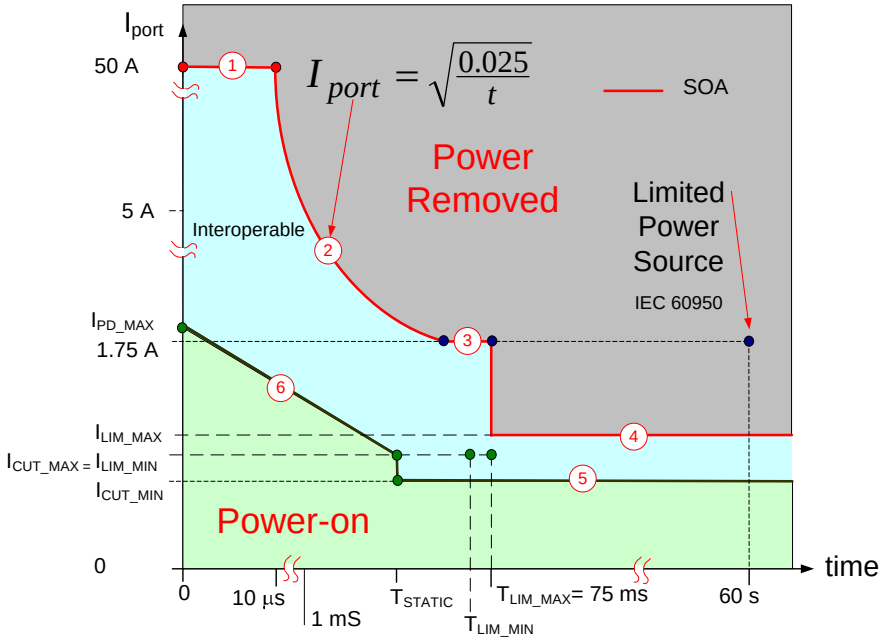


Creating the PD Current Boundary

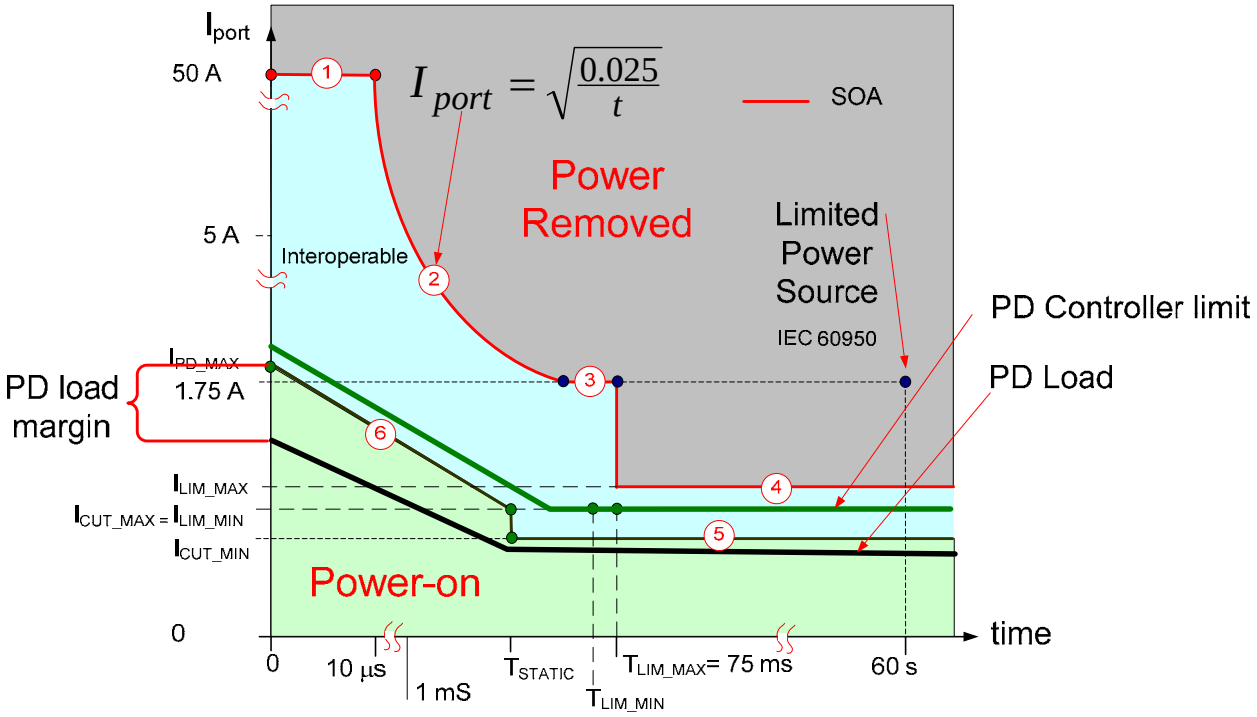
(5) Average Current

- The PD is designed to draw less than I_{CUT_MIN} with a static port voltage.
- PD power compliance may be checked over a period of 1s.
- A PD design must remain within the green zone and this provides “design room.”

  A PD with less capacitance than is permitted will be well below the green boundary. The excess margin can be used to support PD current noise.
- The specification should provide a system model to use.



Creating the PD Current Boundary



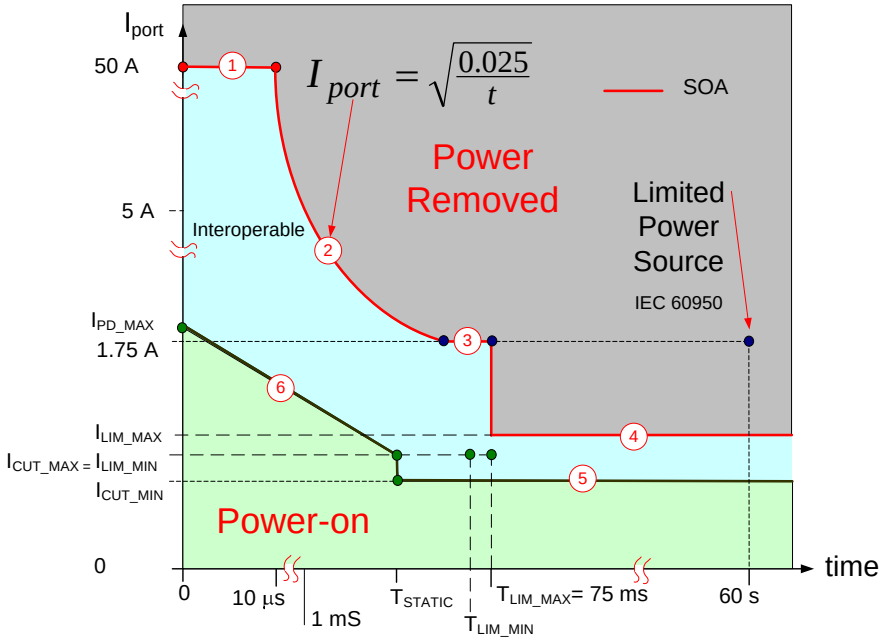
The PD design ensures the average current is within the green zone and may draw the maximum allowable power.

The PD silicon may limit the current above the green zone.

Creating the PD Current Boundary

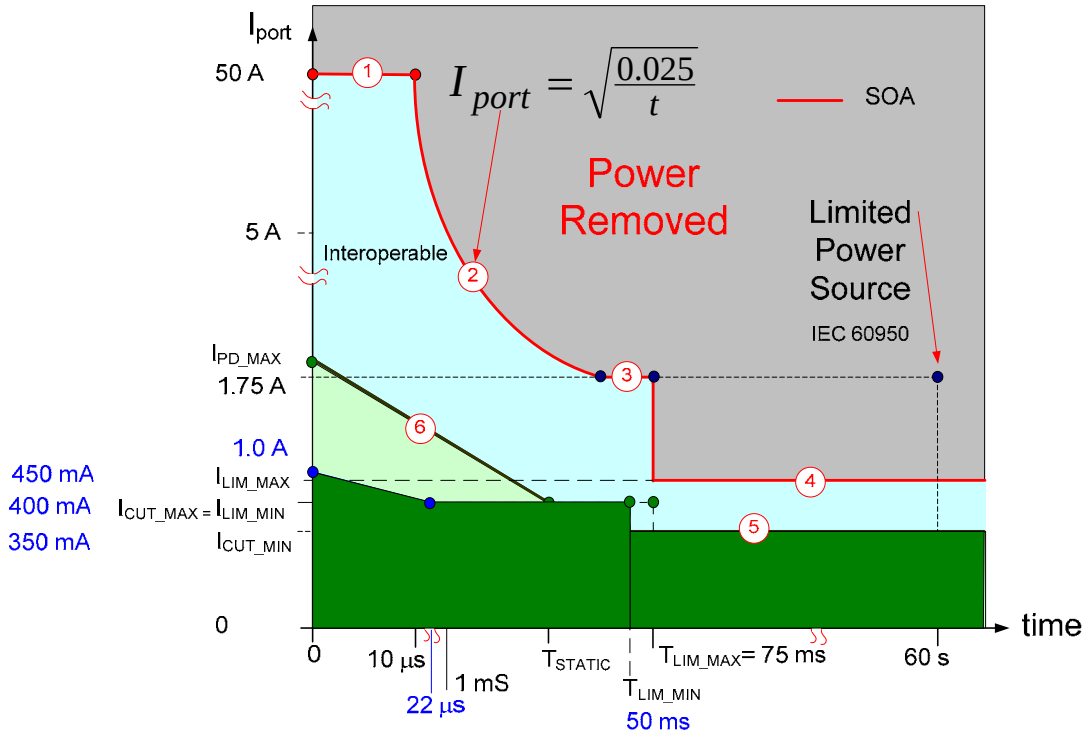
(6) Transient Current

- During permitted system voltage changes the PD shall limit its current to values within the green zone.
- A PD with less capacitance than is permitted will be below the green boundary. The excess margin can be used to support PD current ripple.
- The specification should provide a system model to use.



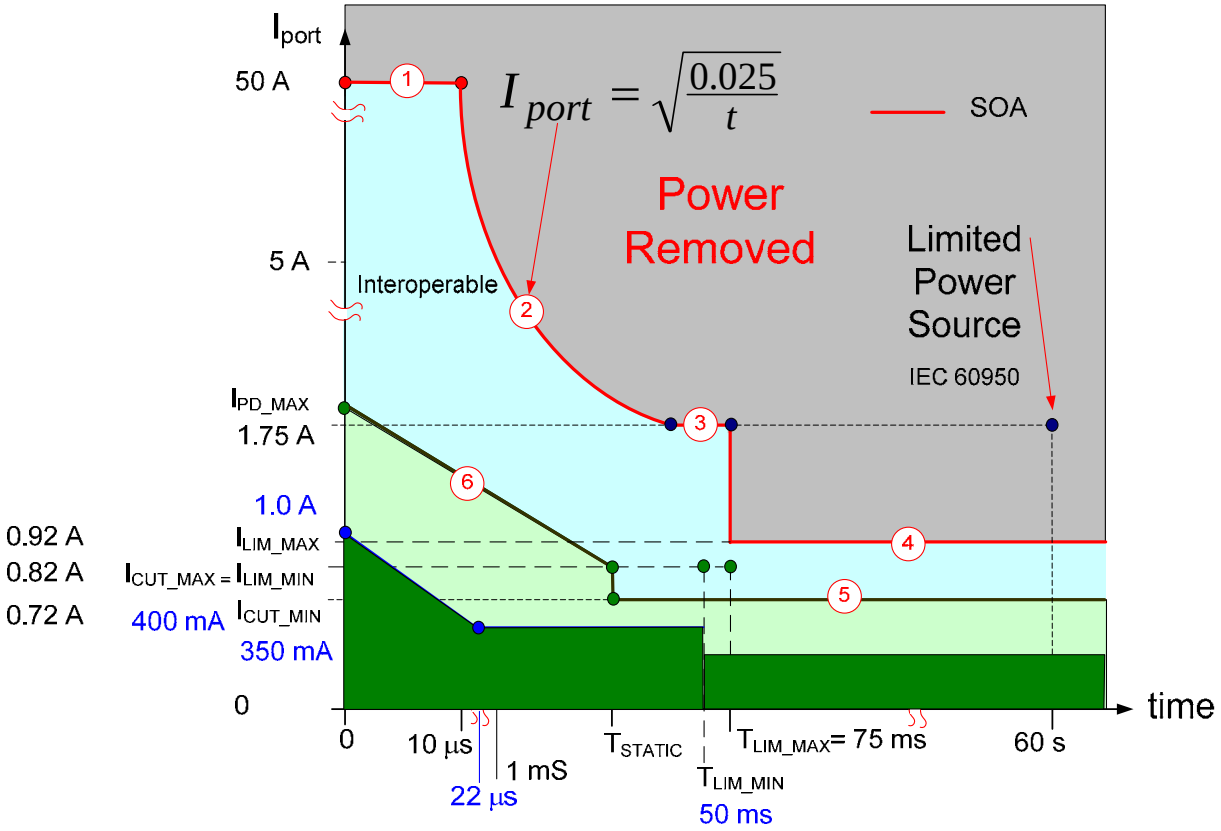
Real PD DC-DC operate near 100 kHz (T = 10µs).
What are our needs for real repetitive current ripple?

Creating the PD Current Boundary



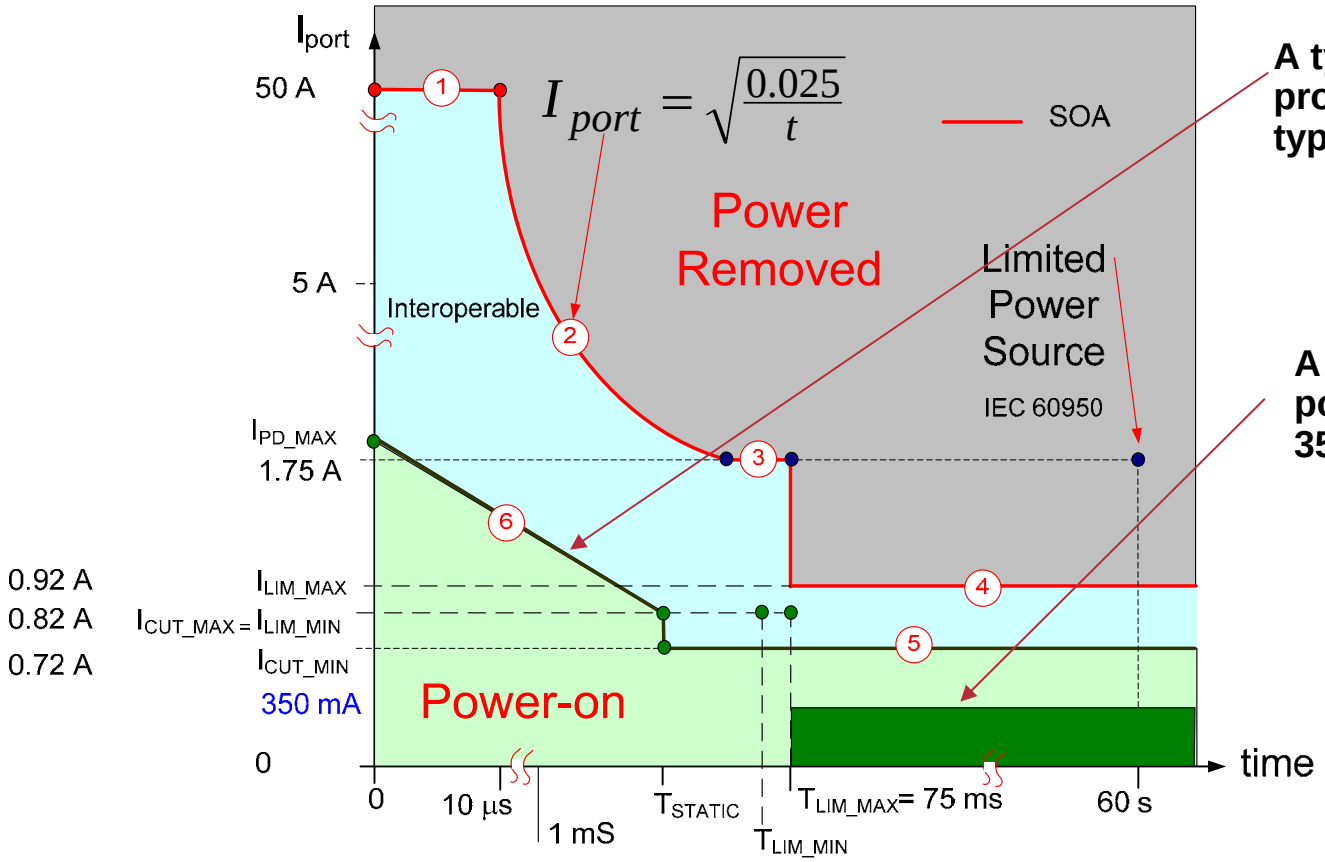
This shows a legacy PD reusing the terminology of the proposed AT curve.

Creating the PD Current Boundary



This shows a legacy PD within the proposed AT curve.

Creating the PD Current Boundary



A type-2 PSE will over provision power for a type-1 PD.

A type-1 PD may have it power removed above 350 mA.

This shows a proposed type-2 PSE AT/legacy curve.