

# DC Current Imbalance

DUE TO CONDUCTIVE AND  
INDUCTIVE ELEMENTS.

By Steve Ellsworth

# What It is

- In a POE LAN interface, current imbalance arises due to the unequal resistance of various segments of the DC current path associated with transferring power from the PSE to the PD.
- The net effect of this current imbalance is the application of a Bias current to the interface transformers associated with the current path.

# The Typical Transformer

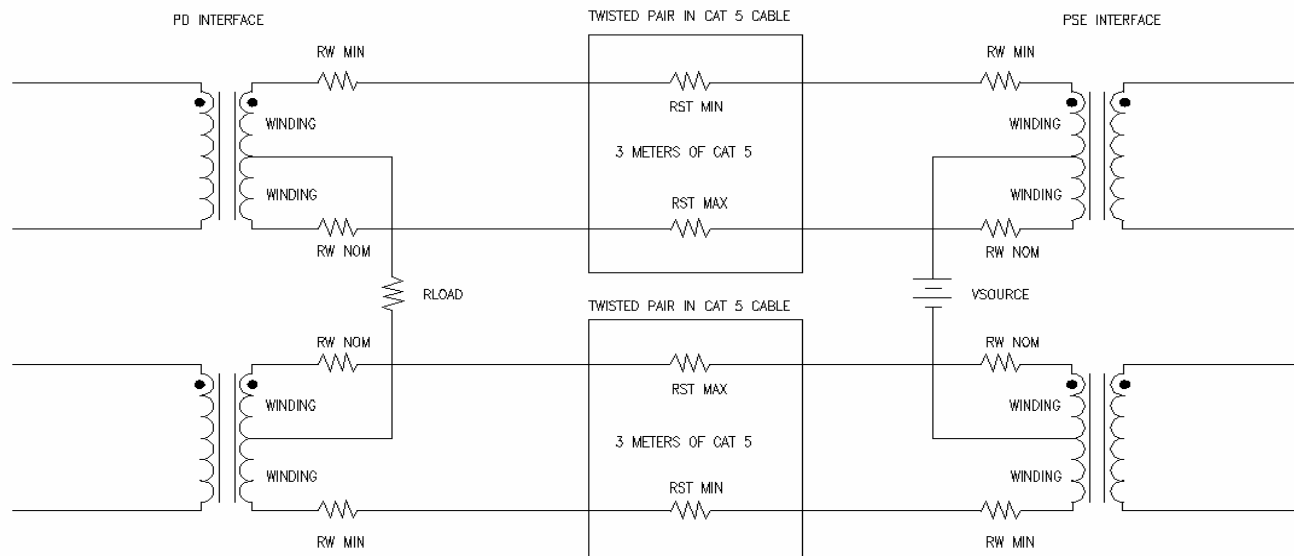
- Ferrite Core and number of turns chosen to yield a transformer which has sufficient bandwidth to meet all IEEE 802.3 requirements. And contemporary size constraints.
- Wire gauge is 39 QPN. (Min to Nom).
- Wire cross sectional area tolerance from Min to Nom. Diameter is 6.5 %.

# The Typical Cable

- 3 Meters of 24 AWG CAT 5e Cable
- 9 ohms/100 Meter
- DCR Imbalance 3.5%

# Worst case conditions

- All Resistances are arranged in the circuit to yield the highest current imbalance i.e. All Minimum Resistances are in series and all Maximum Resistances are in series.
- The interconnect cable is assumed to be minimum length (3 Meters)



# D.C. Current Imbalance

## POE IT IS NOW:

- DC Current Imbalance at a Load Current of 350 mA is 9.2 mA.

## POE AS IT IS PROPOSED:

- DC Current Imbalance at a Load Current of 850 mA is 22.5 mA.

# Negative Effects of current imbalance

- **REDUCTION OF INDUCTANCE:**

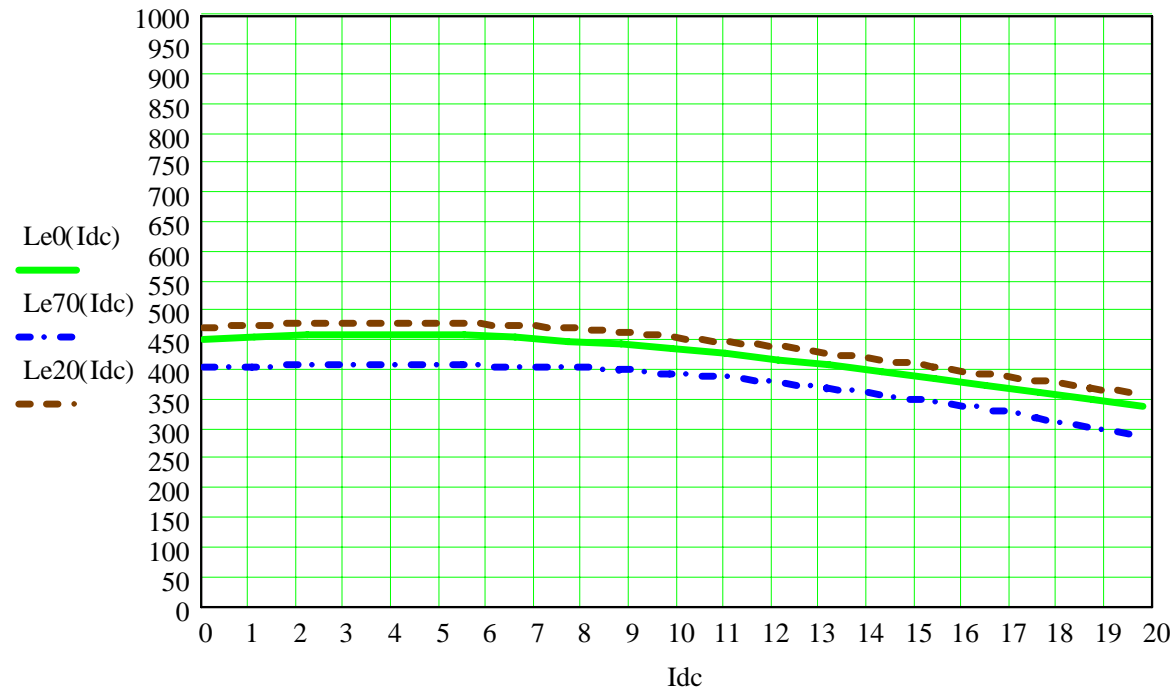
The present IEEE 802.3 requirement for Inductance (OCL) is 350uH @ 8mADC Bias from 0 Degrees C to +70 Degrees C.

For a typical interface transformer the inductance is around 400 uH under worst case Bias and temperature conditions. **With 0 ADC current imbalance.**

# Negative Effects of current imbalance

The following graph shows the relationship between OCL of a typical Interface transformer and DC Bias current.

Effective Inductance vs D.C. Bias @ 0, 20, AND 70 C.  
(uH vs mA)





# Negative Effects of current imbalance

As it can be seen from the previous graph, the minimum transformer inductance spec. of 350  $\mu\text{H}$  cannot be maintained above a 16 mA DC Bias.

As an 8mA DC Bias is an IEEE 802.3 requirement, the remaining overhead for imbalance is 8 mA.

# Negative Effects of current imbalance

## POE IT IS NOW:

- With a DC Current Imbalance of 9.2 mA + 8 mA Bias the OCL of the transformer is 325  $\mu$ H.

## POE AS IT IS PROPOSED:

- With a DC Current Imbalance of 22.5 mA + 8 mA Bias the OCL of the transformer is 156  $\mu$ H.

# Negative Effects of current imbalance

- INCREASE IN WAVEFORM DROOP:

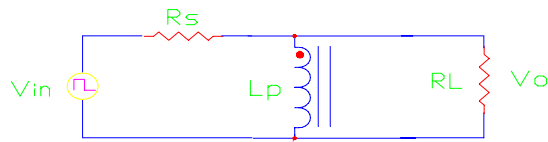


Fig. 1 The circuit.

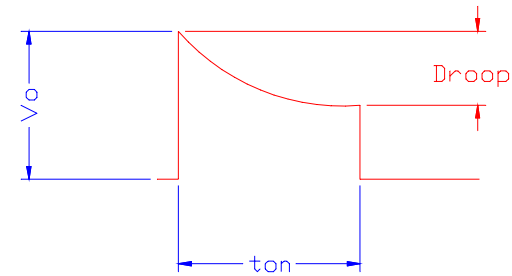


Fig. 2 The output waveform.

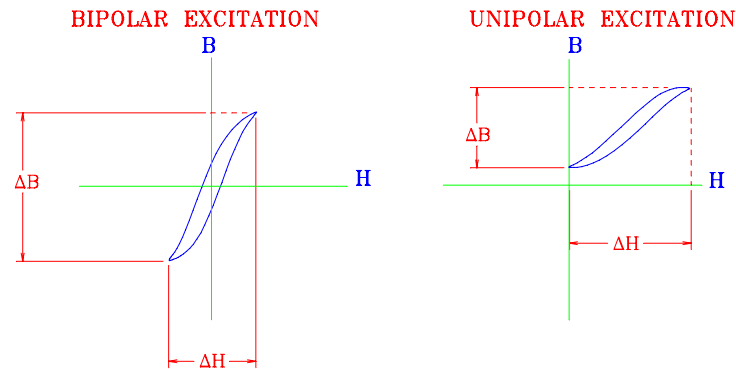


Fig.3 B H loop characteristics for unipolar and bipolar excitations.

# Negative Effects of current imbalance

## POE IT IS NOW:

- With a DC Current Imbalance of 9.2 mA + 8 mA Bias the Waveform Droop of the transformer is at 1000 ns is 9.9 %.

## POE AS IT IS PROPOSED:

- With a DC Current Imbalance of 22.5 mA + 8 mA Bias the Waveform Droop of the transformer at 1000 ns is 15 %.

# Conclusions

- The worst case current imbalance in the present POE scheme creates only a marginal problem in terms of transformer inductance (OCL) and waveform Droop.
- The proposed 850 mA load current for POE Plus will have a significant effect on the interface transformers used in today's LAN interface.