Port To Port Cross-Regulation (PPCR)

For IEEE 802.3af Standard Power over MDI

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Problem Definition

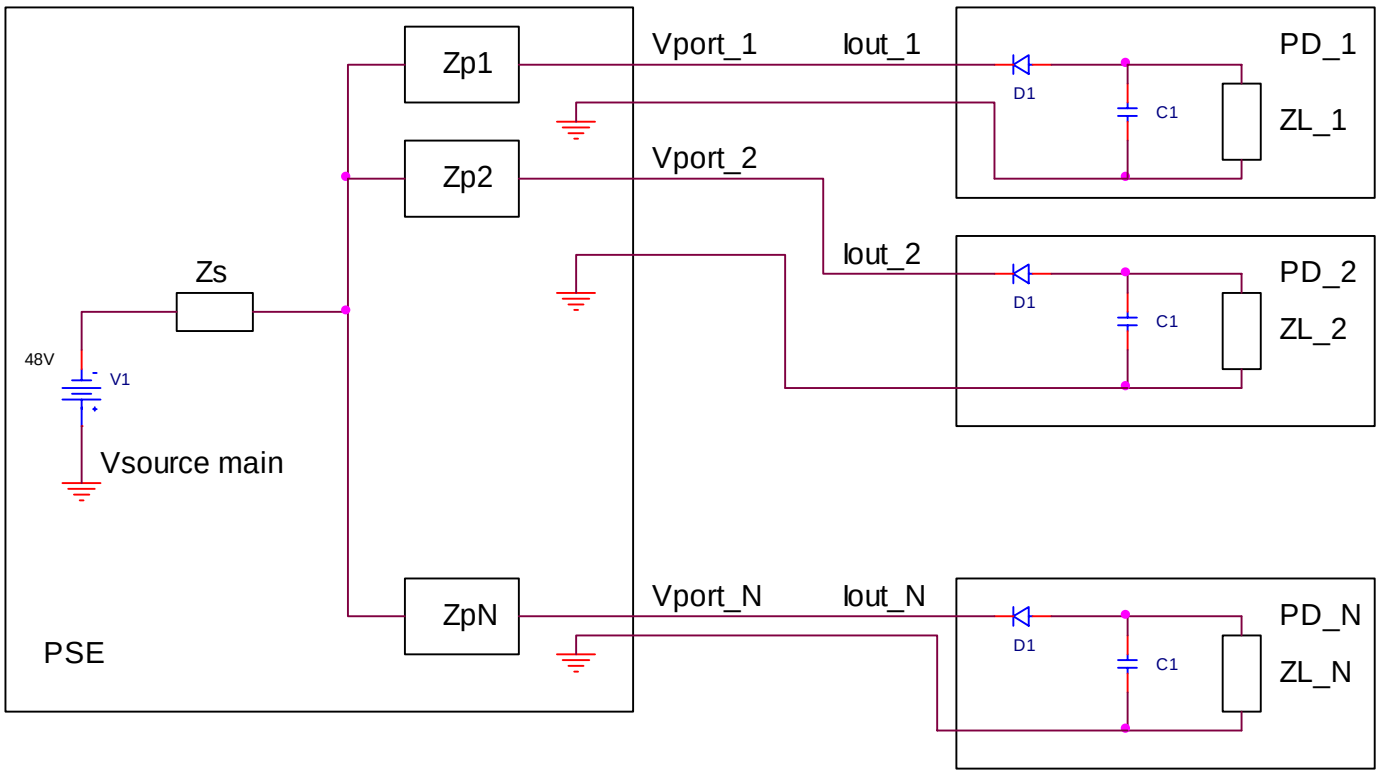
- Load changes at port N affects the output voltage of port M through a main power source used by all ports (Usually main power supply for all ports is used at Environment A).
- Voltage changes at port M will generate current transients at normal powering mode.
- Voltage changes at PSE port as function of changing power source from battery to primary power source or vice versa will generate the current transient as well and will not be discussed in this paper.
- The current transients can be higher than the normal operating current or below the normal operating current.
- At low load condition the current can go down to zero and stay there for long time depending on PD load condition, PD input capacitor and PSE output dV/dT value.

- The following parameters have to be defined:
  - Port to Port Cross-Regulation at the worst case conditions.
  - PSE output regulation

Note: The worst case is when in a multi-port system with N ports is loaded as follows:
N-1 ports are loaded with dynamic load that simultaneously changes from min to max.
The last port is loaded with constant minimum load. (~10mA)
The main PSE power supply output voltage is changed due to its finite output impedance and affects the current through the port loaded with the minimum load.

Figure 1: Cross Regulation in multi-port system.

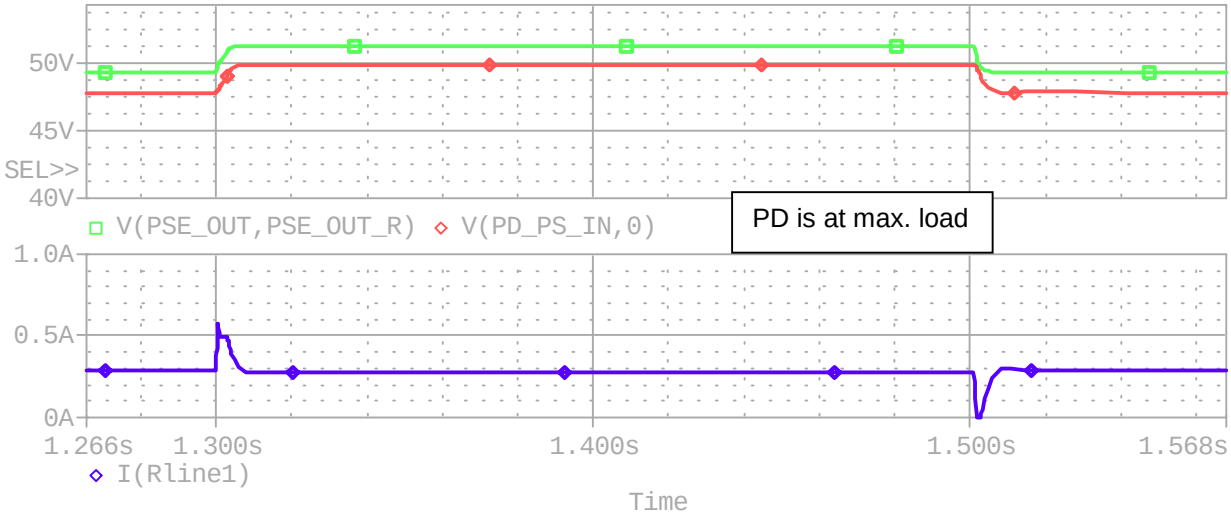
Load changes at any port affect the output voltage of other port. In any PD, C1 is charged to its steady state value, a positive change in PSE port voltage will generate a peak current of I=CdV/dT. A negative change in PSE port voltage will reverse bias D1 and the current will drop to zero and stay there until C1 voltage will discharged by its load to the steady state voltage of the port.



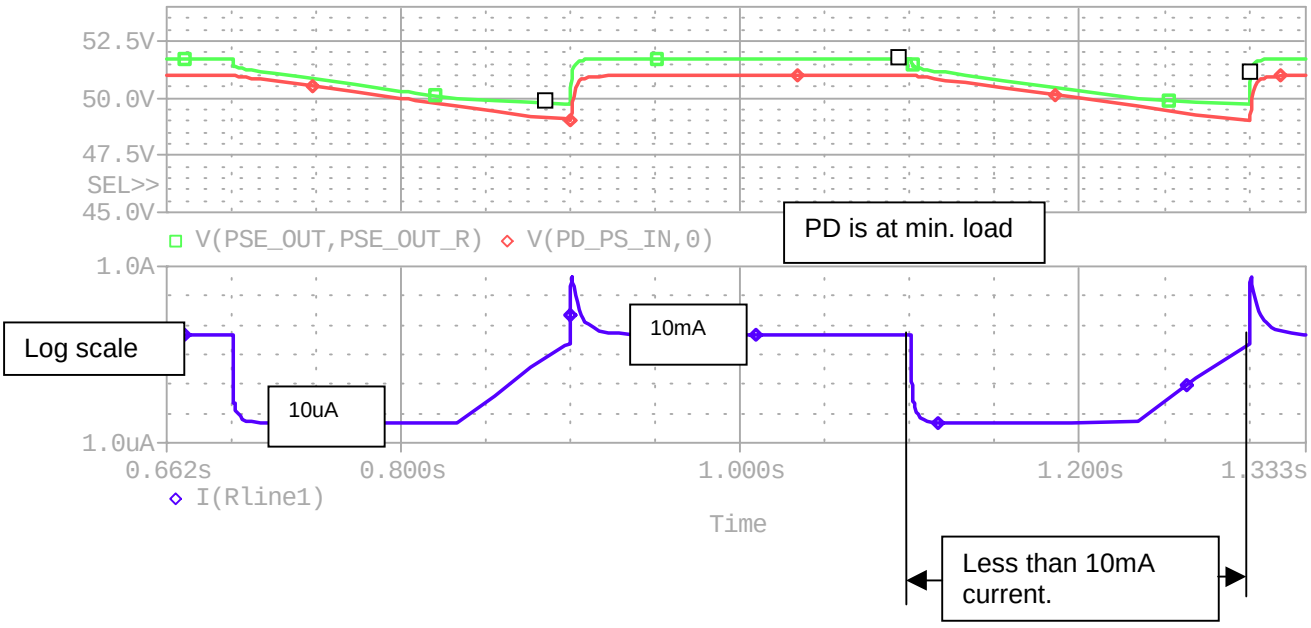
System Parameters affected by Port to Port Cross-Regulation.

- Max peak current and its duration during normal powering mode.
- Zero current duration allowed without disconnecting the port.

Figure 2 – PSE voltage changes affect PD input current transient behavior.



- Trace 1: PSE output voltage and PD input voltage as a result of PSE output changes
- Trace 2: PD Input current transients. Current drops to zero!
- PD is at max load, PSE current is limited to 0.5A max.



- Trace 1: PSE output voltage and PD input voltage as a result of PSE output changes
- Trace 2: PD Input current transients. Current drops to zero!
- PD is at min load (0.5W, Cpd=500Uf), PSE current is limited to 0.5A max.

Equations Derivation

Two cases should be considered.
1. Negative voltage change
2. Positive voltage change

1. Negative voltage change.

PSE voltage has drop from Vs1 to Vs2, Vs2<Vs1.
In this case the current through the cable will drop to zero for a time duration determined by Eq-1.

$$Td \le \frac{0.5 \cdot Cpd \cdot (VL1^2 - VL2^2)}{Ppd} \qquad \text{Eq-1}$$

VL1 and VL2 can derived from Eq-2 and Eq-3.
Eq-2 and 3 assume that:
PD load can be modeled as constant power load (switching regulator)
The diode voltage drop at the PD is negligible compared to the PSE source voltage.
Our goal is to define low frequency behavior (at the msec range) thus Cable is modeled as only resistance.

$$VL1 = \frac{Vs1 + (Vs1^2 - 4 \cdot Ppd \cdot Rline)^{0.5}}{2} \qquad \text{Eq-2}$$

$$VL2 = \frac{Vs2 + (Vs2^2 - 4 \cdot Ppd \cdot Rline)^{0.5}}{2} \qquad \text{Eq-3}$$

(See detailed derivation of Eq-2 and Eq-3 at “Considerations in selecting feeding voltage/current” May 2000 presentation)

Worst case condition would be when cable length is zero, hence VL1=Vs1, VL2=Vs2

Cpd = PD input cap during normal powering mode.
Ppd = PD input power consumption
Vs1 = Initial PSE output voltage
Vs2 = New PSE output voltage
VL1 = PD input voltage for PSE output voltage = Vs1
VL2 = PD input voltage for PSE output voltage = Vs2
Rline = Cable resistance

Example-1:

For the following numbers:

Cpd=500
Ppd=0.5W (min load current ~ 10mA)
VS1=50.5V
VS2=48.5V
Rline= 20?

From Eq-2 and Eq-3: (at 100m cable length)

VL1=50.3V
VL2=48.29V

From Eq-1:

Td=98.9mSec.

Conclusions:

Under the above numbers, the current will drop to zero for approximately 100mS.

Now, PSE output port parameters may be define as follows:

- The PSE output variations should be specified to –2V max.
  Include the following:
  - single port load regulation
  - port to port cross regulation
  - all ports are changed from min load to max. load (worst case) and their effect on a single port loaded with constant low load (0.5W)

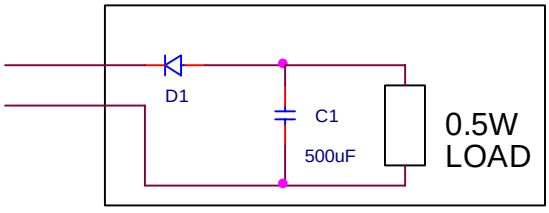
- The PSE will disconnect the port if the current is below 10mA for time duration greater than 100ms.

- Taking 6db safety margin: We can change the load regulation to –1V max. or increase the time to 200ms.

  It means that the PSE will not disconnect the port if as a result of –2V drop at PSE output voltage the current is below 10mA for time duration below 200ms.(same 6db margin)

The above behavior will be tested with a PD having 0.5W load and 500uF input capacitor (See figure 3)
For a PD with higher than 500uF, Td will be much higher. To keep it below the above value, Ppd min should be increased according to the following rule: for each 500uF capacitance in the PD, a minimum load of 0.5W is required. e.g. for 1000uF the minimum load will be 1W)

Figure – 3: Load test setup for the negative part of load regulation



2. Positive voltage change.

PSE voltage is increased from Vs1 to Vs2, Vs2>Vs1.
In this case the current through the cable will increase and can be limited by the inrush current limiter in the PSE or in the PD. The peak current time duration is set by Eq-4.

$$Td \le \frac{Cpd \cdot (Vs2 - Vs1)}{\Delta Ip} \qquad \text{Eq-4.}$$

$\Delta Ip =$ max. peak current change allowed.

If Ip max for normal powering mode is 0.4A and the average current is 350mA max than $\Delta Ip = 50\text{mA}$

Using Eq-4 with the numbers used in Example-1 result with the following:

Td=20ms.

The above result can be translated as follows:

- The positive rate of change of the port output voltage will be 2V/20ms max = 0.1V/ms.

Note:
Important conclusion from the above analysis is that the PD input capacitor value must be limited to a specific max value in order to ensure PSE-PD inter-operate. Otherwise, max. value for positive voltage transient's cant be defined.

Other alternative is to leave this as an implementation issue by setting a requirement that PSE vendor will specify the max. PD capacitor that is supported by his PSE. Under this definition, the PSE will ensure that with the max. capacitance supported by his PSE, the PSE will maintain 44V to 57V during PSE voltage transient events(as specified above as the worst case) and will not shut down the port.The controlling parameter on the transient current peak would be the dV/dT value, which is set by PSE vendor.

Lab results

Lab results have shown the following:

Test # 1 Results
Test # 1 check the load regulation results of real system.
Load changes from 200Watts to 5Watts and from 5Watts to 200Watts changes PSE main power supply by 200mVp max. and settling time to steady state was 20mS max.

Test # 2 Results

Test # 2 check the peak to peak voltage changes at low frequency of 0.5hz , duty 50% required to generate negative current transients with time duration of 100ms at the .
The max drop voltage allowed generating zero current for 100ms max. was 1.5V. (See figure 4.)

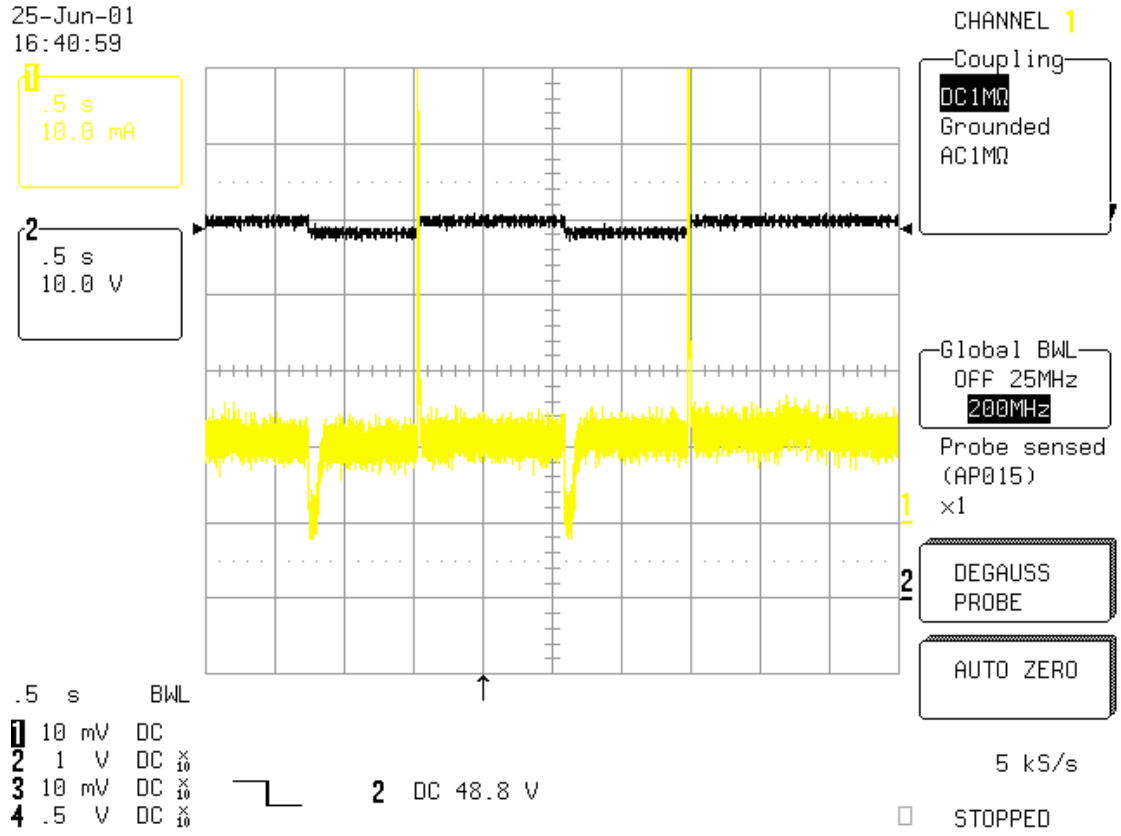
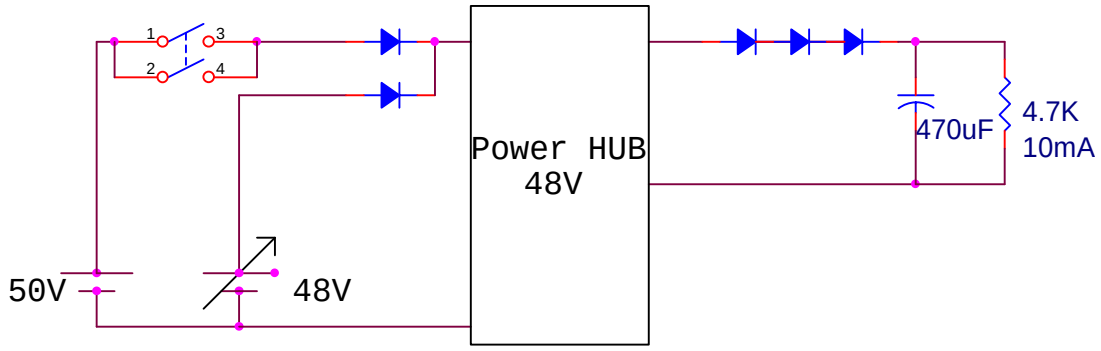


Figure 4:
Upper trace: PSE output voltage changes
Lower trace: PSE output current.

Test # 2 setup:



Summary.

1. Actual results in a real system shows that for a 200W total load change, the effect on a single port would be 200mVp max.
2. The voltage drop in a real PSE port required to reverse bias the PD input diode and cause zero current for a time duration of 100ms is 1.5V. (when min load of 0.5W in parallel to 500uF is connected to the port)
3. In order to limit the transient current to +50mA max. the rate of change in the PSE output voltage should be limited to 0.1V/ms. Higher rates is possible pending on the PSE ability to stay in current limit mode and sustain PSE voltage between 44V – 57V.
4. PSE vendor should specify the max. load capacitance supported by each port or PD input cap max value must be limited.

Combining all the above information generate the following PSE requirements:

Option 1:

1-1 PSE output port line/load regulation : +/- 1V max. settling time to steady state < 50ms.
1-2 PSE output port to port cross regulation : +/- 1V max. settling time to steady state < 50ms.
1-3 PSE will disconnect the port if the current is below 10mA from time duration > 100ms.

Option 2:

2-1 PSE output port line/load regulation : +/- 2V max. settling time to steady state < 50ms.
2-2 PSE output port to port cross regulation : +/- 2V max. settling time to steady state < 50ms.
2-3 PSE will disconnect the port if the current is below 10mA from time duration > 200ms.

Both for options 1,2.

3. PSE vendor should specify the max. load capacitance supported by each port **or** PD input cap max value must be limited.
   If PD input cap max value will be limited, than PSE output voltage rate of change should be limited to 0.1V/ms.

- For both options min load setup is defined according to figure-3.

4. PD min load is represented by load of 0.5W in parallel to 500uF fed through series diode. Higher caps than 500uF requires higher load. The new min load will be calculated to ensure that each 500uF will have 0.5W load in parallel. 1000uF need 1W as min. load etc. It is required according to Eq-1 to keep Td within the same time duration limits.
   Final wording of (4) is pending on final decision of (3).