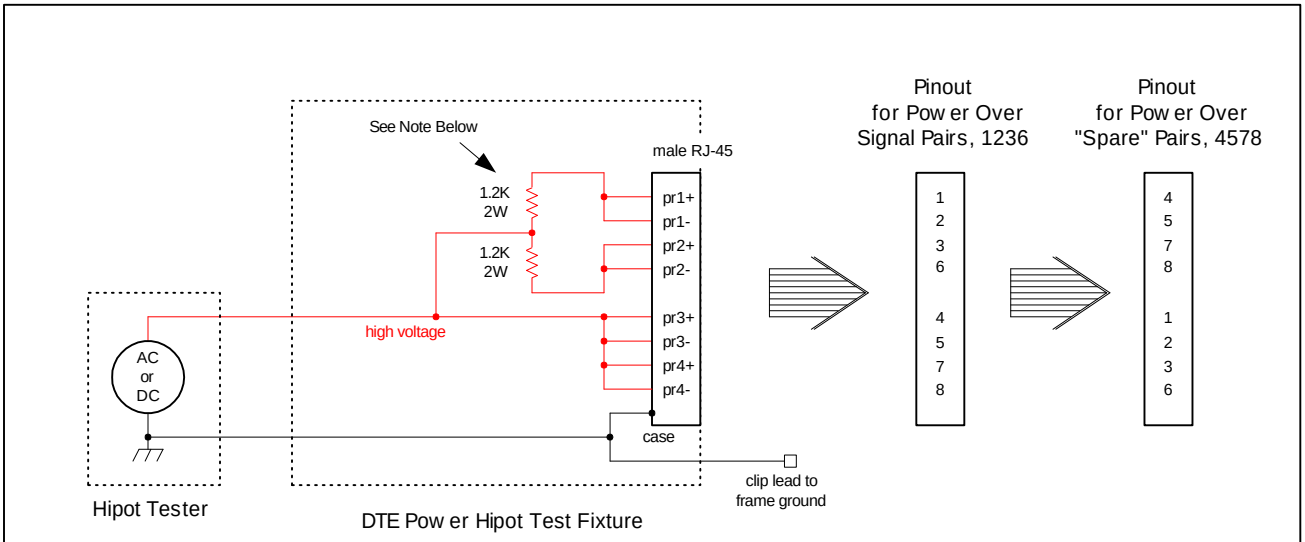
Hipot Testing for DTE Power.

Normal Hipot testing is done with the "unit under test" powered off. This setup is normally valid since the topology of what is being tested does not fundamentally change when power is applied. For example, a transformer's isolation does not change when data is sent through it.
However, in the case of DTE power, it is possible for the port topology to change from the point of view of common mode leakage current (current to frame ground) when the power is on. For example, if the DTE power supply has a leakage path that only presents itself with the power on, then doing Hipot testing with the power off will not find this problem.

So, I personally think that it would be in the spirit of the Hipot requirement to test both with DTE power off as well as on.
I believe that by doing so, we will improve the safety of our systems.

Below is one possible test setup to accomplish this test.
As always, Hipot testing typically uses 1500VAC, 50/60Hz for 1 minute, or +/- 2250 VDC for 1 minute. Immediately after this one minute period of time, the leakage current is measured at a lower voltage, say at 500 VDC.
For this test, the DTE power port under test must be either forced to be energized, or established using the discovery process, then switched over to the Hipot test mode.

Here is an example Hipot test setup, based on a conversation with Roger Karam:



Note:
The resistor values are set so that the series resistance of the tw o provides the minimum load for the PSE pow er supply. The resistor w attage rating is chosen to handle the maximum continuous fault current from the Hipot Tester, as w ell as the DC current from the DTE pow er supply

Hipot Test Setup
for PSE port with DTE Power Applied
(requires the ability to force DTE power on)