Implementation Study of Gigabit Copper Ethernet Receivers

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Motivation

- Three Competing Proposals for Gigabit LAN modem
  - ✓ 25 QAM
  - ✓ 12 CAP
  - ✓ PAM (5 level)

- Question
  - ✓ Are these proposals implementable and/or cost effective with the current (or 2 years later) technology?
Five Criteria for 1000BASE-T

- Broad Market Potential
- Compatibility with IEEE 802.3
- Distinct Identity
- Technical Feasibility
  - Demonstrated feasibility
  - Proven Technology
  - Confidence in reliability
- Economic Feasibility
  - Cost factors known, reliable data
  - Reasonable cost for performance expected
  - Total installation costs
Scope of the study

- No transmitter
- Only receivers
  - ✔ Adaptive filters only
  - ✔ No matching filter
  - ✔ No frequency/phase recovery
  - ✔ No control/memory calculation
  - ✔ No Viterbi decoder
  - ✔ No timing recovery
- DFE/NEXT/EC use sign-shift operations
  - ✔ No multipliers
- FFE: multiplier needed
- Coeff. update requires only 1/4 hardware
- CAP/QAM complex
- PAM real operations

✔ Minimum Assessment
Assumptions (1)

- **FFE (Feed-forward Equalizer)**
  - Requires multiplier
  - 7x12 (CAP/QAM), 6x12 (PAM)
  - CAP uses T/3 FSE
  - CAP uses phase-splitting FFE (2x real taps)
  - QAM: complex operation
  - PAM: real operation
  - 12 bit coefficients

- **DFE/NEXT/EC**
  - Use symbols (+/-1, etc)
  - No need to use multiplier for efficient implementation (CAP)
  - 10 bit coefficients
  - QAM/PAM need 3x10 multiplier

<table>
<thead>
<tr>
<th>Accumulator size</th>
<th>DFE</th>
<th>FFE</th>
<th>NEXT</th>
<th>EC</th>
</tr>
</thead>
<tbody>
<tr>
<td>QAM/CAP</td>
<td>16</td>
<td>21</td>
<td>16</td>
<td>20</td>
</tr>
<tr>
<td>PAM</td>
<td>16</td>
<td>22</td>
<td>21</td>
<td>21</td>
</tr>
</tbody>
</table>
Assumptions (2)

- Gate estimate for small cell
  - 7x12 multiplier: 800 gates
  - 6x12 multiplier: 650 gates
  - 3x10 multiplier: 330 gates
  - Signshift: 6 gates
  - Full adder: 10 gates
  - Flip-flop: 8 gates
- All gate estimates are “conservative”
- CAP @ 83.3 MHz
- PAM @ 125 MHz
- QAM @ 125 MHz

<table>
<thead>
<tr>
<th>Cell Calculation</th>
<th>7x12 mult</th>
<th>6x12 mult</th>
<th>signshift</th>
<th>FA</th>
<th>Flip-flop</th>
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<tbody>
<tr>
<td></td>
<td>800</td>
<td>700</td>
<td>4</td>
<td>10</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>16bit acc</td>
<td>20bit acc</td>
<td>21bit acc</td>
<td>22bit acc</td>
<td>3x10 mult</td>
</tr>
<tr>
<td></td>
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<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>330</td>
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<tr>
<td>Gate Estimate / TAP</td>
<td>CAP</td>
<td>PAM</td>
<td>QAM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DFE</td>
<td>328</td>
<td>618</td>
<td>618</td>
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<td></td>
</tr>
<tr>
<td>FFE</td>
<td>1178</td>
<td>1096</td>
<td>1178</td>
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<tr>
<td>NEXT</td>
<td>328</td>
<td>708</td>
<td>690</td>
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<tr>
<td>EC</td>
<td>400</td>
<td>708</td>
<td>690</td>
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</table>

<table>
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<tr>
<th>#TAPs</th>
<th>DFE</th>
<th>FFE</th>
<th>NEXT</th>
<th>EC</th>
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</thead>
<tbody>
<tr>
<td>CAP</td>
<td>8</td>
<td>24</td>
<td>12</td>
<td>64</td>
</tr>
<tr>
<td>PAM</td>
<td>10</td>
<td>20</td>
<td>80</td>
<td>120</td>
</tr>
<tr>
<td>QAM</td>
<td>6</td>
<td>9</td>
<td>30</td>
<td>45</td>
</tr>
</tbody>
</table>
Formula

- **CAP/PAM/QAM**
  - ✅ 4 receivers
  - ✅ 25% overhead for updating

- **CAP**
  - ✅ 4 real taps for DFE/NEXT/EC
  - ✅ 2 real taps for FFE

- **QAM**
  - ✅ 2 real taps @ 2x speed
  - ✅ use 3x10 multiplier for 5 level

- **PAM**
  - ✅ 1 real tap for real operation
  - ✅ use 3x10 multipliers for 5 level

- **CAP**
  - $5 \times (4 \times \text{DFE} + 2 \times \text{FFE} + 12 \times \text{NEXT} + 4 \times \text{EC})$

- **QAM**
  - $20 \times (\text{DFE} + \text{FFE} + 3 \times \text{NEXT} + \text{EC})$

- **PAM**
  - $5 \times (\text{DFE} + \text{FFE} + 3 \times \text{NEXT} + \text{EC})$
# Gate Estimates

<table>
<thead>
<tr>
<th>Number of TAPs</th>
<th>#TAPs</th>
<th>DFE</th>
<th>FFE</th>
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**CAP** = 10 * (2 DFE + FFE + 6 NEXT + 2 EC)

**PAM** = 5 * (DFE + FFE + 3 NEXT + EC)

**QAM** = 20 * (DFE + FFE + 3 NEXT + EC)

<table>
<thead>
<tr>
<th>#gates</th>
<th># transistors</th>
<th>speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAP</td>
<td>1,083,360</td>
<td>4,333,440</td>
</tr>
<tr>
<td>PAM</td>
<td>1,414,900</td>
<td>5,659,600</td>
</tr>
<tr>
<td>QAM</td>
<td>2,149,200</td>
<td>8,596,800</td>
</tr>
<tr>
<td>QAM2</td>
<td>1,074,600</td>
<td>4,298,400</td>
</tr>
</tbody>
</table>

Example:

**CAP** = 10 *
(2 * 8 * 328
+ 24 * 1178
+ 6 * 12 * 328
+ 2 * 64 * 400 )

(*) **QAM2**: 2*real tap, but running @ 2x speed
Analysis

- Total receiver = 1.3 * adaptive filters ("aggressive")
- Pentium CPU= 4 mil. transistors(*)
- All proposed systems are larger than the Intel’s Pentium (or Sun’s UltraSparc)
- PAM is larger and consumes more power than CAP/QAM
- Not cost effective
  - Modem chip will be as expensive as a Pentium class chip
  - Power consumption
  - Issue on Criteria 5

(*) from Texas Instruments
So, what’s next?

- A New Proposal
  - ✓ 1 Gb LAN uses 4 UTP
  - ✓ Dual-Duplex Transceiver over 4 pairs
    - • 2 x 500 Mbps transmitter / 2 pairs
    - • 2 x 500 Mbps receiver / 2 pairs
  - ✓ Two NEXT cancellers (not three) needed
  - ✓ No Echo canceller required

![Diagram of CAT5 UTP (4 pairs)](image-url)
Dual Duplex System

- **A New System**
  - ✓ 500 Mbps for each pair
  - ✓ Use 64 QAM/CAP
  - ✓ Baud rate = 83.3 MHz
  - ✓ Sampling frequency = 250 MHz

- **Key Issues**
  - ✓ Implementation complexity
  - ✓ Performance margin for BER = $10^{-10}$
  - ✓ Data conversion precision
Implementation Complexity

- **Same Gate Calculation**
  - ✓ Filter uses 8x12 multiplier (950 gates) for FFE
  - ✓ Use 3x10 multiplier for DFE/NEXT
  - ✓ Tap numbers are same as QAM/CAP system
  - ✓ Two NEXT cancellers
  - ✓ No Echo Canceller

- **Complexity Comparison**
  - ✓ 32% of CAP
  - ✓ 24% of QAM
  - ✓ 18-25% of PAM

CAP = 10 * (2 DFE + FFE + 6 NEXT + 2 EC)
PAM = 5 * (DFE + FFE + 3 NEXT + EC)
QAM = 10 * (DFE + FFE + 3 NEXT + EC)
New/QAM = 5 * (DFE + FFE + 2 NEXT)
New/CAP = 5 * (2 DFE + FFE + 4 NEXT)

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<td>5,659,600</td>
<td>125 MHz</td>
</tr>
<tr>
<td>QAM</td>
<td>1,074,600</td>
<td>4,330,240</td>
<td>125 MHz</td>
</tr>
<tr>
<td>New/CAP</td>
<td>359,280</td>
<td>1,437,120</td>
<td>83.3 MHz</td>
</tr>
<tr>
<td>New/QAM</td>
<td>264,510</td>
<td>1,058,040</td>
<td>125 MHz</td>
</tr>
</tbody>
</table>
Other Key issues

- **Performance Margin**
  - ✔ Target BER = $10^{-10}$
  - ✔ Required SNR = 29.4 dB
  - ✔ Question
    - Is there enough performance margin?
    - We might have just enough margin due to less NEXT interference and no echo.

- **Data Conversion Issue**
  - ✔ ADC
    - Should run at 250 MHz
    - Required Precision: 7/8 bits?
    - 7 bit ADC@250MHz seems OK
  - ✔ New proposal needs 2 ADC’s (not four)

- **Lucent’s Initial simulation study**
  - Positive margin
  - 7 bit ADC @ 250 MHz
  - no DFE

Ongoing study in progress!
Conclusion

- The Existing Proposals are not cost effective
  - ✔ Do NOT meet criteria 4 and 5
- The new proposal is only 30% of the existing proposals in terms of gate numbers
  - ✔ Meets criteria 5 better than the existing proposals
- 7/8 bit 250 Msps ADC feasibility issue
- On-going study on unresolved issues by simulation with real data (not simulated data)