Update on QAM-Based 1000BASE-T Transceiver

Oscar Agazzi, Mehdi Hatamian, Henry Samueli

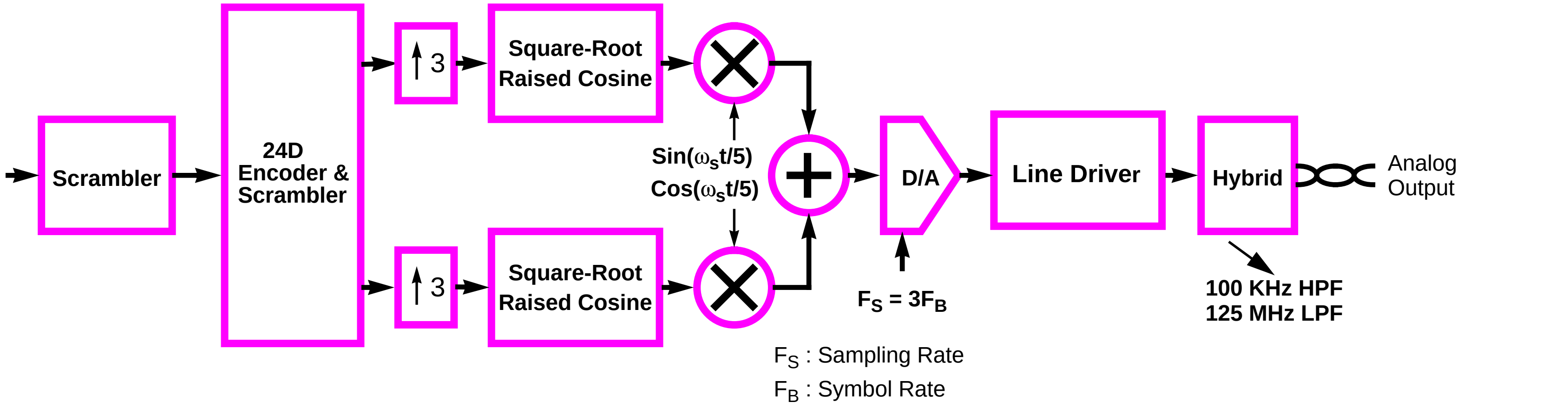
Broadcom Corp.

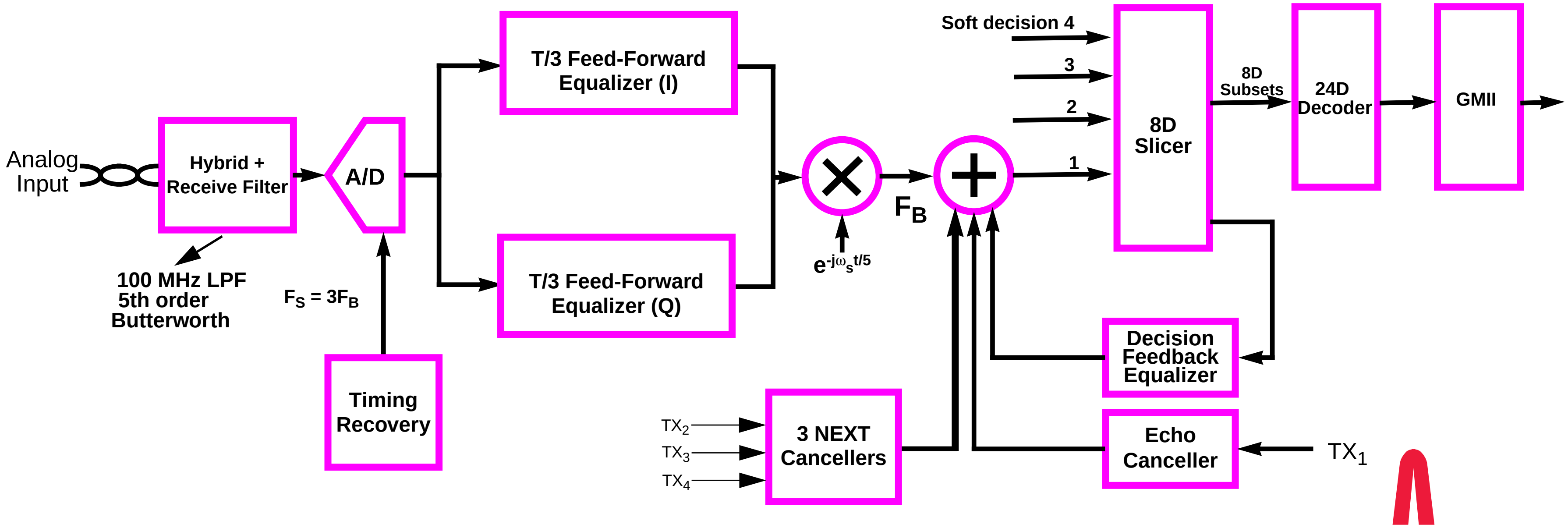
16251 Laguna Canyon Rd.
Irvine, CA 92618
714-450-8700

Overview

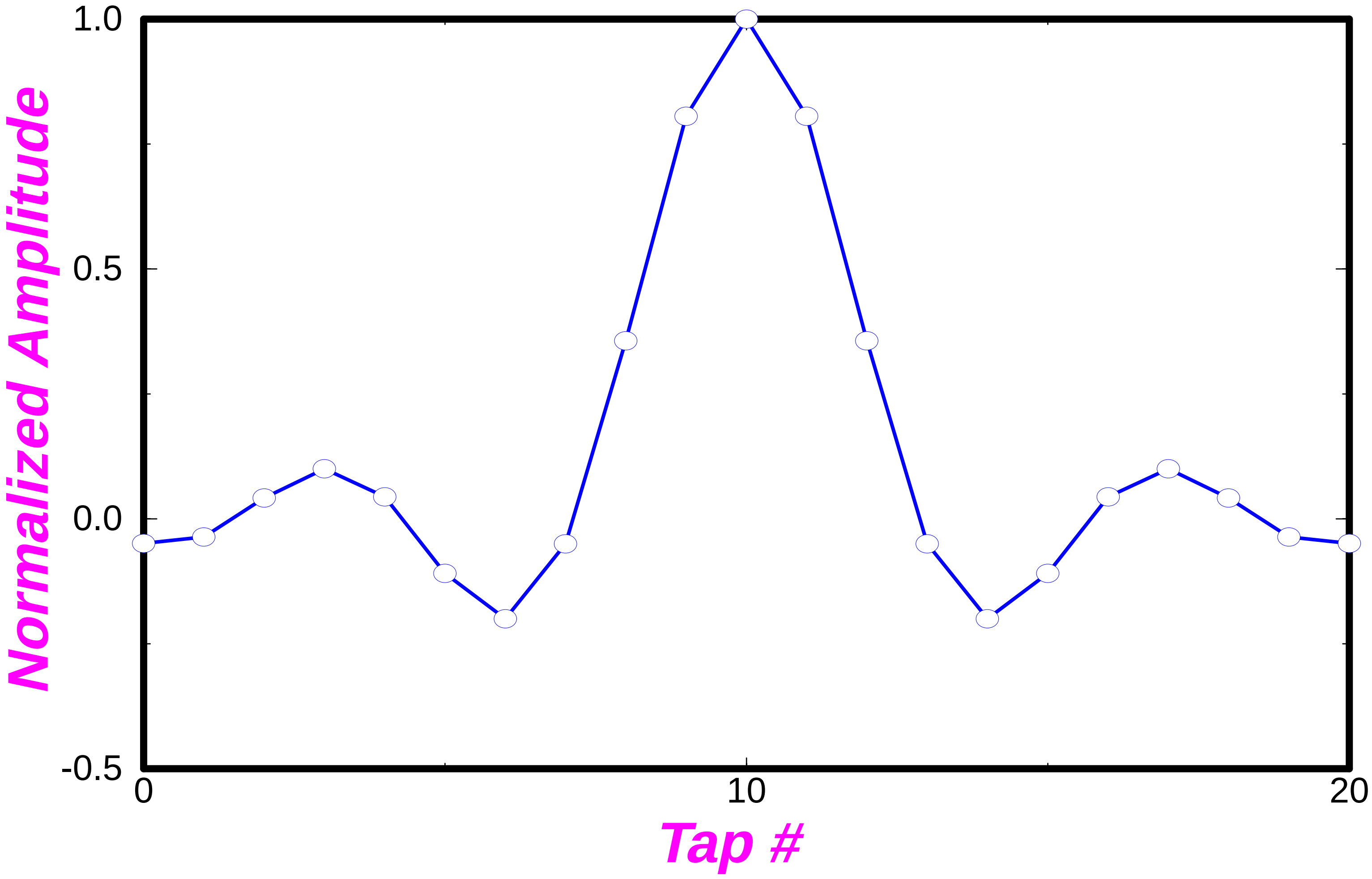
- Emissions
- Jitter performance
- TX compatibility
- Coding
- Latency budget
- GMII and clocking
- Start-up protocol
- PCS
- Conclusions

QAM Transceiver

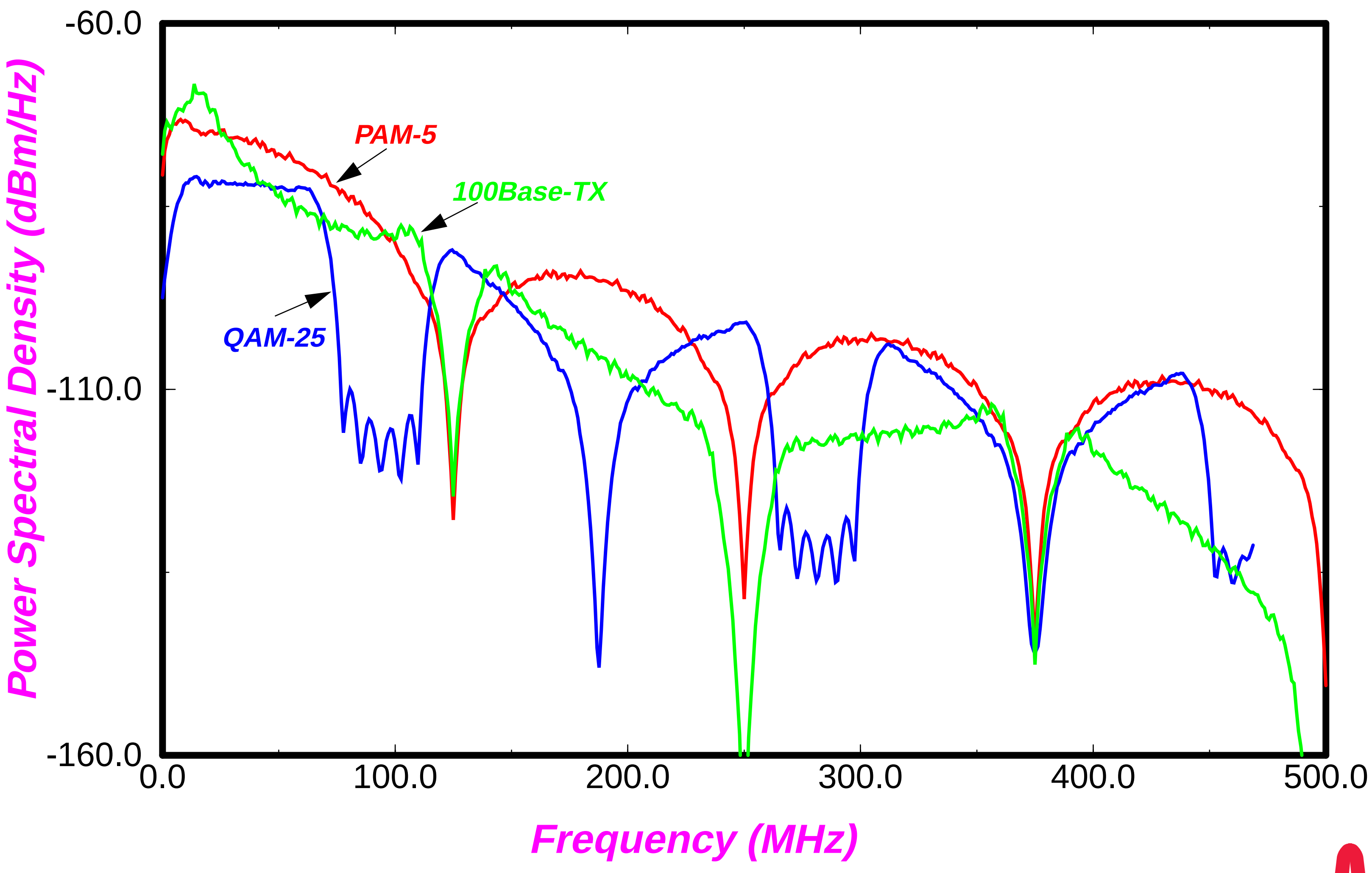




QAM-25 Transmit Filter Impulse Response



Emissions



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Jitter Behavior

- The jitter by the local oscillator will be attenuated by the PLL provided that the loop bandwidth is larger than the bandwidth of the jitter.

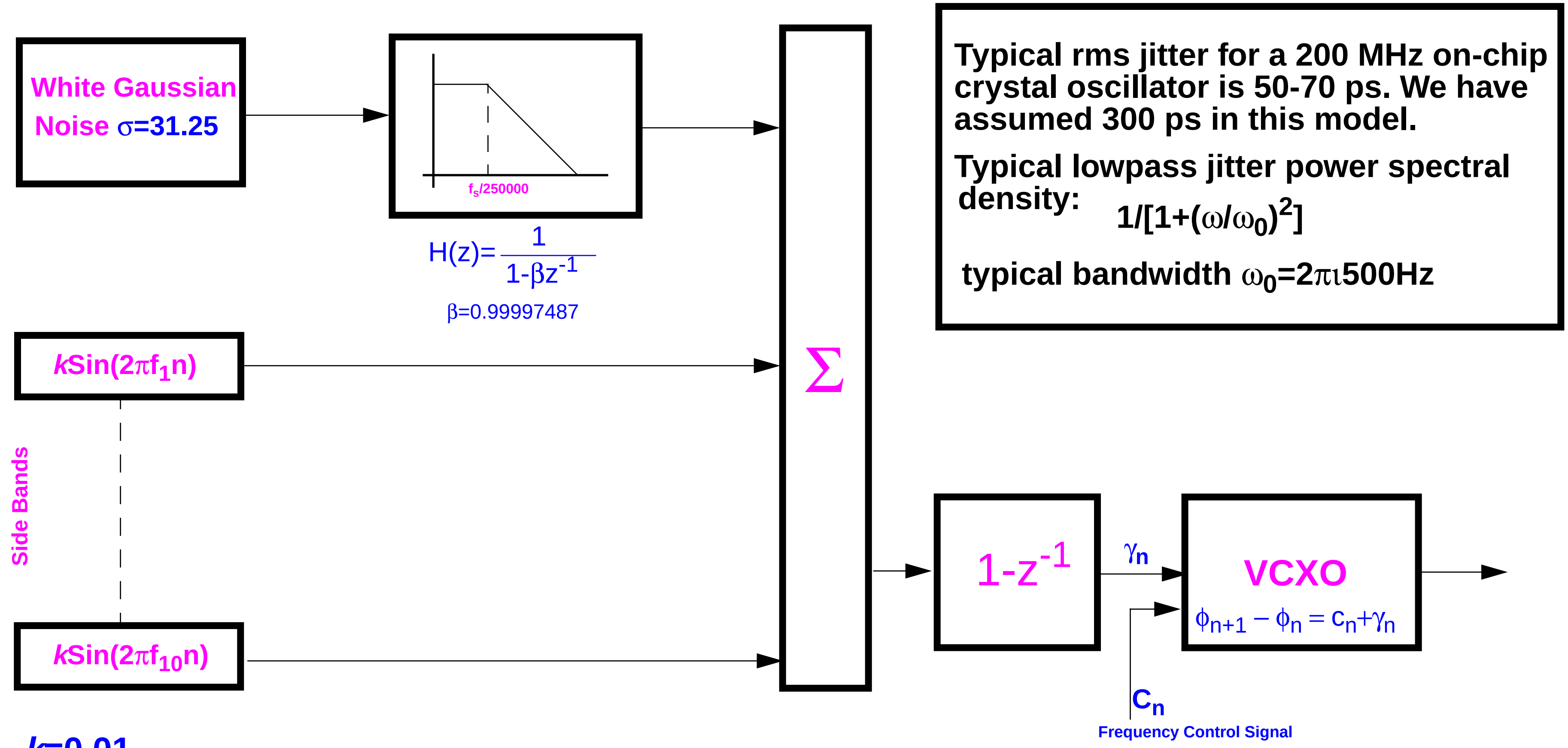
- Jitter in the received signal due to remote oscillator and remote timing recovery will be tracked if the bandwidth of the PLL is larger than the bandwidth of the jitter.

- Jitter due to local timing recovery can be reduced using a narrow band loop.

- Even relatively large values of rms jitter can have little effect on the receiver performance if the condition $B_{PLL} > B_{jitter}$ can be satisfied.

- The choice of PLL bandwidth is a tradeoff between data dependent jitter in recovered clock and intrinsic jitter filtering/tracking performance.

Proposed Jitter Model for VCXO



Typical rms jitter for a 200 MHz on-chip crystal oscillator is 50-70 ps. We have assumed 300 ps in this model.

Typical lowpass jitter power spectral density: $1/[1+(\omega/\omega_0)^2]$

typical bandwidth ω_0=2πι500Hz

***k*=0.01**

40dB down from carrier

f_1/f_s=8.133331e-5 f_2/f_s=1.704673e-4 f_3/f_s=2.278352e-4 f_4/f_s=3.371772e-4 f_5/f_s=4.222677e-4

f_6/f_s=5.111033e-4 f_7/f_s=6.213375e-4 f_8/f_s=7.411157e-4 f_9/f_s=9.227653e-4 f_{10}/f_s=1.087743e-4

From Low Pass Noise to Jitter Spectrum

Phase modulation for small phase is approximately amplitude modulation.
Low pass noise spectrum must be phase (not frequency) modulated to appear as sidebands of the oscillator’s nominal frequency

$$x(t)=A\mathrm{Cos}[\omega_s t+\Phi_m(t)]$$

If $\Phi_m(t)=\Phi_m \mathrm{Sin}\,\omega_m t$ and $\Phi_m<<1$ radian, then:

$$\begin{aligned} x_1(t) &= A\mathrm{Cos}\,\omega_s t\,\mathrm{Cos}(\Phi_m \mathrm{Sin}\,\omega_m t) - A\mathrm{Sin}\,\omega_s t\,\mathrm{Sin}(\Phi_m \mathrm{Sin}\,\omega_m t) \\ &\approx A\mathrm{Cos}\,\omega_s t - (A\mathrm{Sin}\,\omega_s t)(\Phi_m \mathrm{Sin}\,\omega_m t) \\ &= A\mathrm{Cos}\,\omega_s t + A\Phi_m/2\ [\mathrm{Cos}(\omega_s+\omega_m)t - \mathrm{Cos}(\omega_s-\omega_m)t] \end{aligned}$$

So, the sinusoidal jitter appears as sidebands at $\omega_s \pm \omega_m$

If $\Phi_m(t)$ is a stationary Gaussian random noise with lowpass power spectral density:

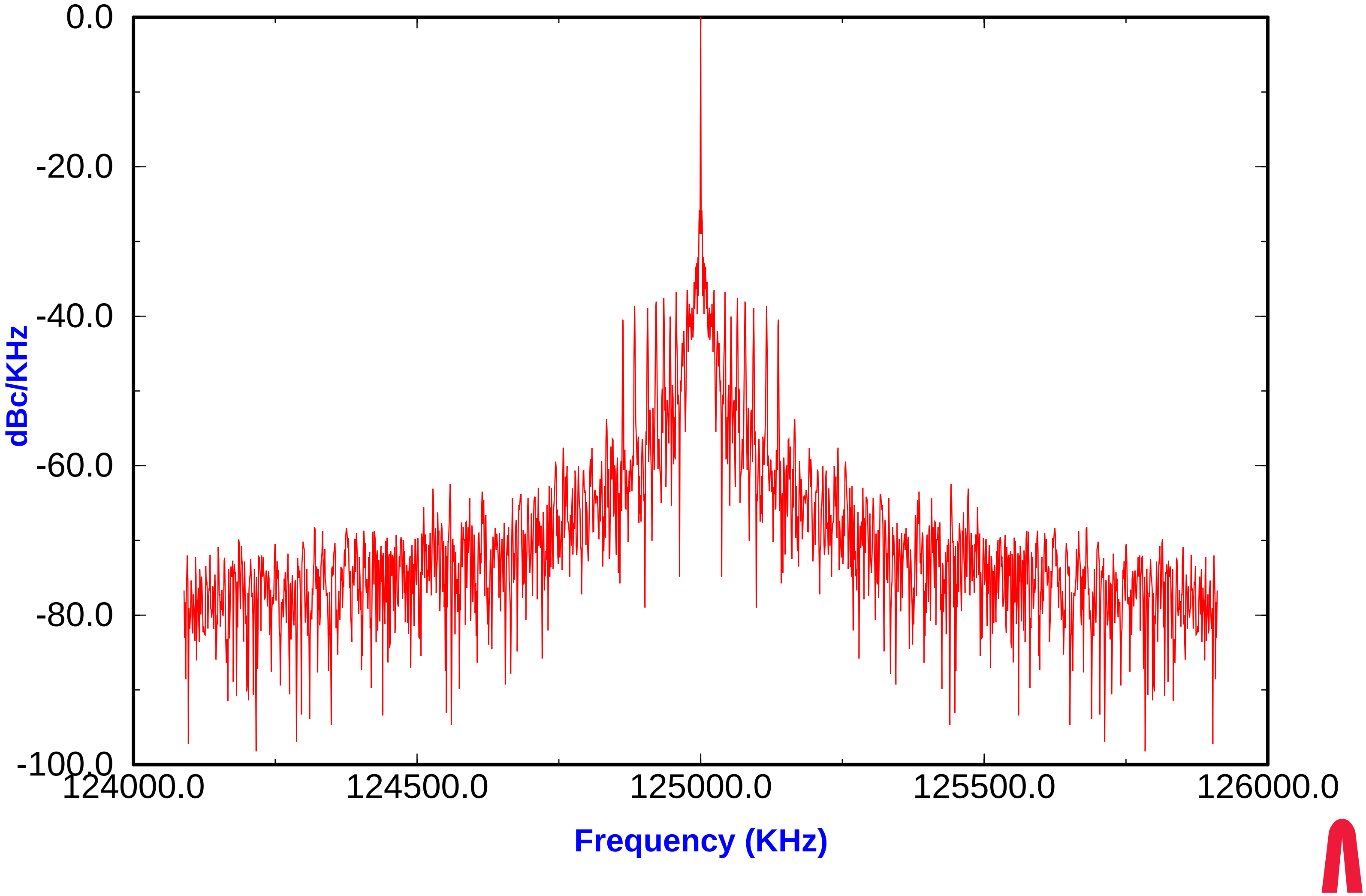
$$P_\phi(\omega)= 1/[1+(\omega/\omega_s)^2]$$

and $|\Phi_m| << 1$, then:

$$x_2(t) \approx A\mathrm{Cos}\,\omega_s t + A\Phi_m(t)\mathrm{Sin}\,\omega_s t$$

and the resulting spectrum exhibits noise skirts around the center frequency.

Jitter Model Plot



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Jitter Tolerance of QAM-25

- Since jitter distribution is Gaussian its peak (or peak to peak) value is infinite.
- For purposes of comparison, we define an equivalent “peak value” equal to 3σ (3 x rms value of jitter).
- Observed jitter tolerance of QAM-25 for 0dB margin:

3dB design point:	6ns p-p (37.5%T)
10dB design point:	10ns p-p (62.5%T)

Limits on Jitter in 1000Base-T Standard

- It is desirable to make the bandwidth of the timing recovery PLL very narrow in order to effectively filter the pattern dependent noise of the phase detector

- Suggested PLL bandwidth $BW_0 \sim 10^{-4}$ X Baud rate = 6.25 KHz (for QAM-25)

- This requires that all transceivers generate jitter with $BW < BW_0$ so that their jitter can be tracked . Otherwise, the minimum bandwidth that a designer can use would have to be determined by the worst transceiver in the market.

- The standard should limit the rms value and bandwidth of the jitter generated by any transceiver

Suggested values: rms < 0.5ns
BW < 5KHz

TX Compatibility

- Including a TX default mode in the QAM transceiver is a straightforward task.
- The PCS section of the TX is the only major block to be added.
- The entire PCS section of a TX transceiver requires less than 1600 gates to implement.
- The majority of these gates will be required by all 1000Base-T proposals. Besides, the added gate count itself is far below the accuracy of the estimated gate counts for all proposals.

QAM/TX Compatibility

- **Transmitter**
  - Add 4B5B encoder, scrambler and MLT-3 encoder.
  - Add a multiplexer at the input of the D/A to bypass QAM transmit section.
  - Less than 400 gates total.
- **Receiver**
  - The slicer for TX is only 6 gates and can be trivially embedded in the QAM slicer.
  - Add descrambler and 4B5B decoder.
  - Clock recovery circuit already generates Baud clock (62.5MHz) and the 125 MHz clock.
  - DFE already runs with the 125 MHz clock. A single control line puts its multiplexer in the TX mode.
  - FFE is used in T-mode instead of T/3. The 6-taps of I-channel are used which is plenty for the TX application. The Q-channel is turned off. The master 187.5 MHz clock is slowed down to 125 MHz.
  - Less than 1000 gates in total.

3dB and 10dB Design Points

Parameters	QAM-25, 3dB	QAM-25, 10dB
A/D resolution	6 @187.5MHz	7 @ 187.5MHz
D/A resolution	6 @187.5MHz	7 @187.5 MHz
Baud Rate	62.5 MHz	62.5 MHz
Analog TX Filter	SP@100MHz	SP@100MHz
Analog Receive Filter	BW5@93.75MHz	BW5@93.75MHz
Launch Level	2V P-P	2V P-P
Digital Transmit Filter (7 symbol span)	42 @62.5MHz	42@62.5MHz
Real FFE Taps	12 @ 187.5MHz	12 @187.5MHz
Real DFE Taps	6 @ 125MHz	6 @125 MHz
Real NEXT Taps	18 @ 125MHz	50 @ 125MHz
Real Echo Taps	50 @125MHz	120 @ 125MHz
Jitter Tolerance *	6ns (37.5% T)	10ns(62.5%T)
BLW Cancellation	NO	NO
Viterbi Decoder	NO	NO
Latency	34.5BT	34.5BT
Crane Test **	60mV P-P	65mV P-P
Actual Margin	3.25dB	10.15dB
Margin with FEXT	1.74dB	7.08dB
Margin with FEXT and FEXT Canceller	3.2dB	10.05dB
Estimated Gate Count	170K	348K
Additional Gate Count for TX	1.5K	1.5K
Estimated Power including analog	2.9W, 0.35µm CMOS 2.1W, 0.25µmCMOS	4.4W, 0.35µm CMOS 3.1W, 0.25mm CMOS

* Jitter tolerance is measured with closed loop timing recovery reflecting the actual operation of the recovery circuit.

** Crane test results were obtained with a transmit power that is 1/4 the transmit power of PAM-5 with 2V P-P launch level.

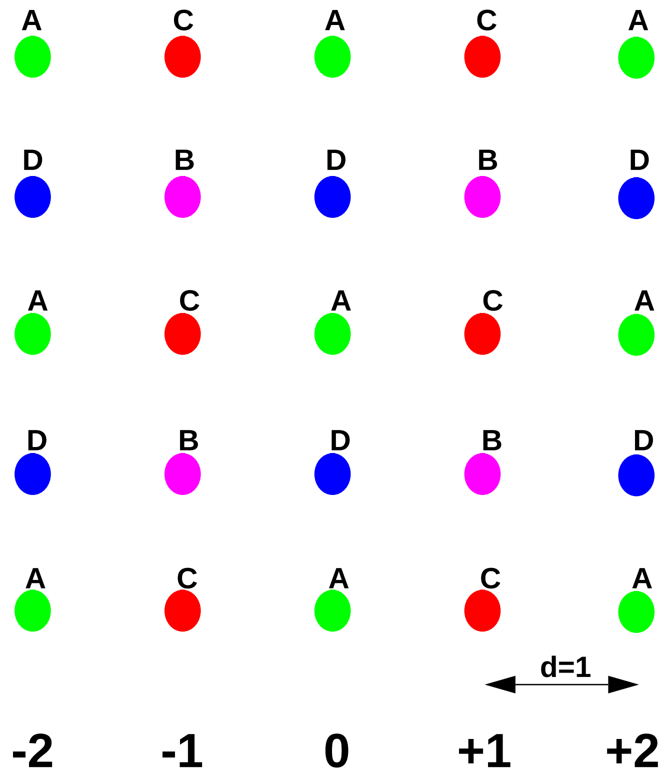
24D Coding for QAM-25

- **We use the 24D code proposed by Lee-Fang Wei from Lucent.**
- **At each baud period, the four 2D symbols on the 4 pairs can form an 8D constellation. Combining the symbols received in three baud periods (12 2D symbols) we can form a 24D constellation which has 5^{24} points.**
- **It is possible a select a subset of the 24D constellation which has 2^{48} points with the minimum squared Euclidean distance of 4 times the distance between the points in the original 2D constellation (6dB coding gain).**
- **The 2^{48} points in the above code represent 12 2D symbols where each symbol carries 4 bits of data (6 Bytes in total).**

2D Subsets

- The 25 point QAM constellation is partitioned into four 2D subsets A, B, C and D as shown here.

- The intra-subset minimum squared Euclidean distance is $4d^2$



4D Subsets

4D subsets are formed by concatenating the 2D subsets corresponding to adjacent wire pairs.

The intra-subset minimum squared Euclidean distance is still 4.

The total number of points in the 8 4D subsets is 8 x 64 = 2^9

Subset #	Elements	# of Points	Pruned to
0:	(A,A) U (B,B)	97	64
1:	(A,B) U (B,A)	72	64
2:	(C,C) U (D,D)	72	64
3:	(C,D) U (D,C)	72	64
4:	(A,C) U (B,D)	78	64
5:	(A,D) U (B,C)	78	64
6:	(C,A) U (D,B)	78	64
7:	(C,B) U (D,A)	78	64

8D Subsets

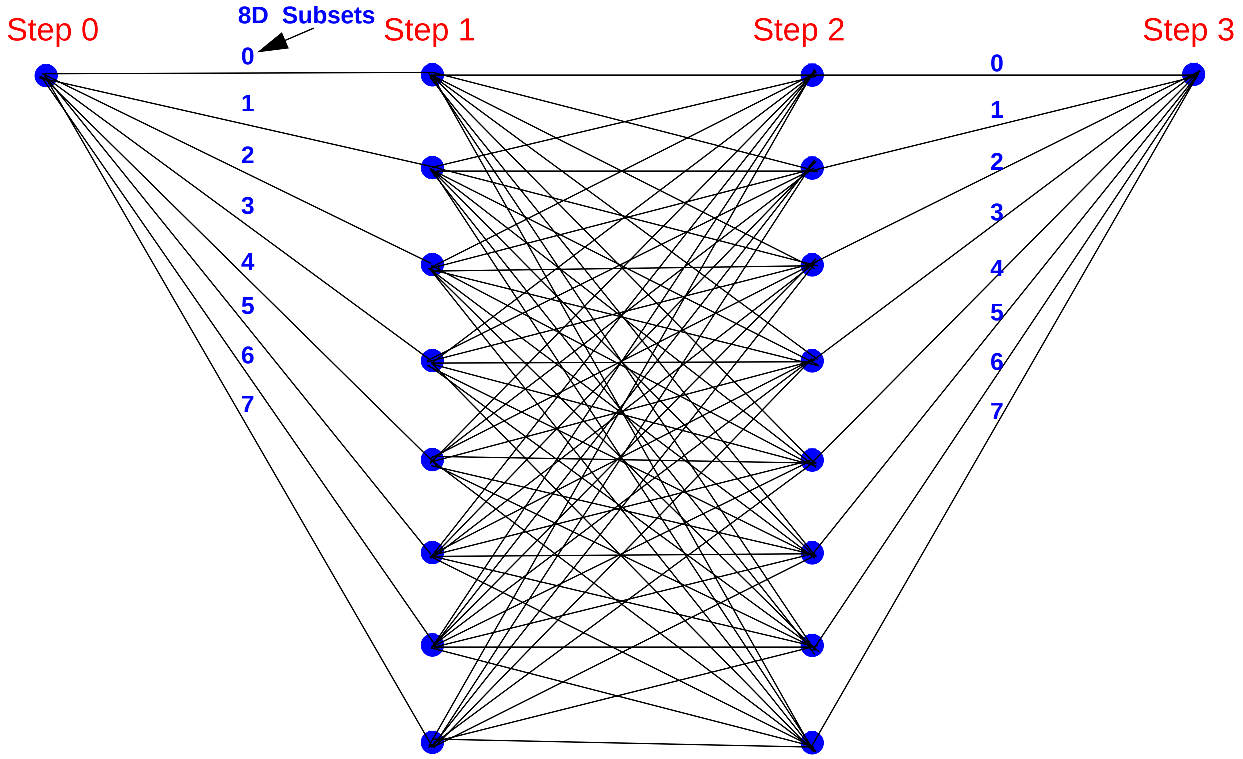
8D subsets are formed by concatenating the 4D subsets.
The intra-subset minimum squared Euclidean distance is still 4.
The total number of points in the 8 8D subsets is 8 x 2^{14} = 2^{17}

Subset #	Elements	# of Points
0:	(0,0) U (1,1) U (2,2) U (3,3)	2^{14}
1:	(0,1) U (1,0) U (2,3) U (3,2)	2^{14}
2:	(0,2) U (1,3) U (2,0) U (3,1)	2^{14}
3:	(0,3) U (1,2) U (2,1) U (3,0)	2^{14}
4:	(4,4) U (5,5) U (6,6) U (7,7)	2^{14}
5:	(4,5) U (5,4) U (6,7) U (7,6)	2^{14}
6:	(4,6) U (5,7) U (6,4) U (7,5)	2^{14}
7:	(4,7) U (5,6) U (6,5) U (7,4)	2^{14}

24D Code

Order of branches from 2nd to 3rd state:

0	1	2	3	4	5	6	7
1	0	3	2	5	4	7	6
2	3	0	1	6	7	4	5
3	2	1	0	7	6	5	4
4	5	6	7	0	1	2	3
5	4	7	6	1	0	3	2
6	7	4	5	2	3	0	1
7	6	5	4	3	2	1	0



24D Decoding Procedure

- **2D Slicing**
  - Slice the soft decisions in subsets A, B, C and D.
  - Compute error and distance for each subset.

- **4D Slicing**
  - Add distances for each one of the 2 pairs in each 4D subset and select the best pair in the subset. For example, referring to the table on page 16, for subset #4, add the distances for pair A & C, call it d1; also add the distances for B & D, call it d2; then pick the smallest of the two and the associated 4D symbol. This process produces 8 4D symbols and 8 distances associted with them.

24D Decoding Procedure (continued)

- **8D Slicing**
  - Add distances for each one of the 4 pairs in each 8D subset and select the best pair in the subset. For example, referring to the table on page 17, for subset #5, add the distances for 4D subsets 4&5, 5&4, 6&7 and 7&6, and pick the smallest of the 4 and the associated 8D symbol. This process produces 8 8D symbols and 8 distances associoted with them.

- **24D Slicing**
  - Referring to the diagram on page 18, at each one of the 8 nodes (states) at step 1, compute 8 distances as the sum of the distance of the 8D subset associated with the incoming branch and the 8 distances of the 8D subsets associated with the outgoing branches at that node.

24D Decoding Procedure (continued)

- At Step 3, select the smallest of the 8 distances of the 8D subsets associated with the incoming branches and the corresponding symbol. This provides the final decision.

Latency Budget

Transmitter

GMII Input Register	1
Synchronization	1
24D Encoder/Scrambler	4
Transmit Filter	7
DAC and Analog Transmit	1.5
	14.5 BT

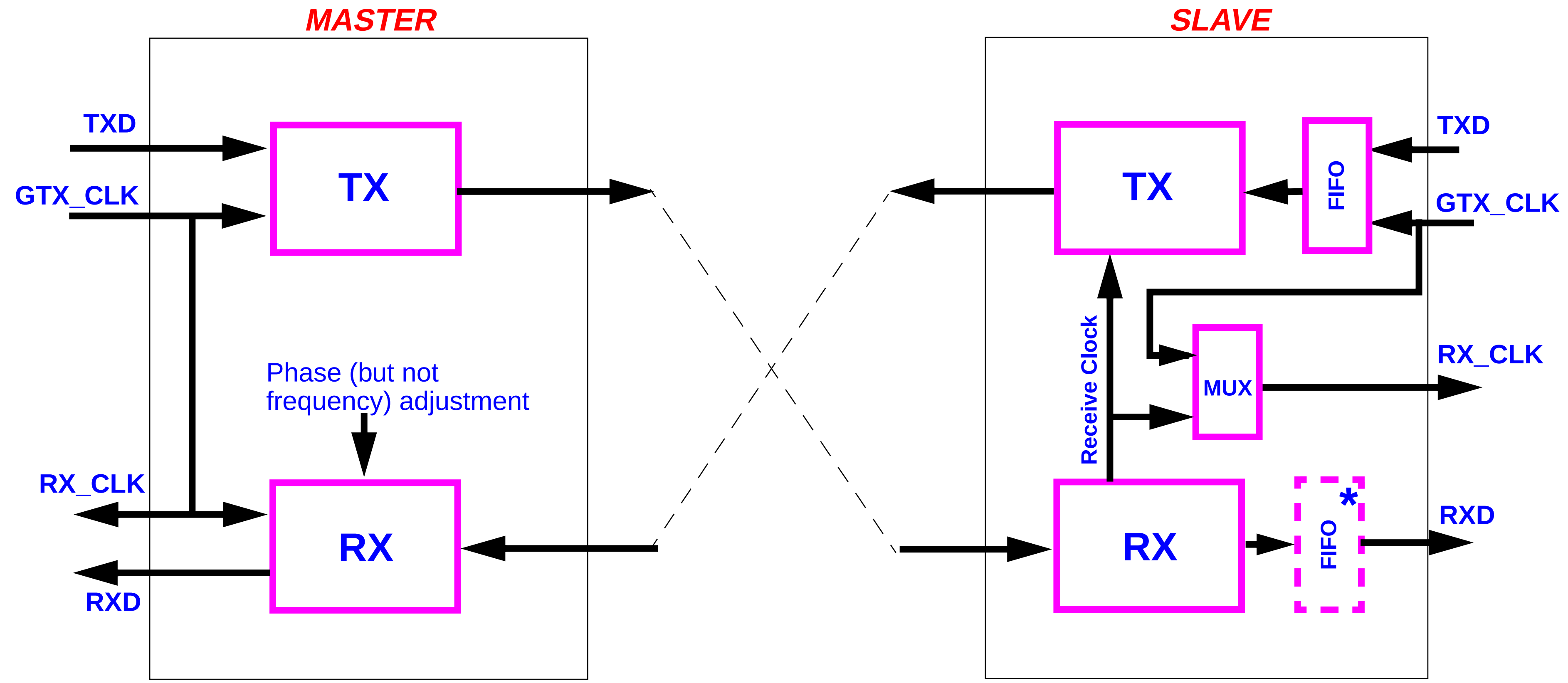
Receiver

Analog input to A/D output	3.5
FFE (including ± 20 ns pair skew compensation)	6 ± 2.5
24D Decoder/Descrambler	6
Resynchronization*	1
GMII Output Register	1
	<= 20 BT

Total PHY Latency = 34.5 BT

* Assuming RX_CLK = GTX_CLK

Clocking



* Needed only if RX_CLK = GTX_CLK

Start-up Protocol

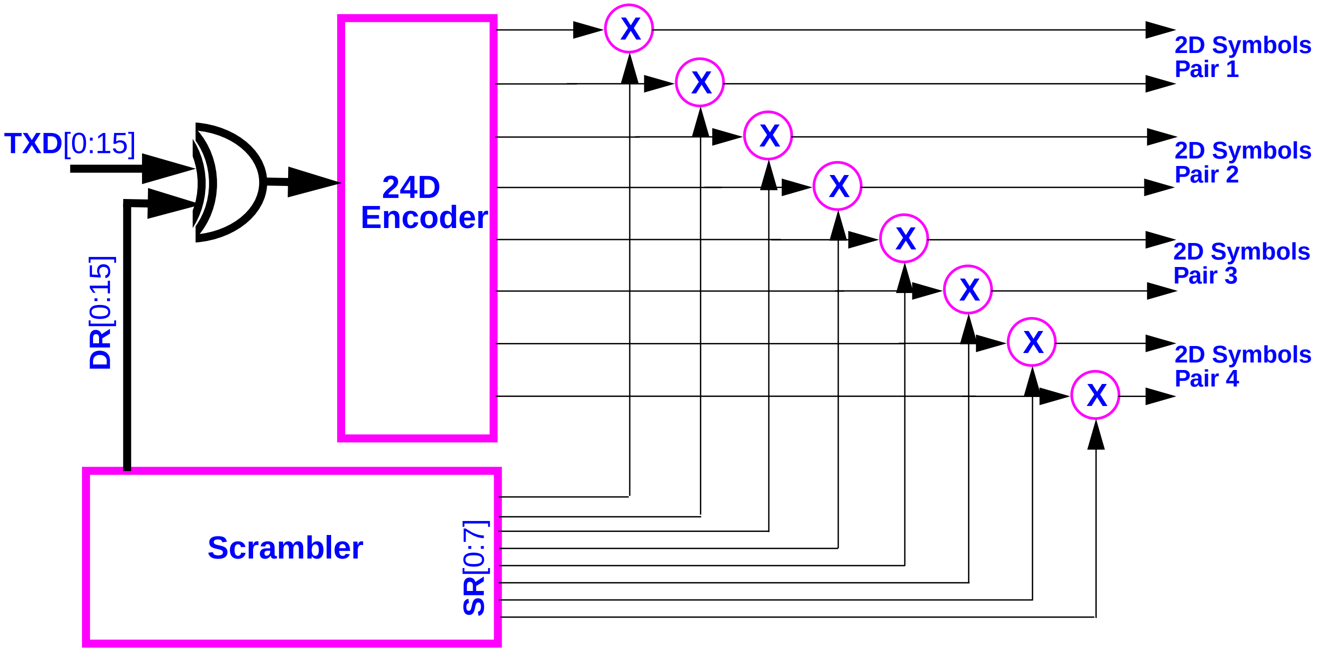
	MASTER	Direction of Signals	SLAVE
~ 1ms	Transmit	→	Receive in half-duplex Train equalizer Acquire timing synchronization
~ 1ms	Stop transmitter Train equalizer Adjust phase of receiver (frequency already known)	←	Start transmitting Freeze frequency and phase of timing recovery* Train echo and NEXT cancellers
~ 1ms	Restart transmitter Freeze phase adjustment Train echo & NEXT cancellers	→ ←	Unfreeze frequency and phase control
	Unfreeze phase control Initiate normal transmission	→ ←	Initiate normal transmission

***NOTE:** *If a second order (Proportional + Integrating) timing recovery loop is used, frequency error after initial acquisition will be very small, therefore the phase drift during this “open loop” period will be negligible. The phase will still be correct when timing recovery is unfrozen.*

PCS

- **Encoding and scrambling**
- **Pair skew compensation**
- **Acquisition of absolute carrier phase (eliminate nπ/2 ambiguity)**
  - This is the passband generalization of wire polarity acquisition in baseband systems
- **Acquisition of the descrambler state**
- **Idle pattern generation**
- **Encoding of SSD, ESD, error indication, link partner receiver status, etc.**

Scrambling



- An 8D generalization of the 2D scrambling method used in 100Base-T2.
- The scrambler is a classical linear feedback shift register.
- The scrambler generates the Data Randomization bits DR[0:15] and the Sign Randomization bits SR[0:7] by XOR combination of the bits of the shift register.

Training Sequence

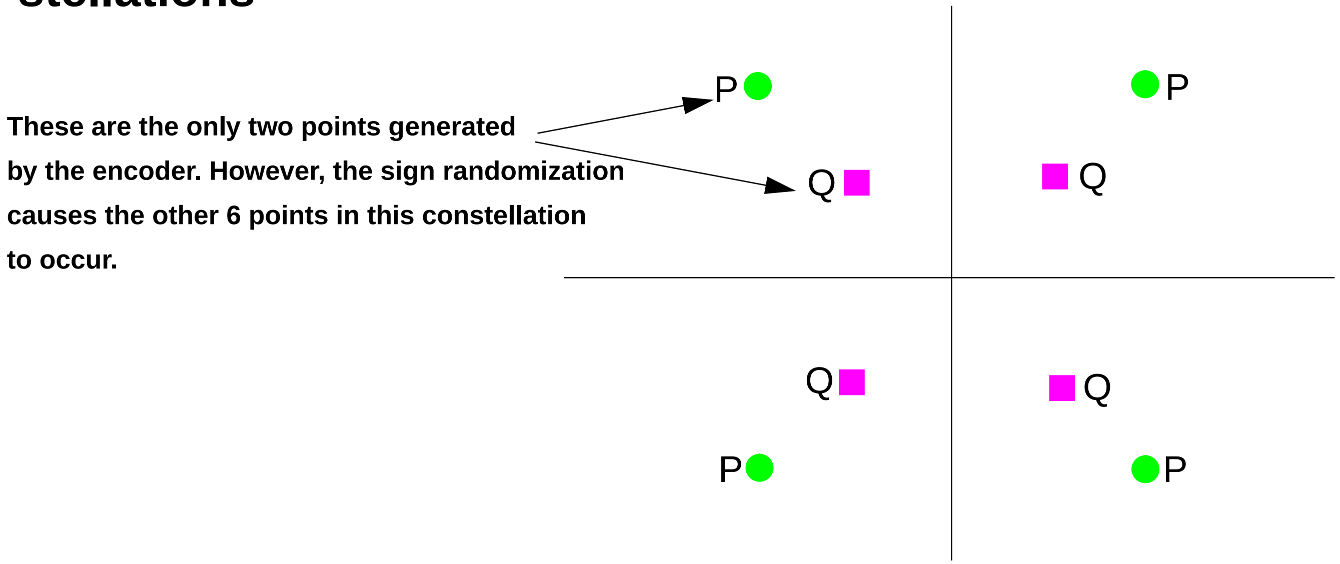
- **The following functions are performed using the equalizer training sequence:**
  - Skew compensation
  - Carrier phase acquisition
  - Acquisition of descrambler state

- **The training sequence is generated by sending the following pattern PPPQQQPPPQQQ....................PPPQQQ on all 4 pairs where P=(-2,-2) in 2D subset A, and Q=(-1,-1) in 2D subset B described before.**

- **During this sequence we perform sign randomization but not data randomization.**

Training Sequence (continued)

- The result is that the equalizer is trained using the following QPSK constellations



These are the only two points generated by the encoder. However, the sign randomization causes the other 6 points in this constellation to occur.

- Since the transitions from constellation P to constellation Q must occur simultaneously in the 4 receivers, this sequence forces the equalizer to train to a state where the skews are compensated. This is simply a case of the reduced constellation algorithm in blind equalization where the reduced constellation is such that the decisions have to be all Ps or all Qs across the 4 pairs.

Training Sequence (continued)

- Since only symbols p=(-2,-2) or Q=(-1,-1) are sent (but not their nπ/2 rotations), the descrambler state and absolute phase can be determined for the 4 pairs. Knowing the sign of both the transmitted and received (at the output of the decoder) P or Q symbols, the sign randomization bits can be recovered from which the state of the descrambler can be inferred.

Wire Pair Identification

- Wire pair identification can be achieved by sending a sequence such as:

Pair1	Pair2	Pair3	Pair4
P	Q	R	S
P	Q	R	S
P	Q	R	S
P	Q	R	S
⋮	⋮	⋮	⋮

where P=(-2,-2), Q=(-1,-1), R=(-1,0), S=(0,1) (other sequences are possible).

PCS (continued)

- The equalizer training sequence (which also achieves skew compensation, carrier phase acquisition, and descrambler state acquisition) and the pair identification sequence are part of the start-up protocol described before.
- The idle pattern is the same as in 100Base-T2 (subset (3,3) of 8D subset #0).
- Since the 4D subsets need only 64 points, but have between 72 and 97 points, which are not used for normal data transmission, there is a vast supply of special characters.
- Some of these special characters can be chosen as SSD, ESD, error indicators, link partner receiver status indicators, etc.
- It is important to observe that these special characters are members of the 8D subsets and there is no constraint on their position in the 24D code word. Therefore, there are no constraints on the length of the packet.

QAM-25 Summary

- Low emissions.
- Latency well within allowed budget.
- 6dB coding gain using simple and robust 24D coding scheme without error propagation problems.
- Very reasonable complexity. Even in today's 0.35 micron CMOS technologies, a single 4-channel 1000Base-T transceiver will be pad-limited!!
- Very robust performance in the presence of jitter.
- Transceiver architecture defaults to 100Base-TX with extremely minimal additional complexity (less than 1500 gates).
- Conceptually simple and well-defined PCS and start-up protocol.
- PCS exploits very elegantly the properties of the 8D sub-constellations to achieve blind equalization, pair skew compensation, wire pair identification, scrambler state recovery, etc.
- All aspects of timing recovery (an important factor in the performance of any transceiver) are included in our simulations in a closed loop system reflecting reality.