1394 Overview

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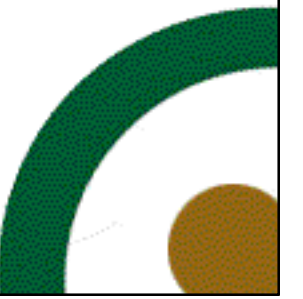
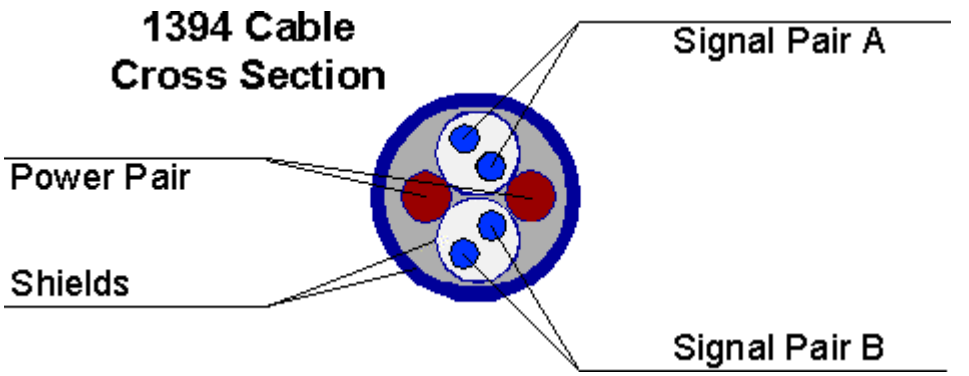
1394 Objectives

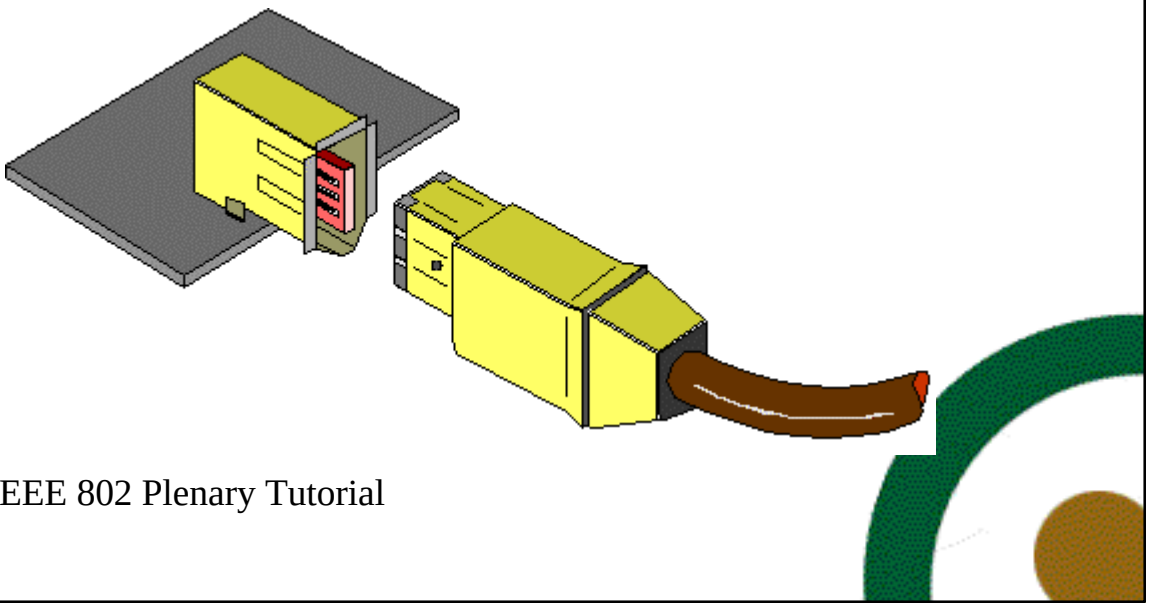
- Digital Interface
- Physically Small
- Easy to Use
- Hot Pluggable
- Inexpensive
- Scalable Architecture
- Flexible Topology
- Fast
- Open Standard



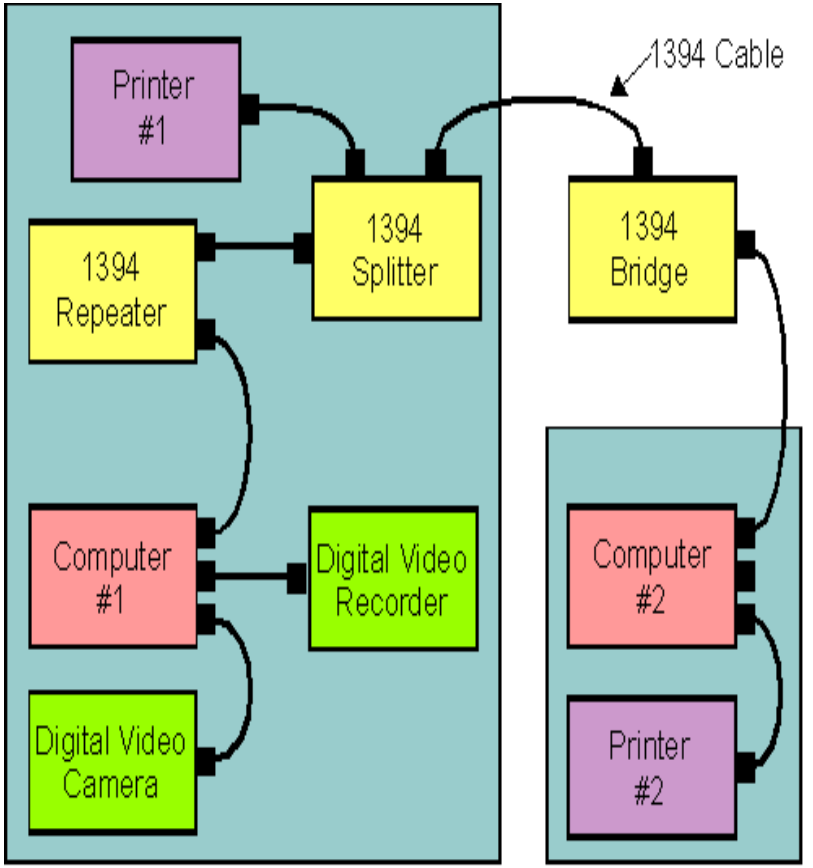
Original 1394 Cable

- Two Pairs of 28 AWG Shielded Twisted Pair (STP) Signal Wires
- Two 22 AWG Power Wires
- Outer Shield
- 4.5 meter Maximum Link Length
- 6-pin Nintendo-like Connector





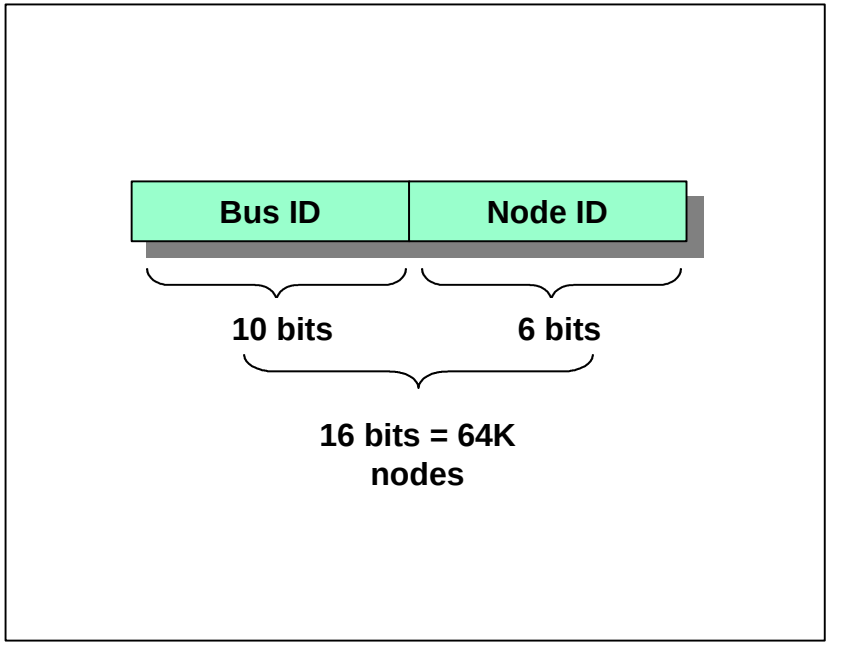
1394 Topology



- Contains Up to 64 Nodes per Bus
- Bridges Link the Buses Together
- Bus Can Fork into a Tree Structure

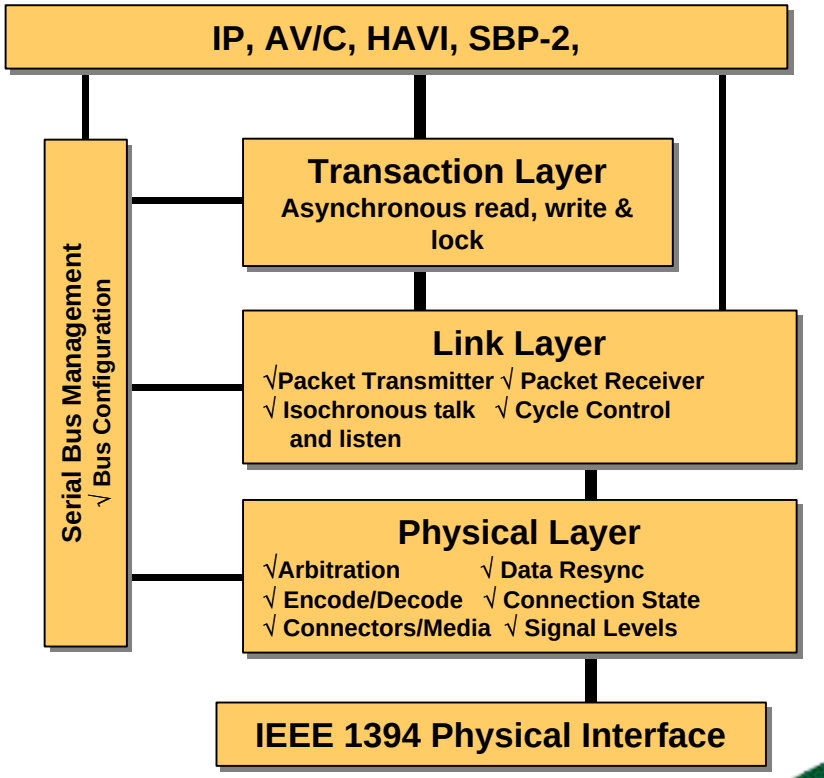
1394 Physical Addressing

- 64-bit Address
  - 48-bit offset
    - register access in node
  - 10-bit bus ID
  - 6-bit node ID
    - dynamically allocated
    - 3F broadcast
- 64K Nodes Max
  - Over bridged buses

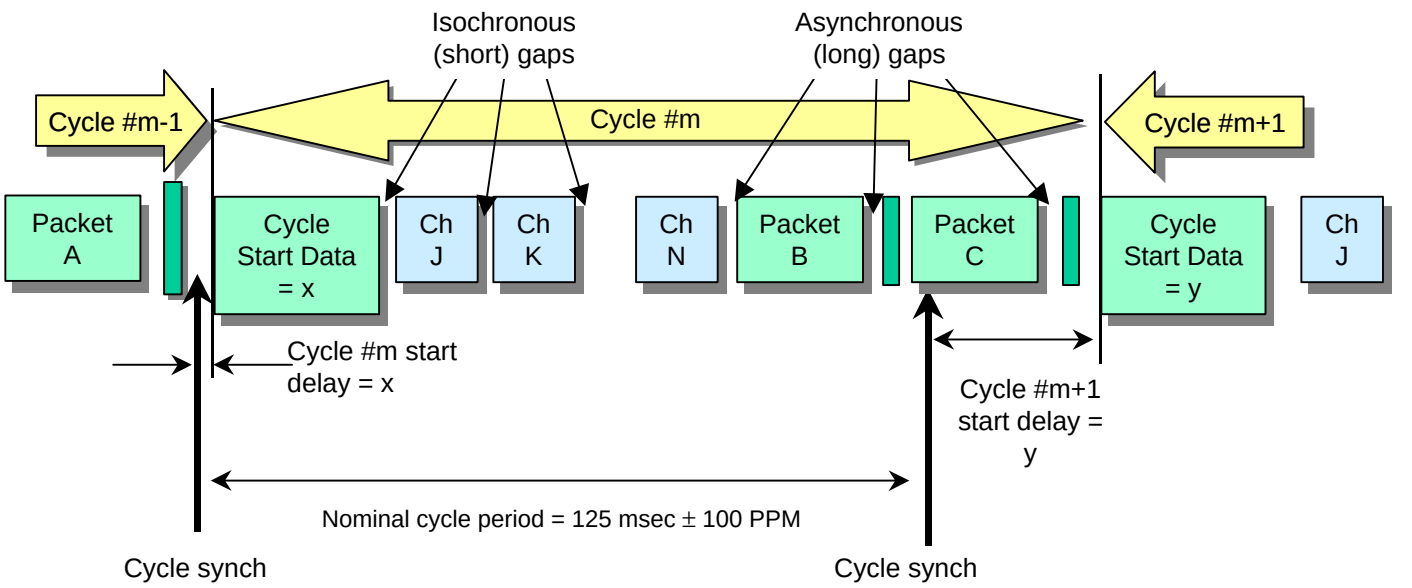


Protocol Architecture

- PHY is Independent Silicon
- Link is Integrated into System's Silicon
- Transaction Layer in Software or State Machine



Cycle Structure



- Isochronous Traffic is Handled in 125µs Slots
- Asynchronous Traffic Uses Remaining Bandwidth
- The Cycle Start Sent by the Cycle Master, the Root Node

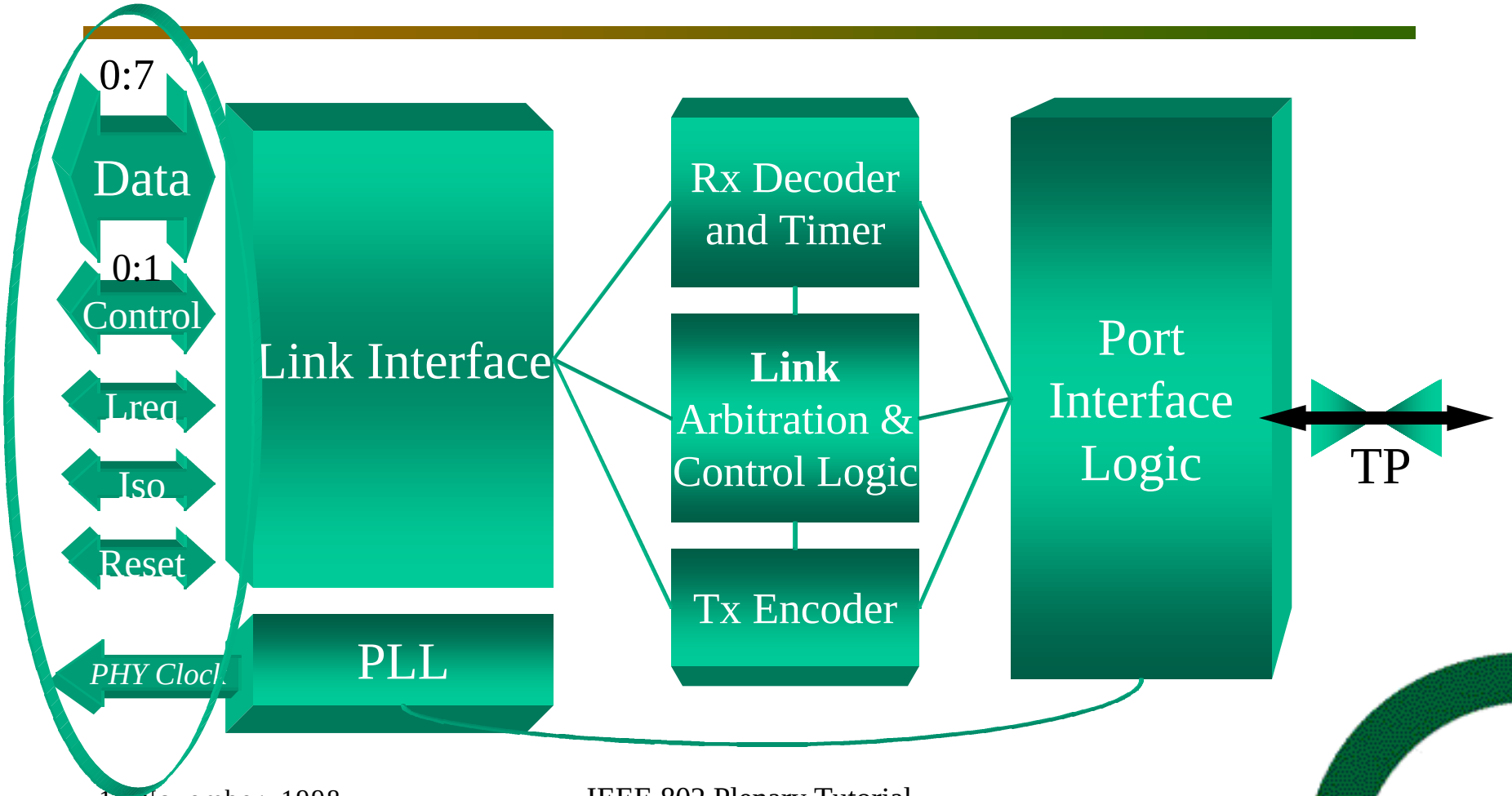
1394a

- Lower-cost 4-pin Cable
- PHY Link Interface in Normative Text
- Bus Arbitration Improvements
  - Fly-by and ack-accelerated arbitration
  - Fairness optimization
- Loop Detection and Correction
- Clean-up

IEEE 1394b

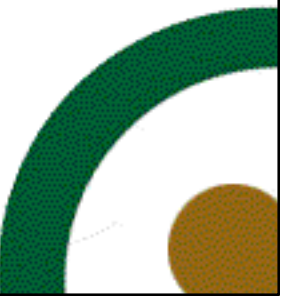
- Extended Distance
  - 100 Mbps using100m EIA/TIA CAT 5 UTP
  - 400/800/1600 Mbps using 50µm Fiber
- Support for AC Coupled Media
  - UTP uses TP-PMD and 8B10B Coding
- Support for Extended Propagation Delay
  - Multiple 100m Links

1394b PHY


0:7
Data
0:1
Control
Lreq
Iso
Reset
PHY Clock
Link Interface
PLL
Rx Decoder and Timer
Link Arbitration & Control Logic
Tx Encoder
Port Interface Logic
TP

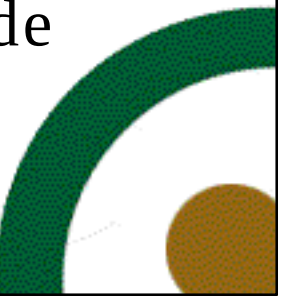
1394 / Ethernet Differences

- PHY Addresses Are Dynamic
- Confirmed Delivery for Asynchronous Packets
- Isochronous Mode
- Notification of Node Connection / Disconnection



1394.1

- Two Port Architecture
  - since *n* portals can be built with 2 portal devices and an internal bus
- Routes Asynchronous and Isochronous Traffic
- Physical Loops Permitted
  - parsed into logical tree for routing
- Virtual Node Address Mapping
- Bus Address Allocation Scheme Similar to Node Addressing

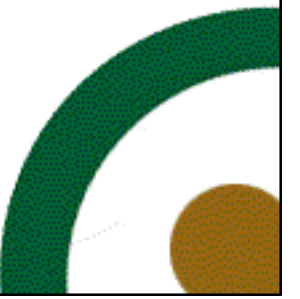


Some 1394 Web Sites

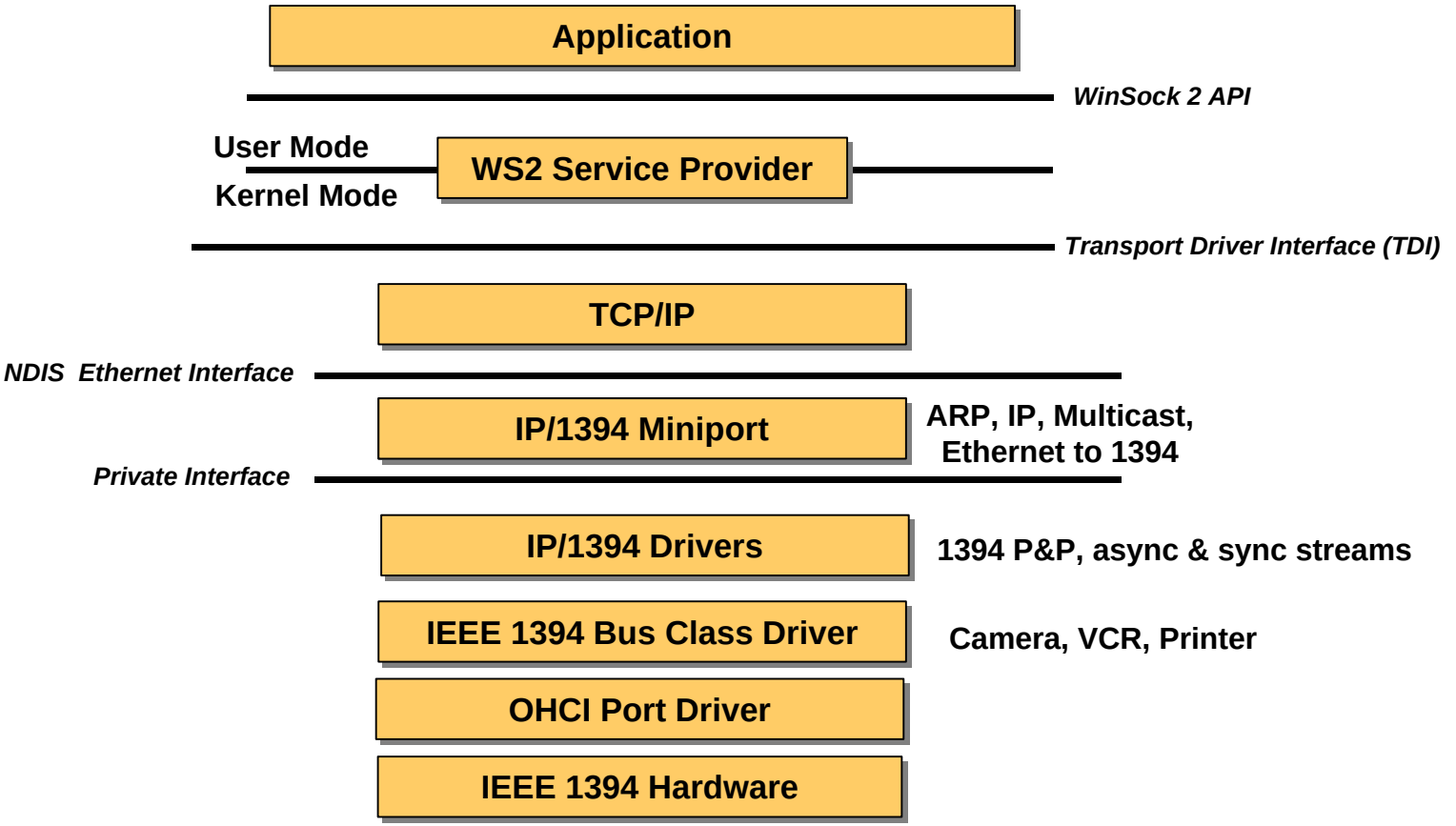
- 1394 Trade Association
  - 1394ta.org (has links to related sites)
- IEEE P1394b
  - www.zayante.com/p1394b
- IEEE P1394.1
  - grouper.ieee.org/groups/1394/1

IETF IP/1394

- IPv4 over 1394 spec (RFC from IETF) is available
  - www.ietf.org/ids.by.wg/ip1394.html
- IP 1394 miniport driver interfacing to NDIS TCP/IP



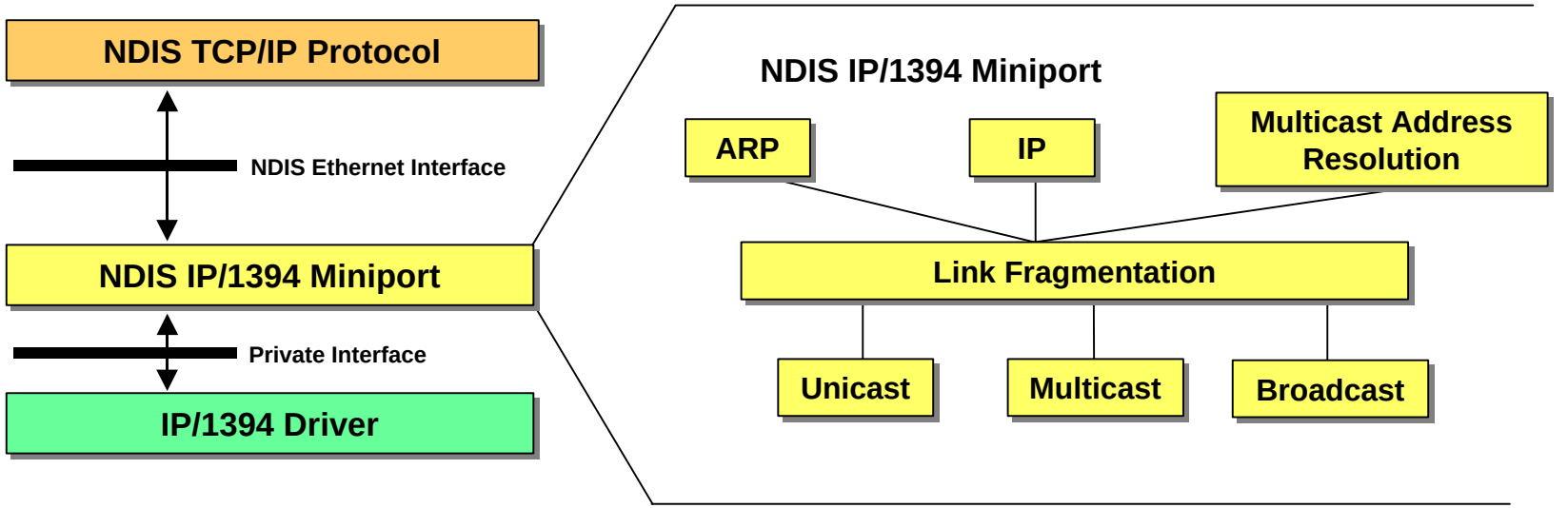
Complete Protocol Stack



Summary

- 1394-1995 began in 1986 and was approved in December, 1995
- 1394a began in 1995 and should be approved next month
- 1394b scheduled for balloting in 1999
- 1394.1 in first complete draft

NDIS IP/1394 Miniport



ARP

- Cache pseudo-Ethernet,EUI-64, IEEE 1394 address (16-bit node ID, 48-bit offset)

IP

- Map pseudo-Ethernet to EUI-64 to IEEE 1394 address
- Strip/add Ethernet headers

Multicast

- Allocate IEEE 1394 channel
- Advertise mapping of IEEE 1394 channel to IP multicast

Current Issues (1)

- Virtual NODE_Ids
- Higher layer protocols and applications
- Routing table setup
- Congestion
- Virtual bus behavior
- Error and retry handling

Current Issues (2)

- Different time on different buses
- Isochronous time stamp adjustment
- Longer split timeout
- Reset notification
- Access to registers on other buses
- Packet size and speed
- Isochronous stream setup