

PAR FORM

PAR Status: New PAR (Unapproved PAR)
PAR Approval Date: 0000-00-00
PAR Signature Page on File: No

1. Assigned Project Number: 1896

2. Sponsor Date of Request: 2004-05-12

3. Type of Document: Standard for

4. Title of Document:

Draft: Memory Channel Standard

5. Life Cycle: Full-Use

6. Type of Project:

6a. Is this an update to an existing PAR? No

6b. The Project is a: New Standard

7. Working Group Information:

Name of Working Group: Memory Channel Working Group

Approximate Number of Expected Working Group Members:50

8. Contact information for Working Group Chair:

Name of Working Group Chair: Bob Davis

Telephone: 408-353-2706 **FAX:** 408-353-8116

Email: bob@scsi.com

9. Contact information for Co-Chair/Official Reporter, Project Editor or Document Custodian if different from the Working Group Chair:

Name of Co-Chair/Official Reporter, Project Editor or Document Custodian:

Telephone: **FAX:**

Email:

10. Contact information for Sponsoring Society or Standards Coordinating Committee:

Name of Sponsoring Society and Committee: Computer Society Microprocessors and Microcomputers

Name of Sponsoring Committee Chair: Bob Davis

Telephone: 408-353-2706 **FAX:** 408-353-8116

Email: bob@scsi.com

Name of Liaison Rep. (if different from the Sponsor Chair):

Telephone: **FAX:**

Email:

Name of Co-Sponsoring Society and Committee:

Name of Co-Sponsoring Committee Chair:

Telephone: **FAX:**

Email:

Name of Liaison Rep. (if different from the Sponsor Chair):

Telephone: **FAX:**

Email:

11. The Type of ballot is: Entity Sponsor Ballot

Expected Date of Submission for Initial Sponsor Ballot: 2005-12-15

12. Fill in Projected Completion Date for Submittal to RevCom: 2006-06-10

Explanation for Modified PAR that completion date is being extended past the original four-year life of the PAR:

13. Scope of Proposed Project:

The scope of this project is to develop a flexible, scalable, secure data interface to transfer data to and from storage. This protocol will be technology independent, to be supported by current communications links, and will remove size and distance limitations on data retrieval, with additional data redundancy and data coherency methods.

Is the completion of this document contingent upon the completion of another document? No

14. Purpose of Proposed Project:

This project will develop a memory transport protocol capable of supporting data growth and data security requirements in the changing microprocessor environment. Memory is stored data in many forms and locations. This Memory Channel protocol shall be independent of link technology. This protocol shall be capable of transparent, secure, access to large, local and remote memory systems, employing coherent and redundant storage methods.

14a. Reason for the standardization project:

The reason for developing this Memory Channel Standard is to remove the limitations on size, distance, shape, speed, and security levels associated with the access to stored data devices - memory - including RAM, ROM, Flash, Disk, and any other method(s) of storing information. This Memory Channel Standard will be a Generic Memory Interconnect and:

1. Remove any memory size and location constraints;
2. Be an Extensible Design with Room for Options and Future Developments;
3. Defines a Memory Channel Protocol independent of any link technology;
4. Does not change at each new Processor design;
5. Will be capable of Plug-n-Play operation;
6. Capable of RAIMM Operation (RAID with/without rotation) *RAIMM - Redundant Arrays of Inexpensive Memory Modules;
7. Design optimized for flexibility and versatility over performance;
8. Provide Extensive Data Protection in addition to link level protection;
9. Provide for Data security required- assume all transactions monitored;
10. Supports Smart Memory Modules concepts;
11. Supports RDMA Remote Direct Memory Access.

The beneficiaries of Memory Channel Standard are:

1. Processor Vendors-No needed knowledge of Memory Module Architecture;
2. Memory Vendors-More Optimized Memory Design, Less physical driving constraints-Add interface to chip for smallest systems;
3. System Builders-More Options for Memory, Better Signal Integrity design, Faster Time To Market, Capable of Upgrade after sale, Expanded System Architecture to meet specific design goals, Component Compatibility over time for longer product life;
4. Memory Module Vendors - More design freedom in sub-unit design, Opportunity to add capabilities for differentiation, Memory is Memory is Memory - different technologies;
5. Users - Plug-n-Play, Capable of upgrading system memory and performance, Ability to support special applications needs, Expanded memory solutions available with wider cost/performance Options.

15. Intellectual Property:

Has the sponsor reviewed the IEEE patent policy with the working group? Yes

Is the sponsor aware of copyrights relevant to this project? No

Is the sponsor aware of trademarks relevant to this project? No

Is the sponsor aware of possible registration of objects or numbers due to this project? Yes

This project will support the IEEE RAC EUI and OUI existing practices. The addition of the World Wide Name configurations use in the INCITS committees is well known and uses the IEEE RAC OUI registration system.

16. Are there other documents or projects with a similar scope? No**Similar Scope Project Information:****17. Is there potential for this document (in part or in whole) to be adopted by another national , regional or international organization?** Yes

If yes, please answer the following questions:

Which International Organization/Committee? ISO/IEC JTC1 SC25 WG4

International Contact Information? Robert Pritchard
Consultant
440 East 79th St.
Apt. 8N
New York, NY 10021
212-517-9446
212-517-9446
r.pritchard@ieee.org

18. If the project will result in any health, safety, or environmental guidance that affects or applies to human health or safety, please explain in five sentences or less.

19. Additional Explanatory Notes: (Item Number and Explanation)