

P1796

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Resilient Backplane Ring
(RBR) slide material
2004Nov04

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IEEE standards may include the known use of essential patents and patent applications provided the IEEE receives assurance from the patent holder or applicant with respect to patents whose infringement is, or in the case of patent applications, potential future infringement the applicant asserts will be, unavoidable in a compliant implementation of either mandatory or optional portions of the standard [essential patents]. This assurance shall be provided without coercion and prior to approval of the standard (or reaffirmation when a patent or patent application becomes known after initial approval of the standard). This assurance shall be a letter that is in the form of either:

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Don't discuss licensing terms or conditions

Don't discuss product pricing, territorial restrictions or market share

Don't discuss ongoing litigation or threatened litigation

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RBR's IEEE heritage

- IEEE Std 1212 – 1991 CSR Architecture
Indivisible memory-mapped update operations
- IEEE Std 1596 – 1992 Scalable Coherent Interface (SCI)
Busy-retry destination-based flow control
- IEEE Std 1394 – 1995 Serial Bus
Isochronous path reservations, time-sync, and per-cycle transmissions
- IEEE Std 802.17 – 2004 Resilient packet ring (RPR)
Scalable network-on-a-ring, classes of service, resiliency
- IEEE 802.3ap Backplane Ethernet Task Force
Physical layers for the backplane (PHYs)
- IEEE 802 (CE) Study group
Isosynchronous path reservations, time-sync, and frame formats

Similar industry technologies

- Infiniband
- HyperTransport
- PCI-express
- Rapid I/O
- Others?
 - Fiber-channel, serial ATA, serial SCSI, FDDI

Current status

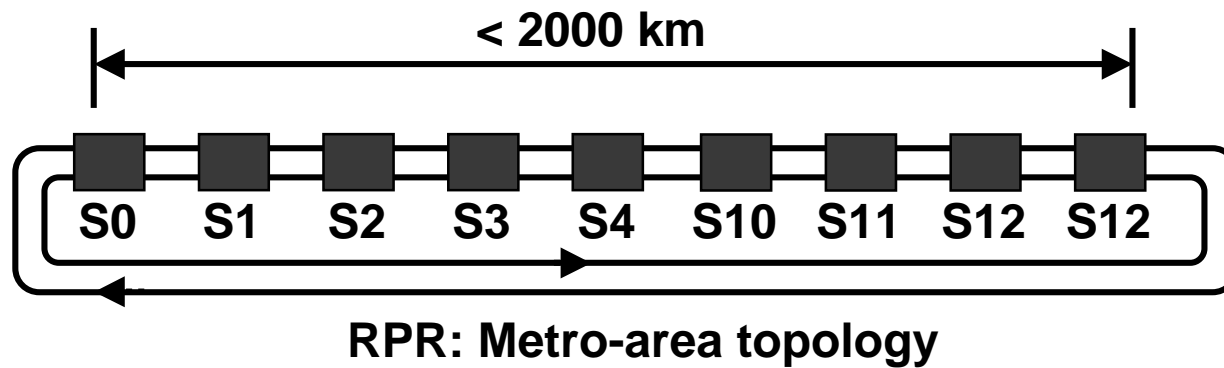
- **Study group authorized by MSC January, 2004**
- **PAR approved June 24, 2004**
- **Scope:**
 - Resilient backplane ring (RBR) is a backplane interconnect based on the dual-ring resilient topology of resilient packet ring (RPR) and the 802 MAC addressing structure. RBR includes features appropriate for the low-latency backplane environment: destination-based flow control, low-power short-haul PHY, backplane-to-backplane links, transport of IEEE-1394 isochronous data, and support of IEEE-1596 memory-update operations.
- **Purpose:**
 - The purpose of this project is to leverage the benefits of network-compatible resilient interconnects within low-latency backplane environment.

Reasons for the RBR standard

- High speed backplanes are oftentimes used within the networking environment, where designs can be simplified by sending network frames and card-to-card communications over the same links.
- Although the resilient packet ring (RPR) has the quality of service (QOS) needed for card-to-card communications, other facilities associated with a low-latency backplane environment are missing.
- When RPR like protocols are supplemented with latency-critical backplane services, the resulting backplane interconnect should be sufficient for many mixed application backplane designs.
- Affected sectors would include enterprise networking and computer server industries; perhaps 100s or hopefully 1000s of companies.

**RPR summary
(a similar existing standard)**

RPR topologies



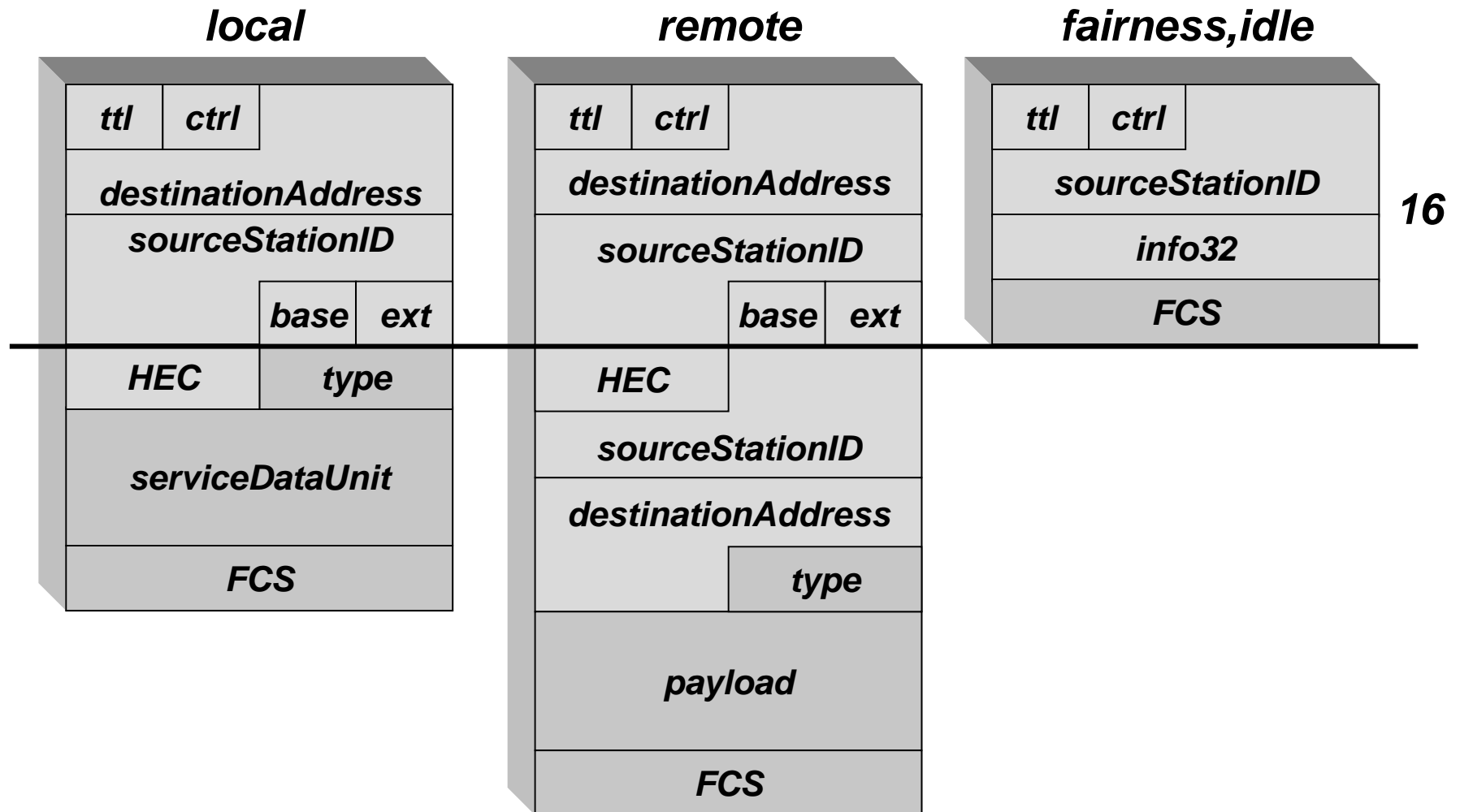
SONET environment applications

Duplex counter-rotating rings with spatial reuse

IEEE 802 frames, with ring-routing supplements

Several product-in-field constraints

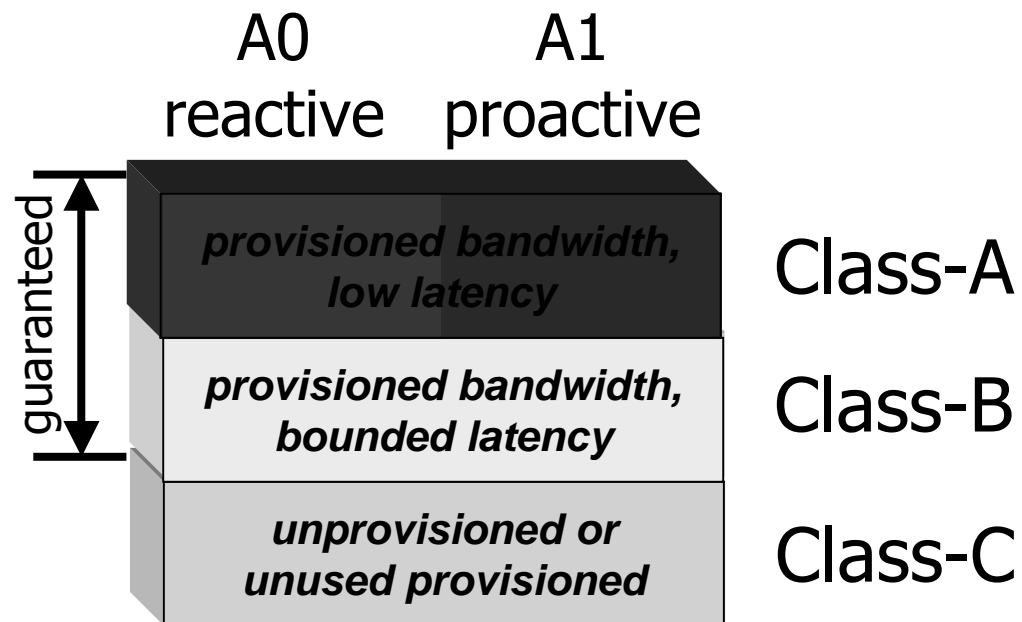
RPR format summary



RPR → RBR simplifications

- ~~Steering, edge wrap, and center-wrap protection.~~
- ~~Single queue and dual queue transit buffers.~~
- ~~Rate based and credit based shapers.~~
- ~~Parity, 16-bit hec, 32-bit fcs, 32-bit hec, and 32-bit fcs.~~
- ~~Conservative and aggressive fairness, without adaptive.~~
- ~~Multichoke “hooks” and single-choke specification.~~
- ~~Negotiated capabilities:~~
 - ~~wrapping mode (→ center wrap)~~
 - ~~jumbo capable (→ all are transit-capable)~~
 - ~~conservative fairness (→ all are adaptive)~~

Arbitration classes



RBR distinctions

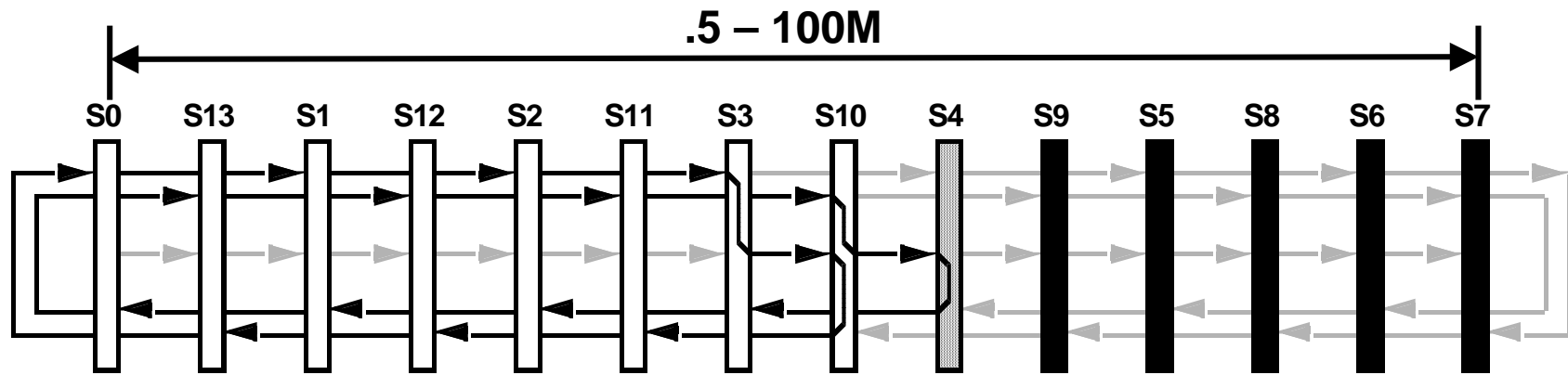
- **WG development process**
 - **Straw men proposals (more than slideware)**
- **RBR is within smaller “boxes”**
 - **Reaction times are much smaller**
 - **Destination-congestion: “retry” becomes practical**
 - **Low-powered transceivers are a must**
- **RBR plug-and-play vs RPR single-vendor acquisitions**
 - **Elimination of most configurable “knobs”**
 - **Negotiated real-time bandwidths**
 - **Real-time bandwidths are “real”**
 - **Specified time-of-day synchronization**

RBR summary (a starting point)

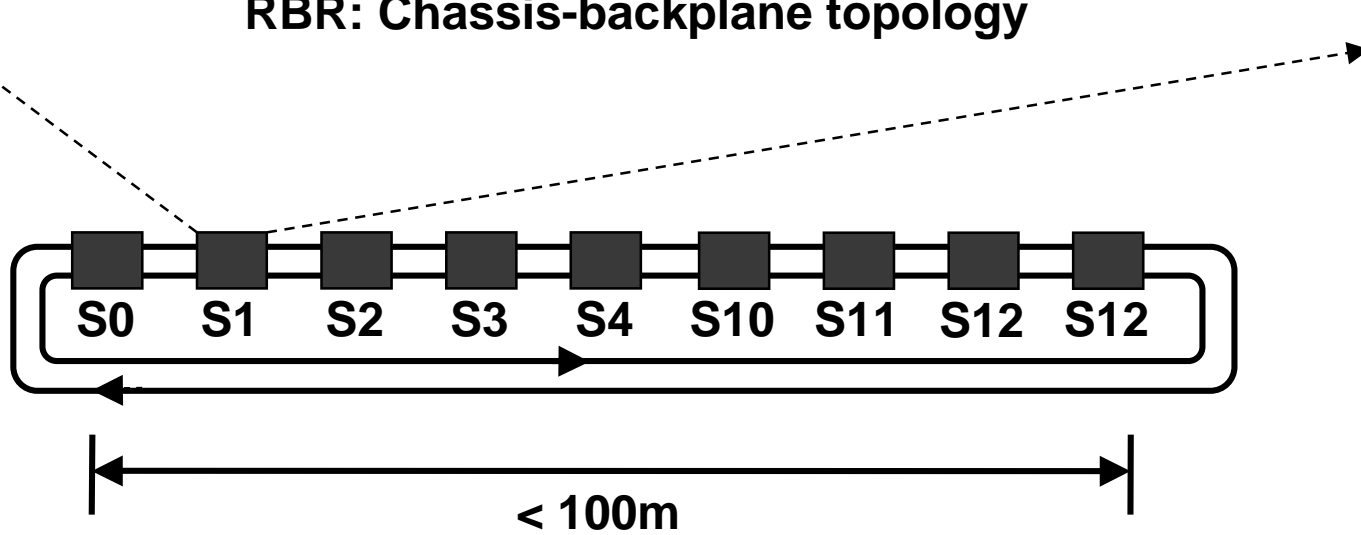
RBR protocol summary

- Leveraged RPR values:
 - Ethernet frames with QOS delivery
 - Ring efficiency and resiliency
- QOS enhancements
 - Accurate time-of-day synchronization
 - Revised/verified classA1/classB guarantees.
 - Quasi-synchronous isochronous transfers
 - Negotiated access controls.
- Lossless transactions
 - Destination-asserted flow control
 - Hard-coded memory-access commands
 - Request/response queuing options
- Backplane PHY definitions

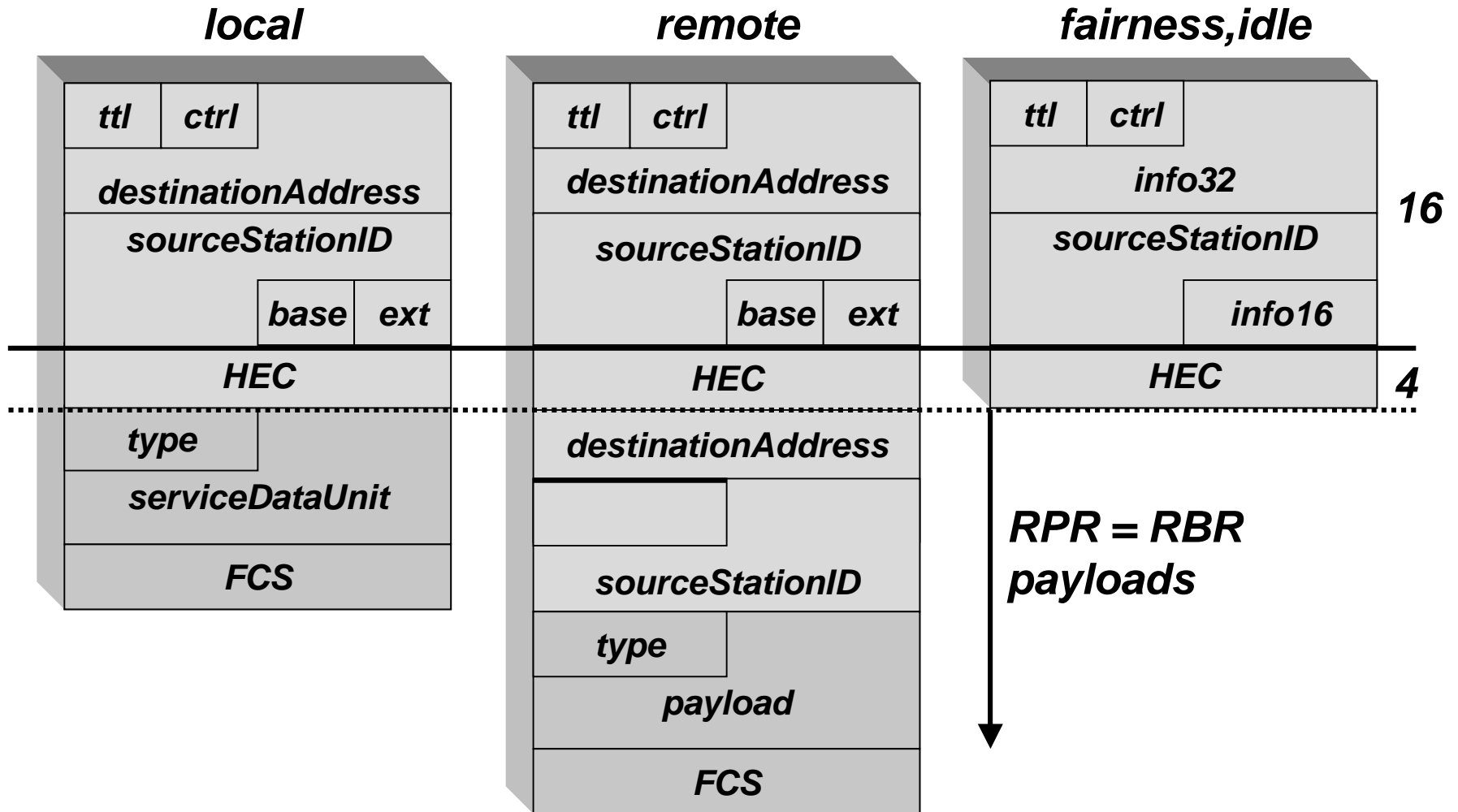
RBR topologies



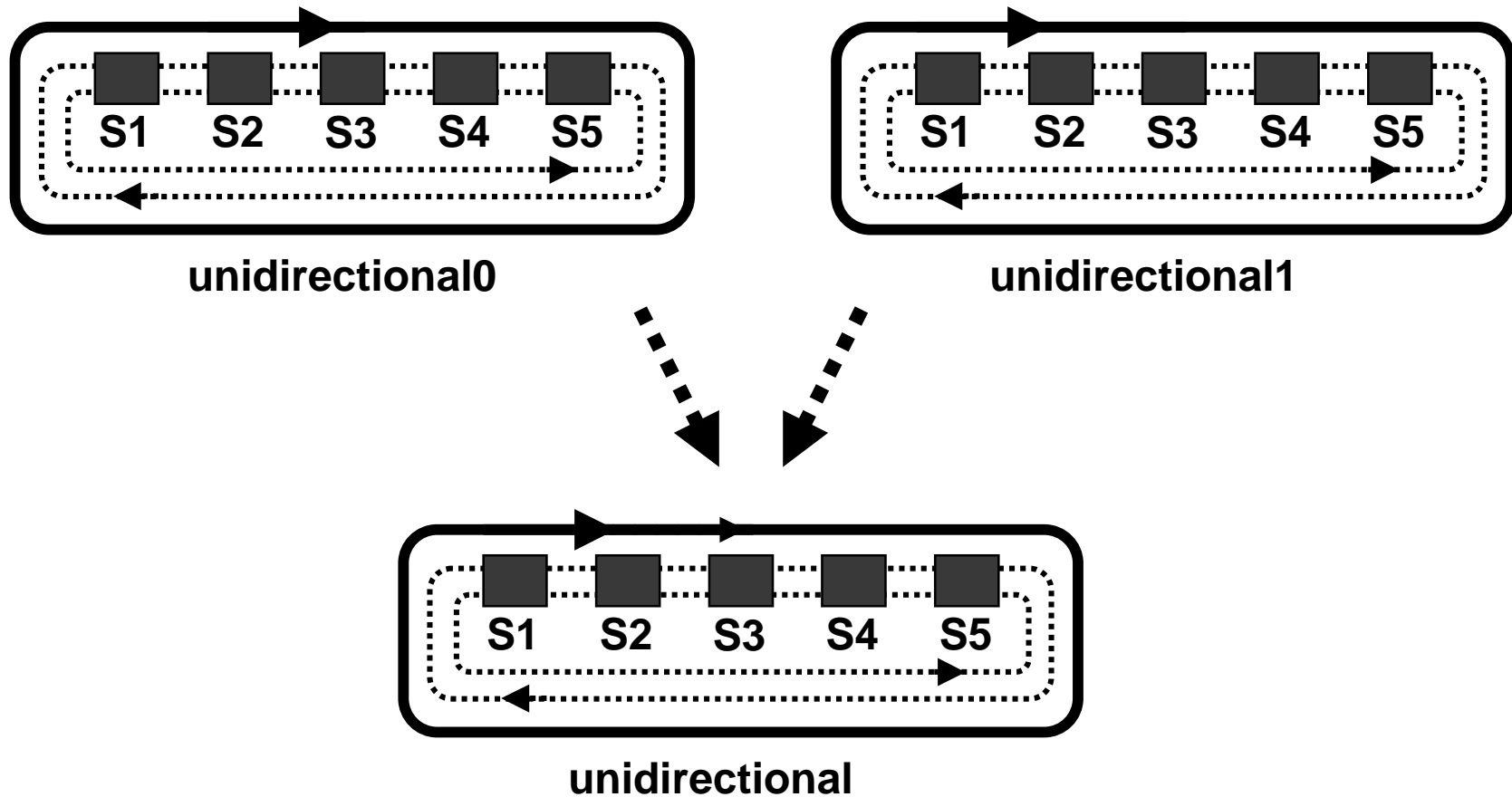
RBR: Chassis-backplane topology



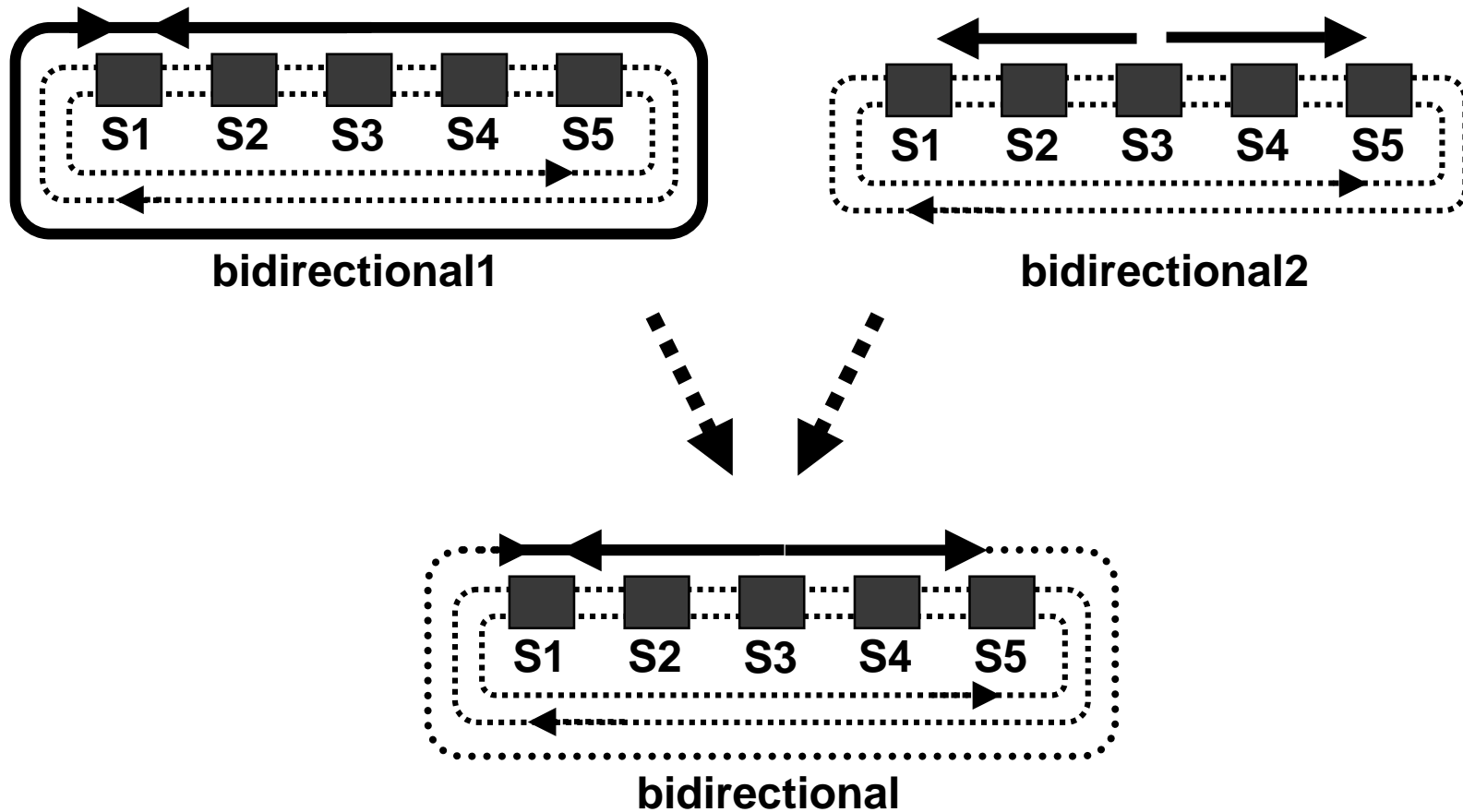
RBR format summary



Unidirectional flooding

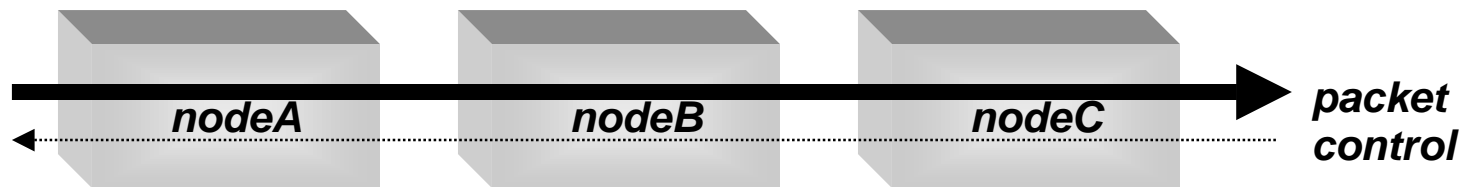


Bidirectional flooding



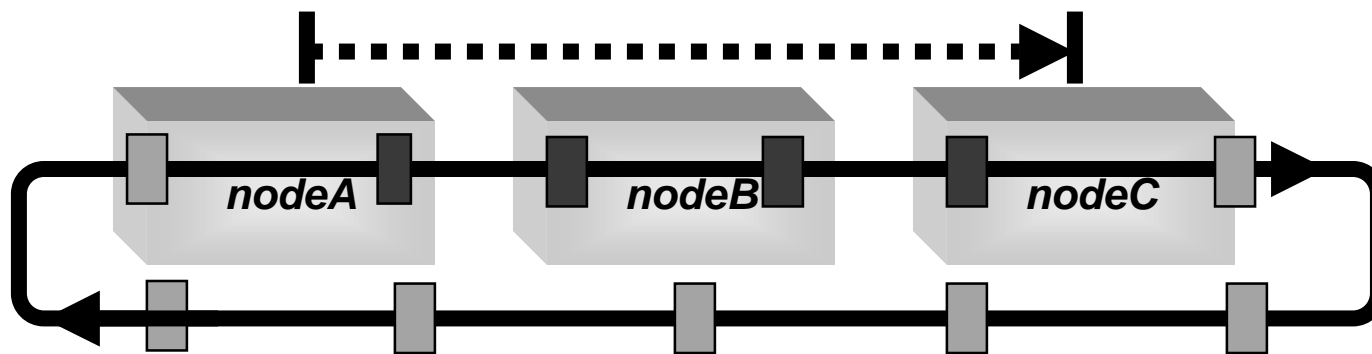
Flow control

Opposing arbitration



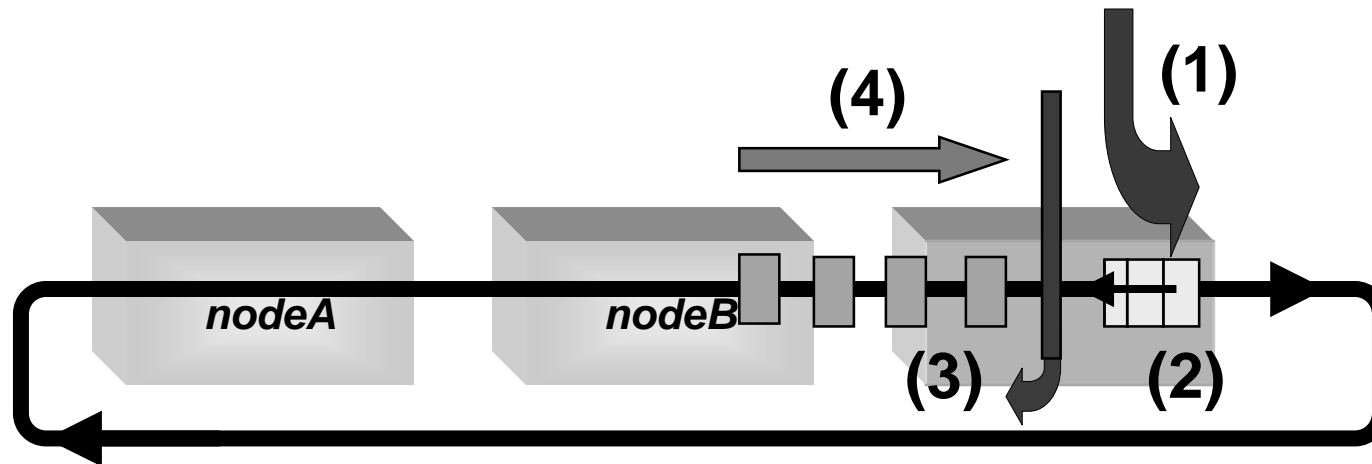
- Data packets flow in one direction
- Arbitration control flows in the other*

Proactive class-A0 partitions



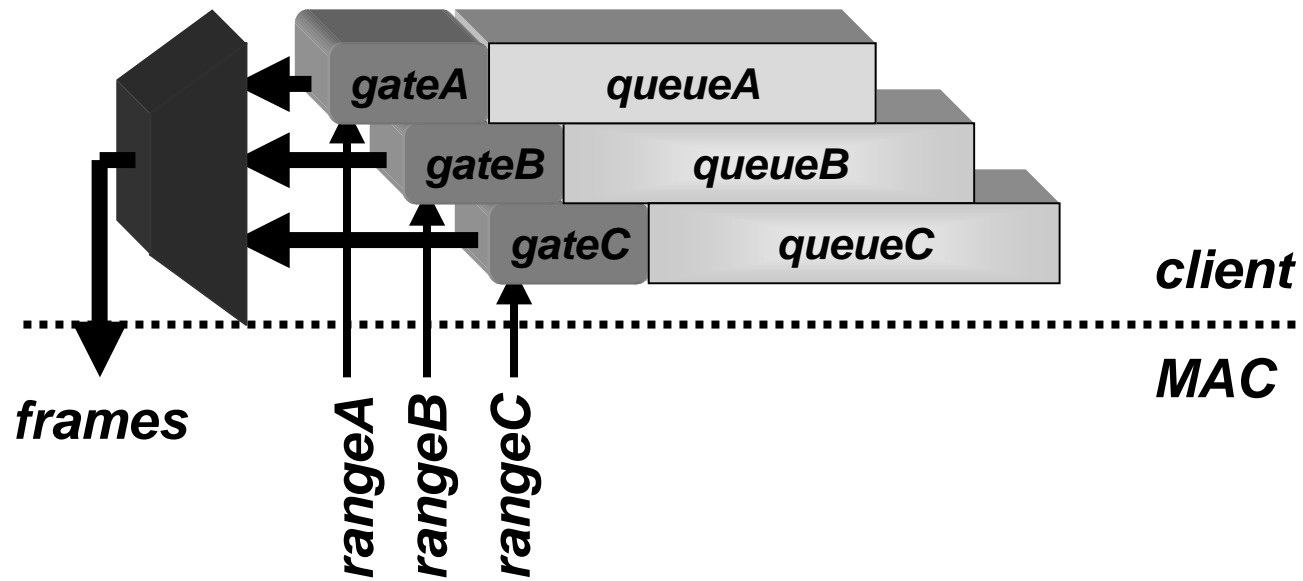
- Data packets go source-to-destination
- Residue returns destination-to-source to provide subsistence for transmissions

Reactive class-A1 control

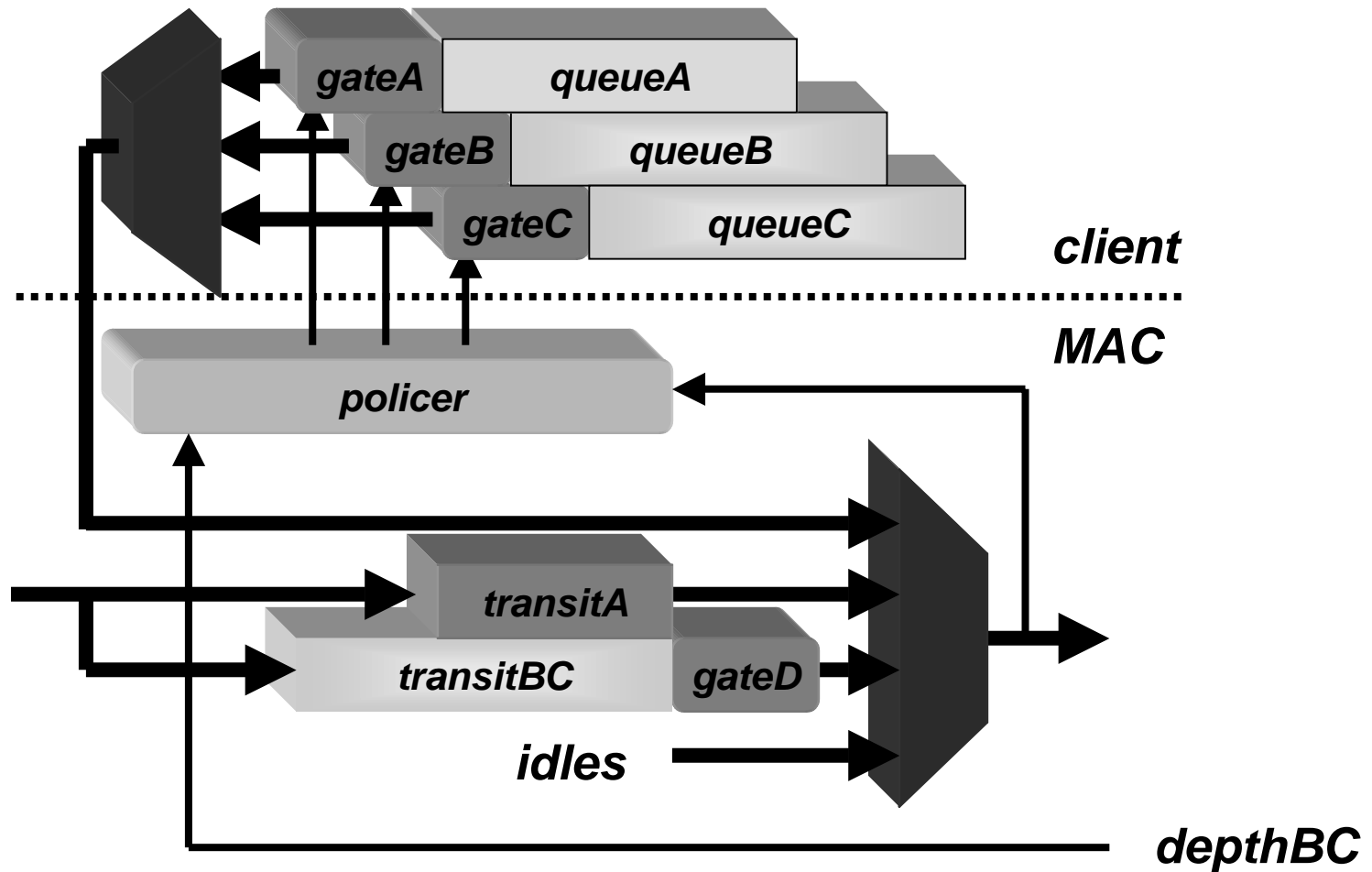


- Transmission of packets causes
- Backup of passBC FIFO that
- Returns flow-control information that
- Provides consumable idle packets

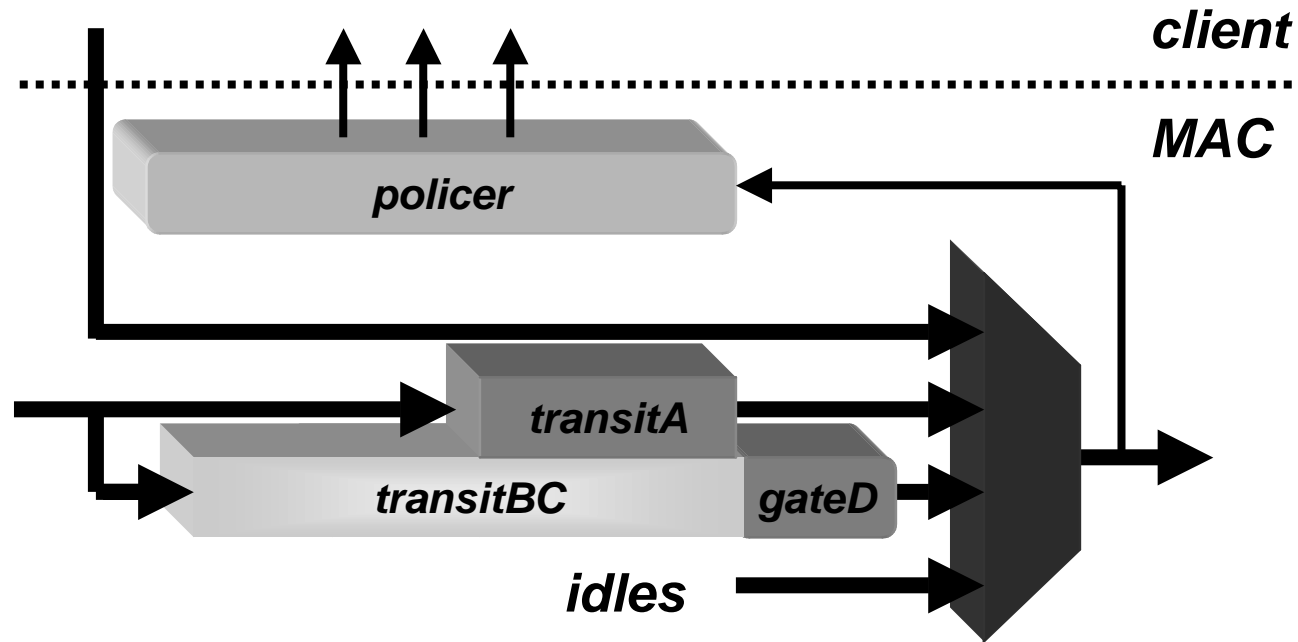
MAC-Client interface signals



Arbitration components

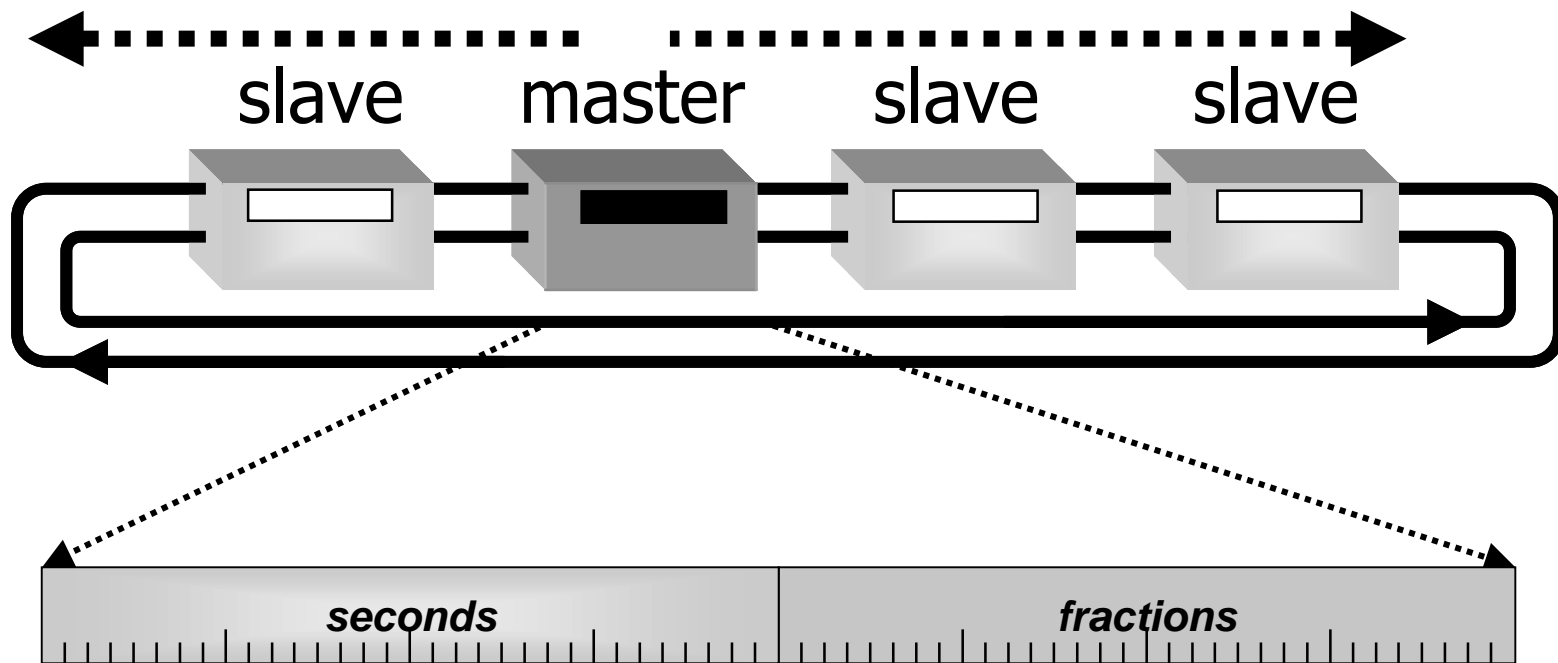


Small-to-large transitBC



- 1) *Small* => *proactive classA0*
- 2) *Medium* => *mixed classA0/classA1*
- 3) *Large* => *reactive classA1*

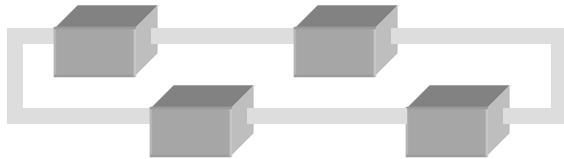
Time-of-day synchronization (not bit-clock synchronization)



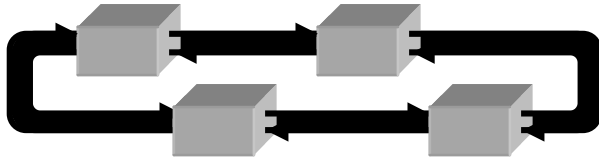
Operations, administration, and maintenance (OAM)

- Recovery from failed components
 - “Protection” via wrap&steer
- Identify failing components
 - MIB counts
 - stomped CRCs

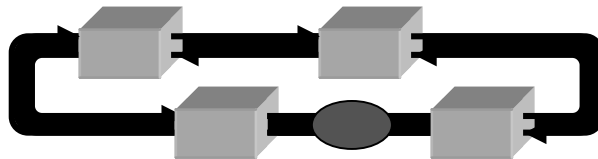
Supported topologies



- A physical ring

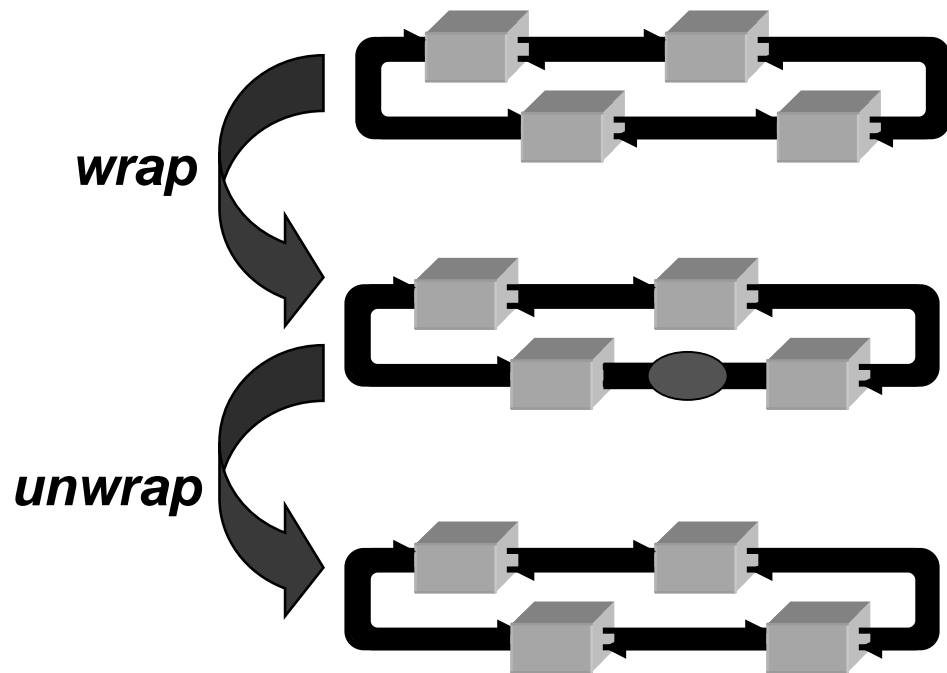


- Dual ringlets



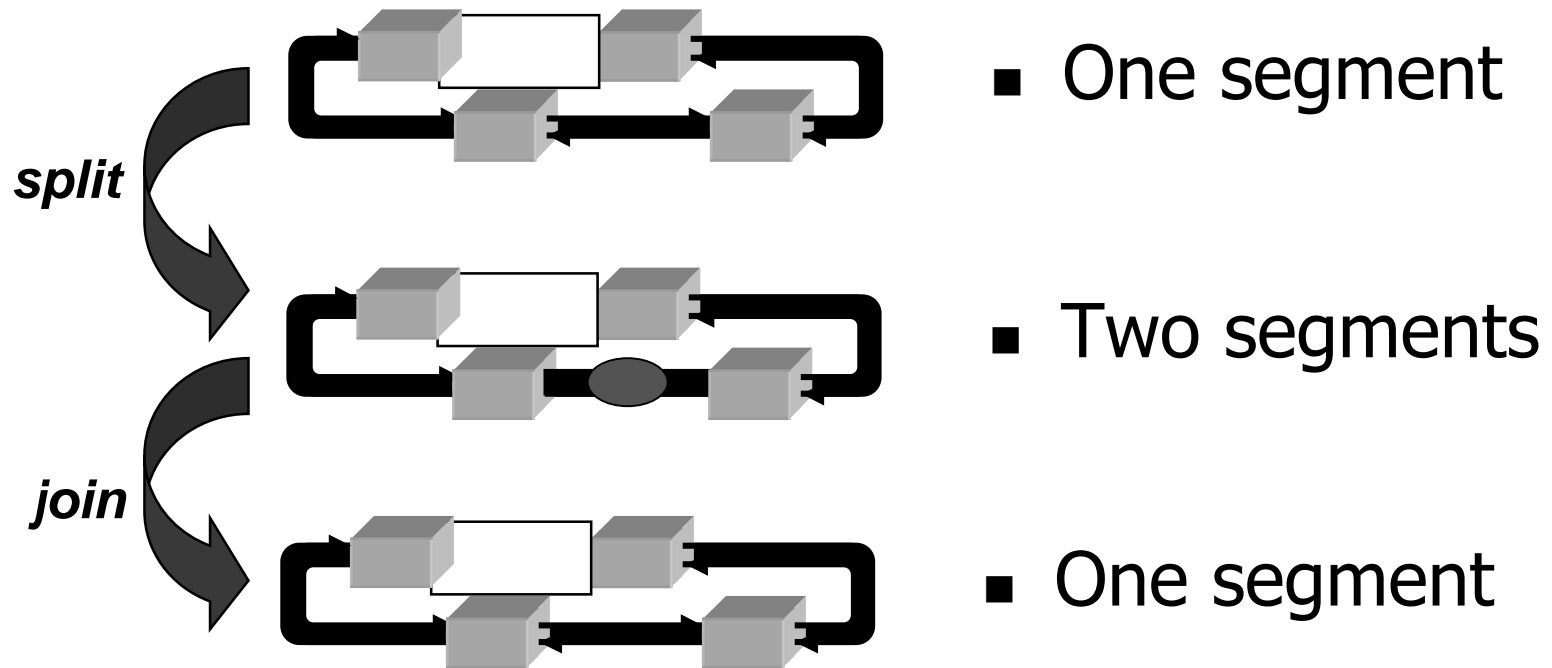
- Duplex ringlet

Link failures: wrap & unwrap

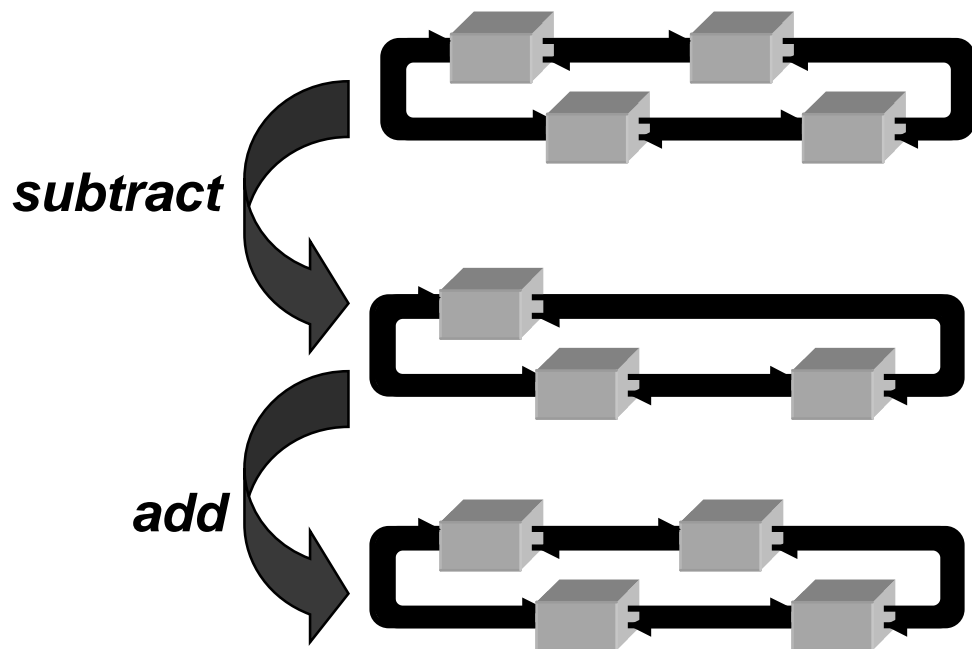


- Dual ringlets
- Duplex ringlet
- Dual ringlets

Link failures: split&join



Link failures: subtract & add

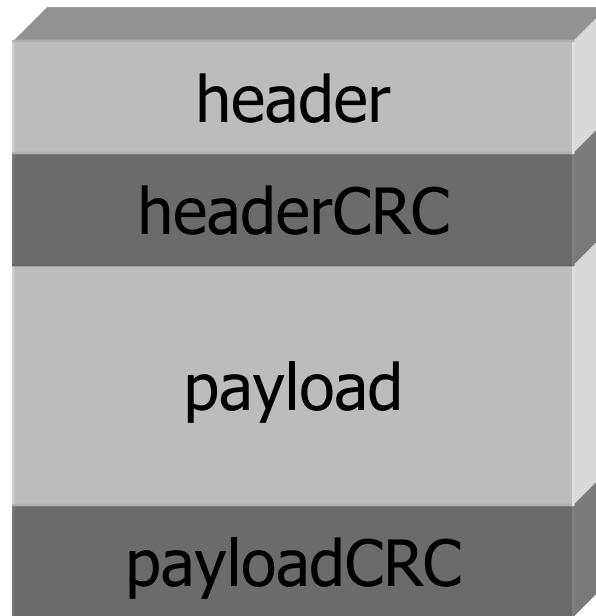


- Basic ringlet
- Reduced ringlet
- Basic ringlet

CRC processing

- **Store&forward/Cut-through agnostic**
- **Invalid data is effectively discarded**
 - **store-and-forward discards**
 - **cut-through stomps the CRC**
- **Maximize error-logging accuracy**
 - **Separate header&data CRCs**
 - **“most” corruptions hit the data**

Separate header and data CRCs

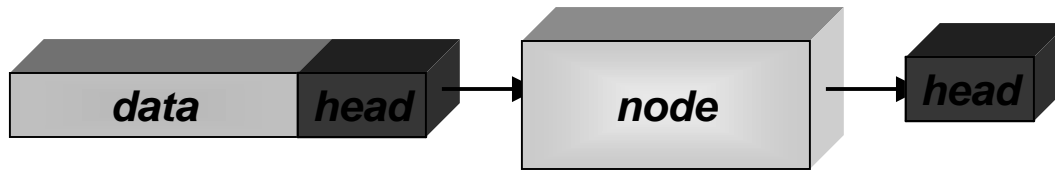


Cut-through CRCs

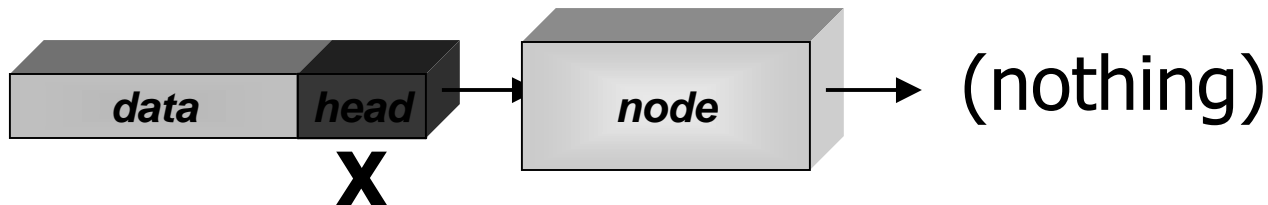


- Corrupted packet remains corrupted
- Error logged when first detected
- ```
if (crcA!=crc) {
 errorCount+= (crcA!=crc^STOMP);
 crcB= crc^STOMP;
}
```

# Distinct CRCs reduces discards

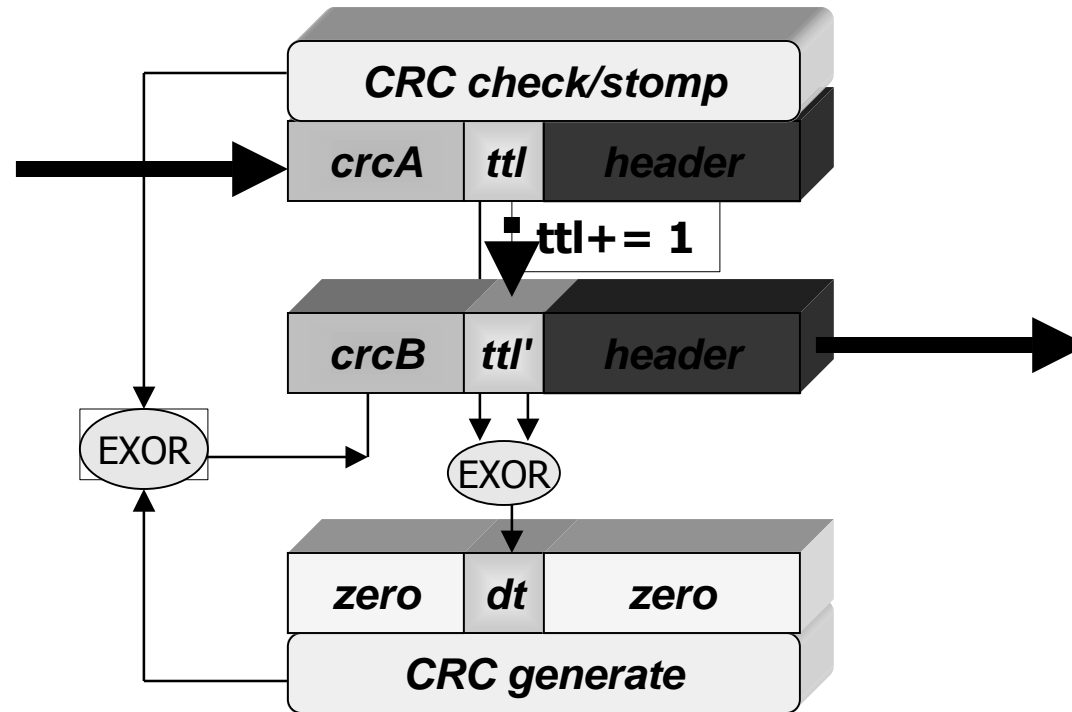


- Discard the corrupted data



- Discard the corrupted packet

# End-to-end CRC protected TTL



# CRC equation examples

```

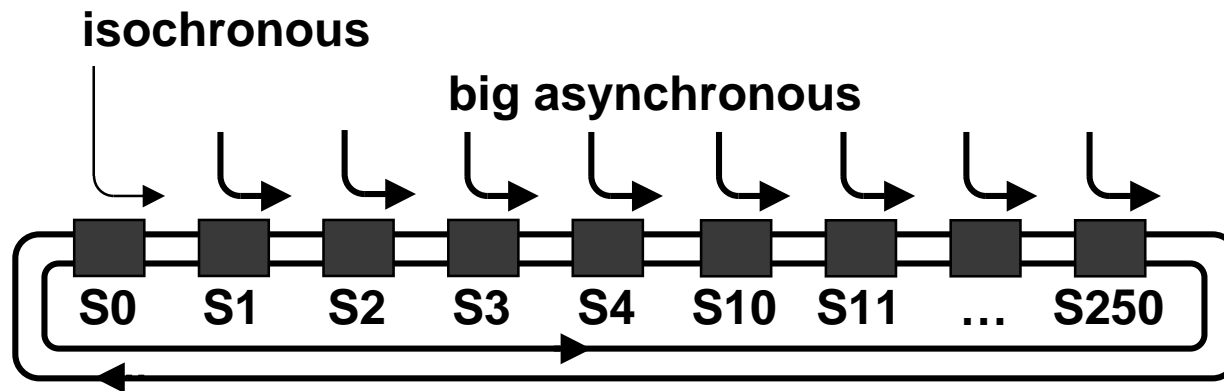
a= c00^d00; b= c01^d01;
c= c02^d02; d= c03^d03;
// ...
s= c14^d14; t= c15^d15;
c00= a^ e^ g^h^ m^
c01= b^ f^ h^j^ n^
c02= c^ g^ j^k^ p^
c03= d^ h^ k^m^ r^
c04= e^ j^ m^n^ s^
c05= f^ k^ n^p^ t^
c06= a^ e^ h^ p^r^
c07= b^ f^ j^ r^s^

```

# Difficult remaining problems

- **Classes of service**
  - **Tight classA latency guarantees**
  - **Unconstrained classB levels**
- **Destination-based flow control**
  - **Busy retry has the right properties**
  - **per-source feedback is simple**
  - **output-port feedback is possible**
  - **Overhead must not exceed 1 retry**

# Worst-case isoch delays

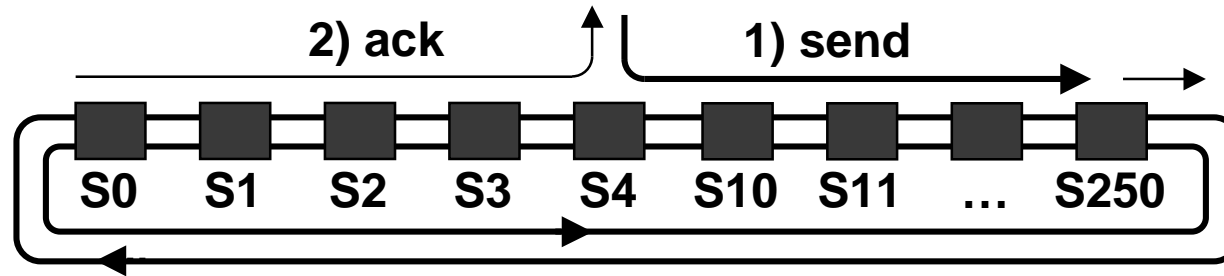


**collisionDelay = stations \* MAX\_SIZE;**

**1.5kB @ 1Gb w/250 stations → 12us \* 250 → 3 ms**

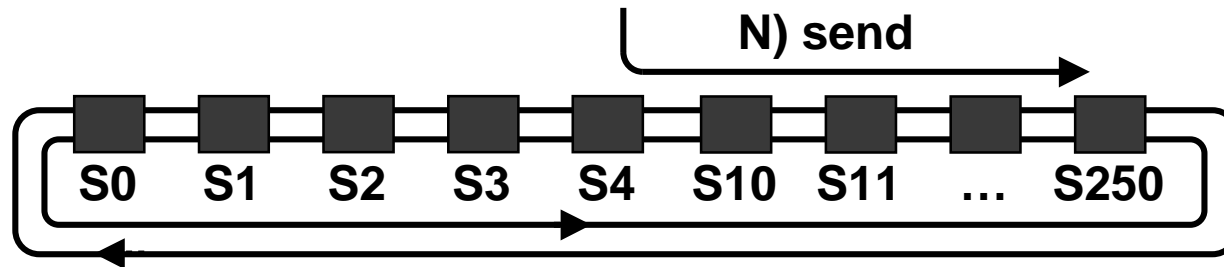
**8.5kB @ 1Gb w/250 stations → 68us \* 250 → 17 ms**

# Destination-based flow



(A) Initial try

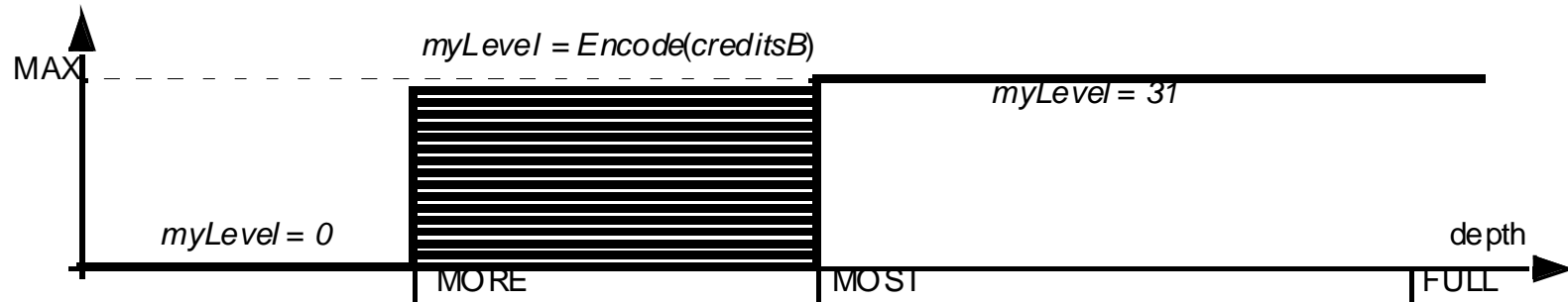
[ (B) TBD signaling ]



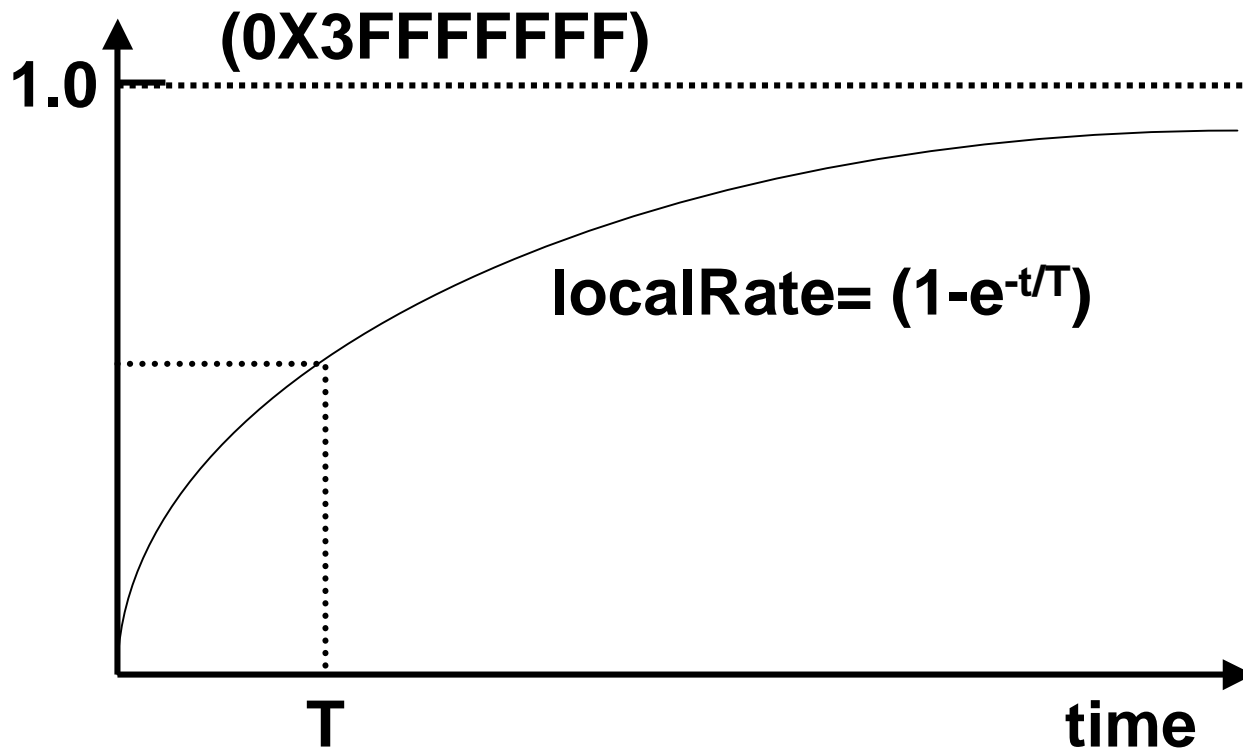
(C) Final retry

# **Evolving slides**

# Queue depth feedback



# DSP perspectives



## Instructions for the WG Chair

- At Each Meeting, the Working Group Chair shall:
  - Show slides #1 and #2 of this presentation
  - Advise the WG membership that:
    - **The IEEE's Patent Policy is consistent with the ANSI patent policy and is described in Clause 6 of the *IEEE SA Standards Board Bylaws*;**
    - **Early disclosure of patents which may be essential for the use of standards under development is encouraged;**
    - **Disclosures made of such patents may not be exhaustive of all patents that may be essential for the use of standards under development, and that neither the IEEE, the WG nor the WG Chairman ensure the accuracy or completeness of any disclosure or whether any disclosure is of a patent that in fact may be essential for the use of standards under development.**
- Instruct the WG Secretary to record in the minutes of the relevant WG meeting:
  - **that the foregoing advice was provided and the two slides were shown;**
  - **that an opportunity was provided for WG members to identify or disclose patents that the WG member believes may be essential for the use of that standard;**
  - **any responses that were given, specifically the patents and patent applications that were identified (if any) and by whom.**