I. INTRODUCTION

In conjunction with the SSC20 Liaison Standards Subcommittee of the Institute of Electrical, Electronic Engineers (IEEE) Standards Organization [1], a new multidimensional ATE “Open System Platform” packaging standard has been initiated under IEEE-P1552 Structured Architecture for Test Systems (SATS). This architecture will have a profound impact on current test computer-busboard systems in reducing costs and size, while improving performance and supportability.

The key to ATS Integration and Test Program Set (TPS) cost reduction/avoidance requires us to reduce variations of the software/hardware interfaces between ATS. Standardization functionally defines and provides guidelines for developing the interfaces within an ATS. Applying these standards with Commercial Off The Shelf (COTS) modular compatible pluggable modules, the ATS structure becomes more homogenous in its integration and supportability. This open architecture approach avoids unique government requirements and associated nonrecurring costs, enhances product availability/performance, and benefits from industry investment/technology.

SATS replaces/extends the current two dimensional plug and play computer-based architecture of VMEbus [2], VXIbus [3], PCIbus [4], PXIbus [5], and several other standards into a multidimensional integrated hardware architecture, as shown by Figure 1. Under the SATS Frameworks, Instrument/Power Mezzanine (IPM) Carrier Modules and Serial/Test Bus Integration, the current 2-D backplane is reconfigured into 3-D matrix wiring panels supporting control, power, and signal interconnectivity.

Legacy VMEbus, VXIbus, PCIbus, PXIbus Standards are supported through a hybrid process that integrates respective backplane standard characteristics with SATS wiring panel specifications. Legacy standards can choose to integrate current front connectors to SATS wiring panels, or convert to the SATS common CompactPCI [6] connector family. SATS reduces dissimilar front panel connector proliferation and eliminates wire between chassis systems. This has the potential of reducing Automatic Test Systems (ATS) material costs, labor, test time, and support by 40%.

II. TECHNICAL PROBLEM

The technical problem of this Standard was first addressed by Department of Defense memorandum OSD (A&T) - 29Apr94, DOD Policy for Automatic Test Systems, by direction of Noel Longuemare. The following memo caption reflects on the intent of Mr. Longuemare’s directive and serves to lead our efforts: “ATS capabilities shall be defined through control of critical hardware and software elements and interfaces to ensure DOD family tester and COTS tester and component interoperability, and to meet future DOD test needs”.

A joint government/industry Critical Interface Working Group (CIWG) effort furthered this ATS interface standardization process. It was conducted under the auspices of the military Joint Service Automatic Test Systems Research and Development Integrated Product Team (ARI), by a combined government and industry investment/technology.
The CIWG objectives were to identify the critical ATS interfaces that impacted interoperability/interchangeability of system hardware and test program set transportability. Although the results established clear definitions of the critical interfaces, very few could relate to commercial interface standards, beyond existing VXI, computer data interfaces and government specifications.

The remaining issues of the technical problem are those critical packaging and interconnect hardware interfaces not addressed by current industry standards. Hardware interfaces relate primarily to packaging and data/signal/power interconnect standards. These standards typically define mainframe and subelement (module) mechanical/electrical mating specifications, that should permit subelements to be interchanged without impact to subelement interoperability. The functional performance of the standard is normally limited to mechanical engagement, connector styles/footprints, electrical pin characteristics, and pin mapping definitions. This permits various vendor products (subelement/module) to interoperate (plug & play) with no or minimum modification by the integrator or user. Functional performance specifications of unique subelement capabilities, that exceed interoperability requirements are typically relegated to the integrator/user to define.

### III. OBJECTIVES OF THE SATS STANDARD EFFORT

The mission of this Standard effort are threefold: (first) to establish ballot ready specifications for the Structured Architecture for Test Systems (SATS) Standards; and (second) validate those specifications through fabrication of multivendor/multifunction prototype modules that would be integrated into working SATS architecture. The (third) objective is achieving Users and Integrators recognition and acceptance of the Standard(s), that in turn will drive vendor/supplier requirements. This represents a departure from previous Test Standards that were established by supplier/vendor motives, and therein reasons for their respective limitations.

Success will be measured by SATS ability to: (a) align with COTS - Commercial Off The Shelf products, that are designed to existing commercial standards, i.e. IEEE, Eurocard, VXI, VME; (b) reduce costs by exploiting commercial investment, limited non-recurring integration development, and competitive pressures; (c) improve availability and interoperability through common architectures and multivendor product offerings; (d) improve test program set transportability; (e) increase ATS supportability through standard acceptance, available technical/spares third-party support tools and resources; and (f) assure longer product life by structuring the architecture for future commercial subelement pre-planned product improvements and ATS technical insertion.

### IV. SATS GENERIC INTERFACE ARCHITECTURE

The following diagram, Figure 2, illustrates the traditional VXI based ATS hardware/electrical connector interface elements employed: (a) Rack/Chassis Mechanical Integration Structure; (b) Computer Control Interface; (c) VXI/IEEE-488 Instruments; (d) Power Distribution; (e) Cabling/Signal Interconnects; and (f) Receiver Fixture Interface Subsystem.

![Figure 2. Traditional VXI/IEEE based ATS hardware/electrical generic interfaces](image-url)
V. RELATED STANDARDS ACTIVITIES
The SATS Program minimized its specification development process by embracing current or planned Standards efforts. The following represents many of those being implemented under SATS:

VI. SATS STANDARD TECHNICAL APPROACH
The SATS Standard defines and implements a scalable/modular/cableless ATE “Open System Platform” packaging specification, conceptually shown in Figure 3, through an IEEE/IEC industry standardization process. The SATS architecture framework and respective seven (7) interfaces are intended to minimize design development by reducing complex functionality to the level of a plug-on mezzanine card (IPM). This minimizes impact to the integrated Carrier Module, Wiring Panel, and RFI structure, thereby accommodating reconfigurability, upgradeability/technical insertion and general reuse more effectively. By distributing the Switch Matrix Bus Architecture from the Carrier Module (functional access port), to the RFI System (UUT access port), in a scalable and software selectable manner, I/O selectability instrument sharing, fault tolerance, and system diagnostics are enhanced.

As the next generation to the current VXI/VME instrument/module control standards, the SATS Frameworks “open” mechanical and electrical packaging specification implements:
1) Mechanical Integration Structure (MIS) modular/scalable plug&play, cableless, environmental sealed, mainframe architecture, utilizing EIA Electronic Rack Specifications [17], Eurocard Mechanical Packaging and DIN 43355 Connectors Standards;
2) Plug-on Instrument/Power Mezzanine (IPM) Card provisioning functionality at the lowest cost/technical impact and Common Carrier Module with 3U/6U/9U scaleability;
3) Computer Control Distribution (CCD) high speed serial bus control for instrument/functional operation, test signal/power switch matrix distribution system management (see Figure 4);
4) Integrated scalable test/power distributed switch matrix for multi-asset selection/sharing;
5) IEEE-P1505 Receiver Interface with I/O switchable and scalable from 4 slot cable/PCB connector interface to 29 slot multi-OTPS Fixture engagement; and
6) Support for legacy VME/VXI/PCI/PXI test standards.

Figure 3. SATS Typical Multi-Framework ATE “Open System Platform”
VII. ELECTRICAL SYSTEM INTEGRATION FRAMEWORKS

A. ESI Overview

The Electrical System Integration (ESI) Specification defines the overall SATS Frameworks electrical interconnect system, connectorization, switching network, and electrical bus pathways for power, control and stimulus/measurement test signals. The diagram (Figure 4), correlates to the atypical configuration shown in Figure 3, reflecting general interfaces and related elements of the electrical frameworks and their respective relationships. When implemented under a plug&play architecture, that utilizes advanced high speed digital/RF printed circuit board technology, considerable benefits accrue. Specifically, it embeds and directly couples control, power and test signal bus pathways between the test system controller, instrument/power resource, and the UUT interface. The advancement of embedded RF printed circuit board transmission lines designs permit signals to reach 18GHz bandwidths. ATE signal integrity and repeatability under plug&play PCB construction, also dramatically improves producibility, as well as reduce integration and test acceptance times by 40%. A greater gain is achieved by through lower maintenance support costs (40%), and product technology insertion/evolution costs (60%).

The ESI specification supports/embeds three distribution subsystems within the plug&play board/wiring panel fabric. They are: (a) the Computer Control Distribution (CCD) Subsystem; (b) the Power Switching/Distribution Bus (PDB) Subsystem; and (c) the Test Signal Switching/Distribution Bus (TSD) Subsystem. The Eurocard DIN 43355 Connector serves as common interconnect between board/wiring subelements.
B. Computer Control Distribution (CCD) Subsystem Spec
Use of an advanced computer serial bus network embraces computer industry trends as reflected in Figure 5. This distribution subsystem (see Figure 6 illustrating Rapid I/O implementation), incorporates physical electrical pathways that will host any number of advanced Computer Standards, such as InfiniBand[18], Rapid I/O [19], or PCI Express [20].

Figure 5. Serial Bus Network and Distribution Subsystem Spec

This distributed network fabric will incorporate advanced transmission line technology facilitating network speeds to 12G Bytes performance. Employing parallel-multi-serial lines interface fabric, distributed multi-task control, and segregated node control points, the test system control can achieve both speeds and technology evolution without impact.

Figure 6. Serial Bus Network and Distribution Subsystem Spec

C. Power Switching/Distribution Bus (PDB) Subsystem Spec
Power Switching/Distribution Subsystem (see Figure 7), combines distributed primary 48 Volts Direct Current (VDC) Bus with DC-DC Fixed/Programmable Instrument and Power Mezzanine (IPM) Submodules. Outputs from these DC-DC IPM’s are switchable to the System Power Distribution Bus Matrix which feed system resources or Unit-Under-Test (UUT) power requirements. The power switch matrix design incorporates: (a) 30 amp [30A] High Current Primary 48VDC Feed and Multi-Return/Ground Lines; (b) 16 wire - 8 output scalable System Power Distribution Bus Matrix; and (c) Power Bus Entry Level Switching at the IPM and In-line Receiver Fixture Interface (RFI) Power Switching.

Figure 7 Power Switching/Distribution Subsystem Spec

D. Test Signal Switching/Distr Bus (TSB) Subsystem Spec
SATS defines an advanced distributed test signal switching fabric, as shown in Figure 4 and 8, that routes resource signals to a wide matrix of pin map contacts at the UUT interface. It includes: (a) Resource-to-Bus Entry Switching at the Instrument

Figure 8. Test Signal Switching/Distribution Subsystem Spec
and Power Mezzanine (IPM) Card level (located on the IPM Carrier Module); (b) **In-line Bus Matrix Switching** as dedicated resource modules (IPM Module); and (c) **Receiver-to-Bus Matrix Switching**, that directs bus signals to specific Receiver Fixture Interface (RFI) contacts. Combined with system control software, the distributed switching architecture provides considerable signal routing flexibility, wire length and pin count reduction, while simultaneously enhancing system diagnostics and fault tolerance.

**E. Scalable High Performance Test Signal Bus Matrix Pin Map**

Scalability of the embedded test signal matrix begins with 4 x 8 wire (16 transmission line signal connectivity-TLC), that can be multiplied by the integrator to serve their respective requirements. Pin Map shown in Figure 9, for a 9U high carrier module and wiring panel interconnectivity can accommodate up to 64 TLC test signal matrix, that can be in turn duplicated within the wiring panel for a number of carrier modules.

**Figure 9. Test Signal Switching/Distribution Subsystem Pin Map**

### Table 1: Test Signal Switching/Distribution Subsystem Pin Map

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**F. **EUROCARD DIN 43355 Connectors

The SATS electrical/pin map specifications builds upon the “open” design of the IEC 917 (DIN 43355) Connector style, shown in Figure 10. SATS will benefit from the well-defined and established connector design, to characterize physical intermateability properties of the interface. Utilizing predefined aspects of VME, VXI, PCI, PXI, and M-Module electrical bus/pin definitions further reinforces SATS implementation of the IEC 917/DIN 43355 electrical pin functionality.

**Figure 10. Eurocard DIN 43355 Connectors**
VIII. SATS MECHANICAL FRAMEWORKS
The SATS Frameworks Mechanical System Integration (MSI) specification describes elements related to the: (a) mainframe and engagement assembly; (b) printed wiring panels, CPC connector family and bus matrix; and (c) instrument/power mezzanine card and carrier module packaging. The SATS Frameworks is based upon VMEbus: IEC 297-3[21], IEEE 1014[22]; and VXIbus IEEE 1155 Eurocard Mechanical Packaging[23] and connector engagement/interoperability between the instrument, power, switch/matrix and cooling module.

A. SATS Mainframe
The SATS Mainframe specification adopts a modular/scalable Eurocard Packaging Standard design, that can be implemented for either a suitcase or high end ATE system application. Although, the mainframe specification permits smaller footprints, typical implementations would build upon the standard B-size depth, 3U/6U/9U VME/PCI or SATS IPM carriers modules, scaled to 9U chassis height and to 12 slots at 1.2 inch spacings (see Figure 11). When fully integrated with cooling, engagement mechanisms, and wiring panels total height can reach 14U (24.5 inches) and 17.5 inch width. Multi-mainframes may be integrated horizontally front-to-back, side-to-side, and vertical to meet various needs as illustrated in Figure 3.

B. SATS Specification Mechanical Interfaces
An alignment/engagement mechanism necessary to integrate multi-mainframes is not defined under the Specification and allows unique solutions under the Standard as competitive incentive to suppliers. Definition is however provided to assure compatible at module interface and direct mainframe pluggable integration levels. Many of these interfaces are related to connectors applied to the module and mating wiring panel. These are critical to the overall objectives in reducing or eliminating the need for wire and related costs and space. The chassis engagement mechanism and test interface may be built upon the same distributed architecture used/proven in the IEEE P1505 Receiver Fixture Interface (RFI) System.

C. SATS Wiring Panel/IPM Architecture
SATS architecture has been developed as a scalable, distributed asset structure that can be employed independently, or in concert, and matriced to a variety of Receiver Fixture Interface (RFI) I/O pins, or with other RFI Ports. The unique High Speed Serial Bus design (Infiniband, Rapid I/O, or PCI Express being considered), permits multi-tasking control at a rate as high as 13 Giga Bytes/Sec. By reducing the functional stimulus/measurement, power, and signal conditioning elements to mezzanine cards, the lowest level of integration and I/O Control (TTL Interconnect) can be implemented as was illustrated in Figure 12. At this level, development costs are marginalized to card functionality, with minimum or no costs expended for packaging, control, and external I/O. Instrument vendors who have developed products previously for the M-Module Mezzanine Specification -VITA 12[16] will see direct similarities with enhanced I/O performance, density, scaleability and common packaging.
D. Instr/Power Mezzanine Card/Carrier Module Spec

The fundamental element of the SATS Standard describes the packaging/interconnect definition of the Instrument/Power Mezzanine (IPM) Card and Carrier Module Specification. Serving as a stable modular/reconfigurable 3U/6U/9U structure, IPM/Carrier Modules (shown in Figure 12), can be developed, integrated and upgraded with minimum efforts. Packaging standards implemented under VMEbus: IEC 297-3[21], Eurocard Mechanical Packaging [17] and IEC 917/DIN 43355 [15] connector, define the mechanical/electrical interconnects between instruments, power, switch/matrix and Receiver Fixture Interface elements. As shown in Figure 13, the 3U IPM/Carrier Modules structure supports a scaleable 1.5U/3U Instrument/Power Mezzanine Card that is plugged on to a 3U Carrier Module. This IPM/Carrier structure supports a broad range of applications in which functionality can be packaged on the smallest 1.5U IPM card footprint, to a custom combined 9U card/carrier module footprint, capable of supporting a vector analyzer capability. The plug&play design also permits easy reconfigurability, expandability, and upgradeability without modification each time functional change is dictated.

Figure 13. SATS 3U Instr/Power Mezzanine Card /Carrier Module

Common carrier modules can support any number of functional I/PM Cards through standard engagement/interoperability connectorization. The Carrier Module also provides the embedded Serial Interface Control, Switch Matrix, and Test/Power Bus interface. Standardization of IEC 917 (DIN 43355) / IEC 603-2 (DIN 41612) Connector Specification at the dual interface points of the Carrier Module and mating Wiring Panels points (see Figure 9). Combined, those features create a stable structural integrity and interchangeability framework for the overall test system architecture.

As described in Figures 13 and 14, the respective 3U and 6U I/PM Card and Carrier Module Specification, IPM Cards are optimized for double side board population and center short wire connectorization to minimize signal path loss. A 3U module can support two 1.5U IPM Cards, while a 6U module supports four cards, and 9U six cards. SATS Specification permits vendors to construct 3U, 6U, and/or 9U size IPM cards to optimize functional component/circuit requirements. Custom combined card/carrier modules may be supplied by vendors, as long as the mechanical/electrical interface specifications remain compatible where the module/wiring panel integrates.

Figure 14. SATS 6U Instr/Power Mezzanine Card/Carrier Module

E. Wiring Panel /Backplane Specification

The SATS Wiring Panel/Backplane construction is a scalable structured interconnect bus design that can be hybridized/customized to meet unique test system requirements. It is the most flexible aspect of any SATS implementation serving primarily as the substitution for wire in current ATE configurations.

Digital I/O, Measurement and Stimulus Instrument/Power Modules (IPM) will apply current VXI Consortium and VXIplug&play Specifications. SATS extends these specifications by applying the DIN 43355 Connector to a transition device that converts current VXI/PXI front panels to common SATS Carrier Module I/O Specifications. The DIN Connector, shown in Figure 59, provides direct signal interfacing direct to Expansion Bay Printed Wiring Panel eliminating wiring while maintaining consistent matched impedance/signal loss pathways to and from the Instrument. Within the Expansion Bay Printed Wiring Panel (EBPWP),
SATS is defining a Common Instrument Signal Bus (CISB) that can be matriced to other instruments through physical pin mapping and/or switching. Through common output ports (pin maps of instrument front panels), categories of instruments having common pin maps can be interchanged, reconfigured/routed through CISB access to any number of points defined by the system integrator without dramatic modification of the hardware.

This Instrument Signal Bus architecture can be iterated between each chassis, as shown in Figure 4 thereby extending/expanding the routing possibilities to either the UUT or other instrumentation. This layering process provides multiple benefits in reduced footprints of the hardware, elimination of costly/performance degrading wiring, and tremendous savings in producing maintaining and upgrading the product. Instrument selection, placement, and functionality become more transparent to the system controller and/or Test Program Set (TPS) software operation, that in turn makes it more migratable between test systems.

IX. TEST SYSTEM INTERFACE TO THE UNIT-UNDER-TEST

The IEEE P1505 Receiver Fixture Interface (RFI) Standard, shown in Figure 15, has been selected for the SATS Standard. It provides a common mechanical quick disconnect for connecting large numbers of electrical signals (digital, analog, RF, power, etc.), between source and recipient of those connections. (a.k.a. General Purpose Interface, Mass Connect Interface, Test Interface System, Test Adapter, Interface Device, Interface Test Adapter). The associated Fixture is thought of as the “buffer” between the Unit-Under-Test (UUT) and Test System RFI Receiver. Its UUT-specific role being to translate standard I/O signal routing for as many as 5,600 pins offered at the Receiver to a wiring interface that directly connects to the UUT. These UUT interfaces can represent cable connectors, direct plug-in (printed circuit board edge connectors), sensor monitoring, or manual feedback from the test technician.

A. Technology Transition

SATS recognizes that solutions of the magnitude discussed will not occur overnight and transitional support must be implemented into the design of SATS to grandfather existing systems into the architecture. This will permit integrators and users to apply existing VXI instruments and cabling where direct interfaces do not exist. Transition extensions (translators) of the SATS architecture allows existing VXI/PXI front panels or cabling to couple with follow-on standard printed wiring panels connectors. When direct integration is possible (VXI/PXI front panels evolve to standard SATS), transition assemblies can be eliminated and the mechanical structure directly coupled with its mating module interface. The Augmentation bay, shown in Figure 16, reflects integration of translator modules with VXI, PXI Modules standards (conversion to cableless interconnect).

B. Hybrid SATS Standard Implementation

Hybrid SATS Standard implementation will apply current VXI Consortium and VXIplug&play Specifications into SATS wiring panels and module packaging integration. The non-defined front panels are resolved by applying the DIN 43355 Connector to a transition device that converts current VXI/PXI front panels to common SATS Carrier Module I/O Specifications. Power may be alternatively distributed from the Power Module front panel interfaces via the Augmentation Bay printed wiring panel, to either the Augmentation Bay, RFI system or UUT. These options permit more efficient use of the available power and support as backup in event module failure. Suppliers are expected to apply features that reconfigure or program outputs to meet multi-applications without augmenting resources. In standardizing on the IEC 917 DIN 43355 Connector, illustrated in Figure 5, throughout the SATS internal interfaces, common footprints and pin characteristics can be defined.
XI. SATS ATE APPLICATION

The Structured Architecture Test System (SATS) is the culmination of several years of study by both the government and industry to define a more structured approach to integrating VXI, PXI, VME, IEC, RFI subset standards into a cohesive system solution. This is done primarily to preserve test program rehostability, equipment reconfigurability, and technology evolution requirements. It further reduces customization/augmentation, test program development, and interface costs, while increasing competition.

Fundamental design is being developed through industry participation to assure product viability and long-term commitments to the standard. Several current government ATE programs such as RTCASS, ARGCS, JSF, and B1-B could benefit from the standard’s process. SATS implementation, as illustrated in Figure 17, offers a fault-tolerant test system structure, that shares 35% of the assets, matrices test signal/power bus I/O to dual multiport RFI, and reduces overall costs, build process and footprint by 50% of current ATE VXI/PXI/19” instrument hybrid system solutions. The SATS program is actively seeking integrators and instrument suppliers to refine and implement the specifica-

tion. Figure 17. SATS RTCASS, ARGCS, B1-B Implementation

• Modular/Scaleable Plug&Play Composite EnvironmentalSealed Chassis for Rugged Transportability/Easy Integration;

• External Heat Exchanger with Sealed Internal Pressurized Cooling SystemProtects Against Environment Quiet Ops;

• Cableless Modular/Scaleable Plug&Play 3U/6U/9U IPM Module and Wiring Panel Construction Offers Easy Mtgg, Maintenance, and Technology Insertion;

• Switched Matrixed Bus Integration Supports Shared Assets and Multi-Port Test Interface Access;

• High Speed Serial Bus Control Supports Point-to-Point Control at a 12GHz Rate;

• Open High Performance Receiver Fixture Interface Offers 2.0 GHz High Speed Digital, Fiber Optics, 60GHz Distributed Pin Map, and Direct Cable Access.

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David Droste is a BSEE graduate of the University of Evansville with 27 year career in military testing projects. In his twelve year tenure with the Government David led a team which produced over 100 AN/USM-465 test program sets. At Harris for 11 years, he was responsible for the development of F/A-18 TPSs and MIL-STD-2165 testability design efforts supporting Boeing on the P-3 ASW aircraft. Dave currently leads a team at PEI Electronics Inc., Huntsville Alabama, on the Re-Entry System Test Set (RSTS) Program for the Minuteman III, MK12/12A Re-Entry Systems. Mr. Droste also serves as Co-Chair for the IEEE-P1552, Structured Architecture for Test Systems (SATS) and Secretary for IEEE’s SCC20 Test and Diagnosis for Electronic Systems Standards Committee.

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