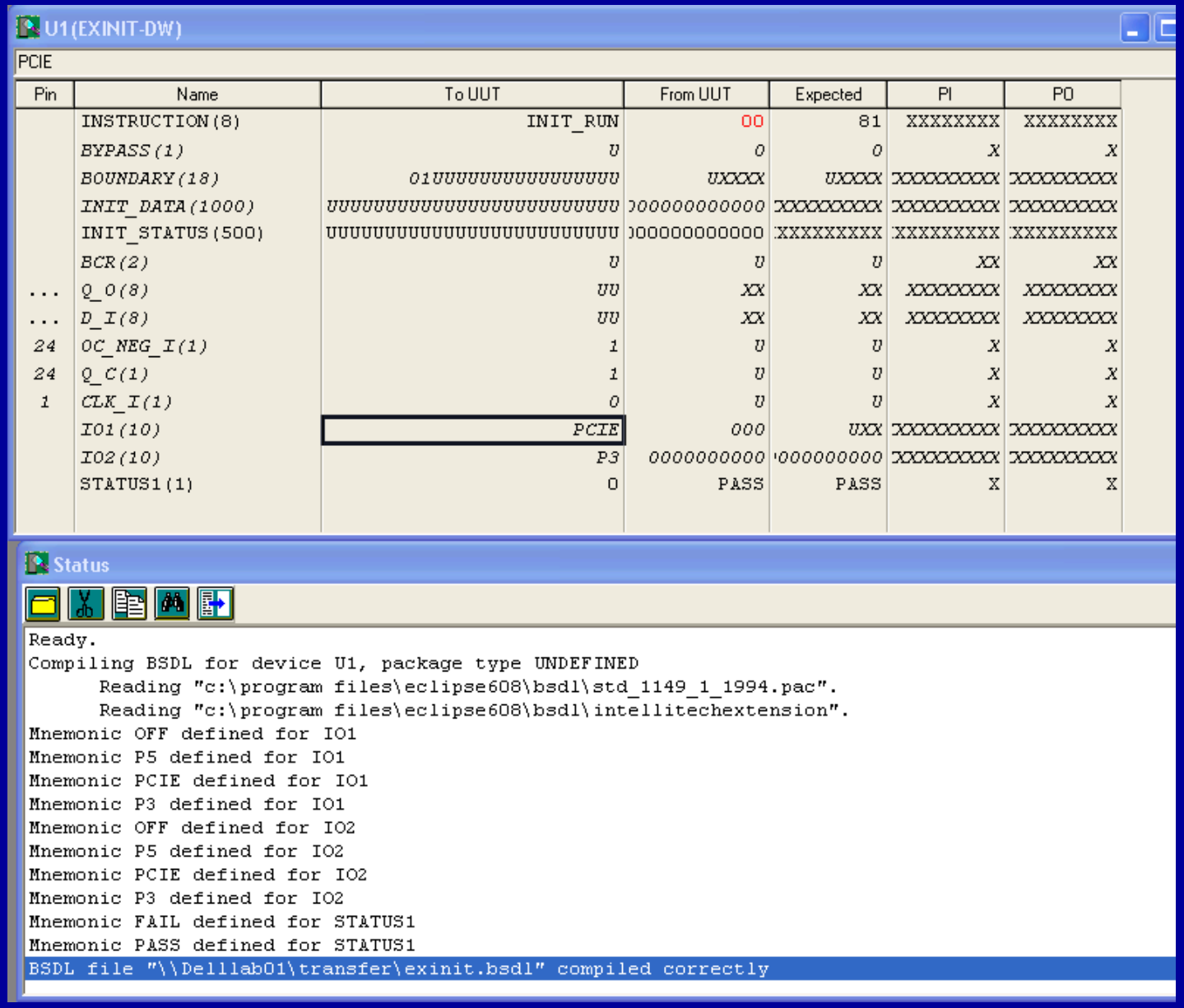
IEEE P1687 PDL

- **Level 0:**
  - **icomment** <string>
  - **ireset**
  - **iwrite** <TDR_bit|UCreg|port|pin> <value>
    - Iwrite reg|port|pin <name> <value>
    - Iwrite [pin] <name> <value> # where name is reg|port if [pin] is omitted
    - Iwrite pin::<name>|<name> <value> # where pin:: is used only for device-level package pins
  - **iread** <TDR_bit|UCreg|port|pin> <value>
  - **iapply**
  - **irun_loop tck | sck <int>**

  - **Maybe not needed for our purposes:**
  - **iscope** [pathRelToModule]
  - **iscan** <scanPort> <length> -si <siData> -so <soData>

```
"INIT_DATA[1000] (INIT_SETUP)," &    -- 1000 bit long INIT_DATA TDR
 "INIT_STATUS[500] (INIT_RUN)," &     -- 500 bit long INIT_STATUS TDR

-- BSDL extensions to describe register with more granularity

attribute REGISTER_NAME of exinit : entity is
       "IO1[10] (INIT_DATA[110,101]),"&
       "IO2[5] (INIT_DATA[210,201]),"&
       "status1[1] (INIT_STATUS[100])";

--  format register/bus:MNEMONIC (bit pattern, data, data)

attribute WRITE_MNEMONIC of exinit : entity is
      "Any:IGNORE (XXXXXX)," &
      "IO1:off (0000000000)," &
      "IO1:2P5 (0000000100)," &
      "IO1:PCIe(1100000100)," &
      "IO1:3P3 (0000000011),"&
      "IO2:off (0000000000)," &
      "IO2:2P5 (00100)," &
      "IO2:PCIe(1100000100)," &
      "IO2:3P3 (0000000011)";

attribute READ_MNEMONIC of exinit : entity is
 "Any:IGNORE (XXXXXXX)," &
"status1:fail(1)," &
"status1:pass(0)";

Attribute REGISTER_MNEMONIC
```



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IEEE P1687 examples

```
iComment  “SVF like setting of register”
# clear of init register
iWrite INIT_REG 0
# use of user defined sub registers
iWrite voltage5555 0x555
# scan the data to the target
iApply
iWrite voltage1 0b11011110011
iApply
# use of mnemonic rather than number

iWrite voltage1  PCIe
iWrite voltage2
iscan 0x15CA
iApply
iRead INIT_STATUS PCIe
```

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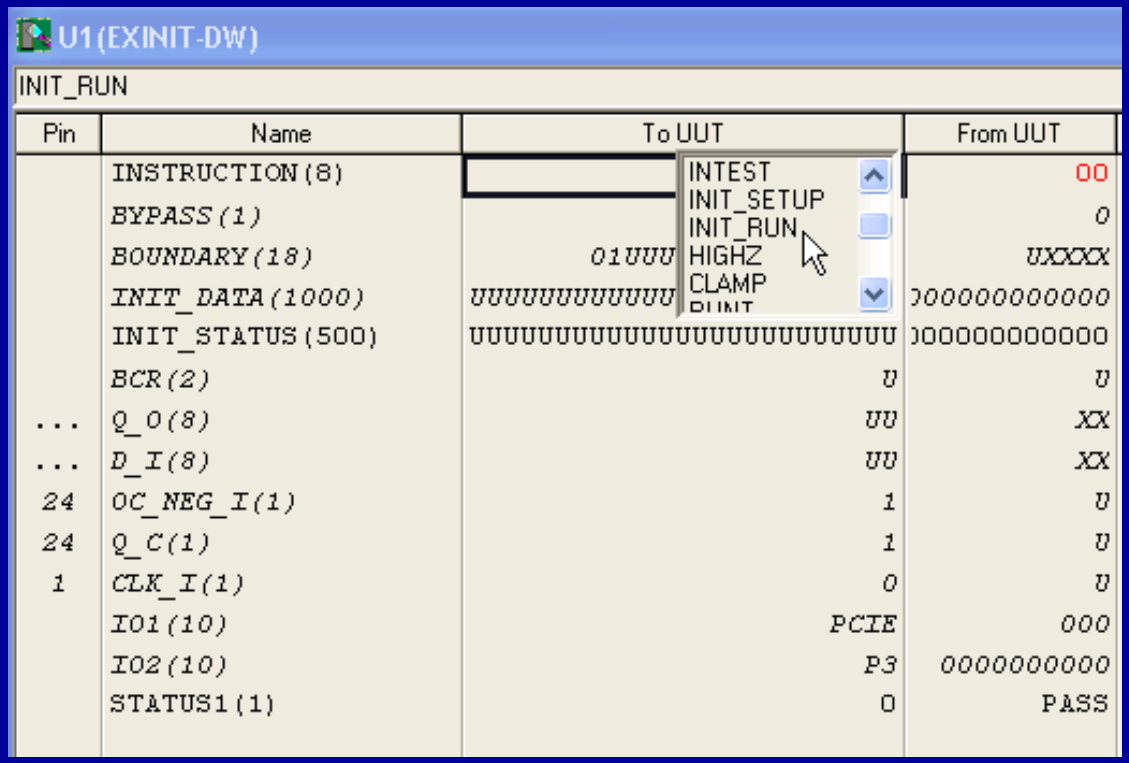
INIT_SETUP or INIT_RUN can be loaded



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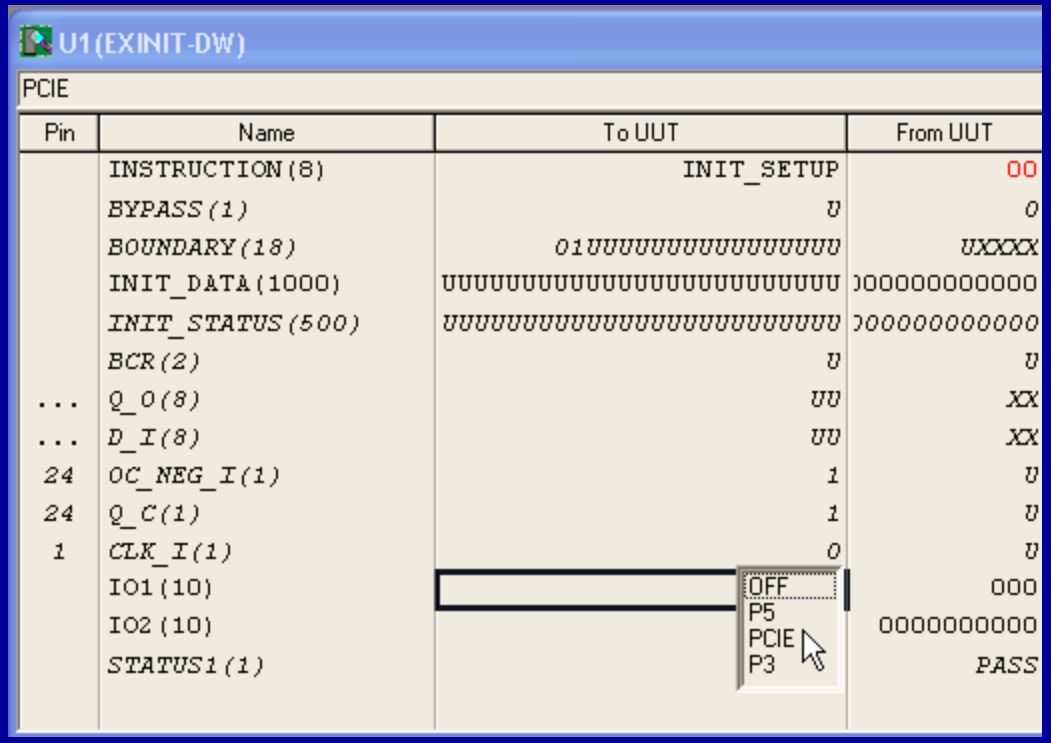
GUI enables interactive setting of I/O Via hex, binary or MNEMONIC



Note Status1 has "Pass" as a return value

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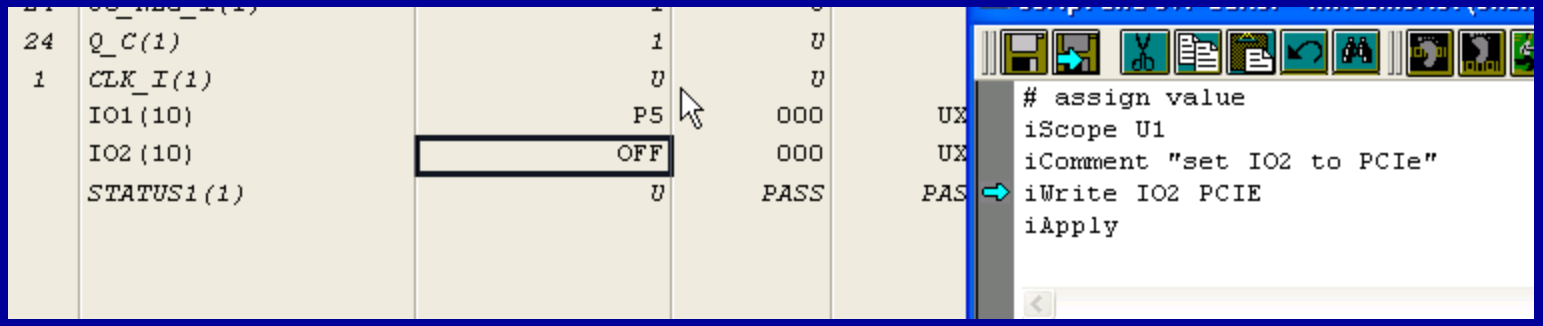
IO2 is OFF, preparing to set to PCIe



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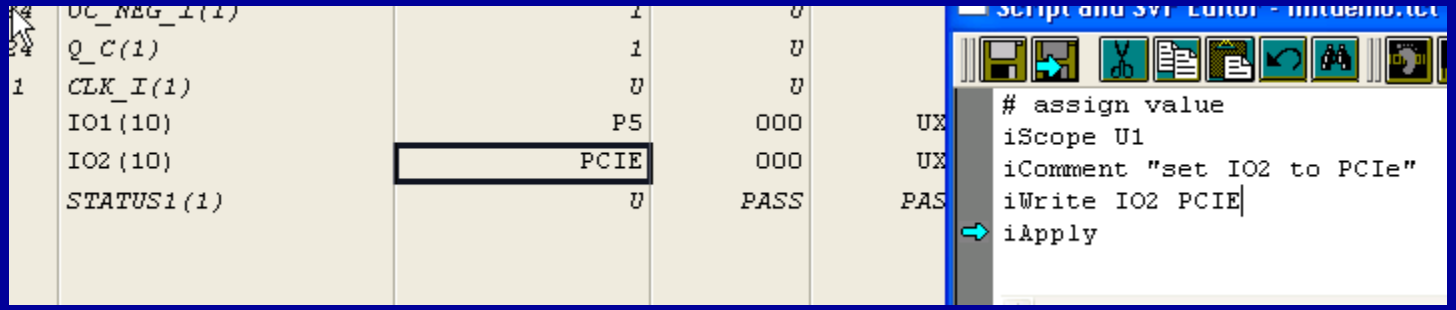
After iWrite, PCIe is now displayed
iApply will send it to the target



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Board or IC level vectors can be recorded

```
ENDDR IDLE;
ENDIR IDLE;
# set IO2 to PCIe
SDR 1000
TDI
(00000000000000000000000000000000000000000000000000000000000000000
0000000000000000000000000000000000
00000000000000000000000000000000000000000000000000000000000000000
0000000000000000000000000000000000000
0608000000000000000000000080000000000000000000000)
TDO
(00000000000000000000000000000000000000000000000000000000000000000
0000000000000000000000000000000000
00000000000000000000000000000000000000000000000000000000000000000
0000000000000000000000000000000000000
0000000000000000000000000000000000000000000000000000000000000000)
MASK
(FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF
FFFFFFFFFFFFFFFFFFFFFFFFFFFF
FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF
FFFFFFFFFFFFFFFFFFFFFFFFFFFF
FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF);
```

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Same construct but using
Ken Parker's Example

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```
attribute REGISTER_NAME of exinit : entity is
        "IO_Bank1[3] (INIT_DATA[16,18]),"&
        "IO_Bank2[3] (INIT_DATA[11,13]),"&
        "IO_Bank3[4] (INIT_DATA[5,8]),"&
        "IO_Bank4[4] (INIT_DATA[0,3]),"&
        "status1[1] (INIT_STATUS[100])";

--  format register/bus:MNEMONIC (bit pattern, data, data)

attribute TDI_MNEMONIC of exinit : entity is
       "IO_Bank1:off  (000)," &
       "IO_Bank1:3P3V (011)," &
       "IO_Bank2:off  (000)," &
       "IO_Bank2:3P3V (011)," &
       "IO_Bank3:off  (0000)," &
       "IO_Bank3:Weak_3P3   (1011)," &
       "IO_Bank3:Fast_Slew   (1010)," &
       "IO_Bank4:off  (0000)," &
       "IO_Bank4:Weak_3P3    (1011)," &
       "IO_Bank4:Fast_Slew   (1010)";


attribute TDO_MNEMONIC of exinit : entity is
"status1:fail(1)," &
"status1:pass(0)";
```

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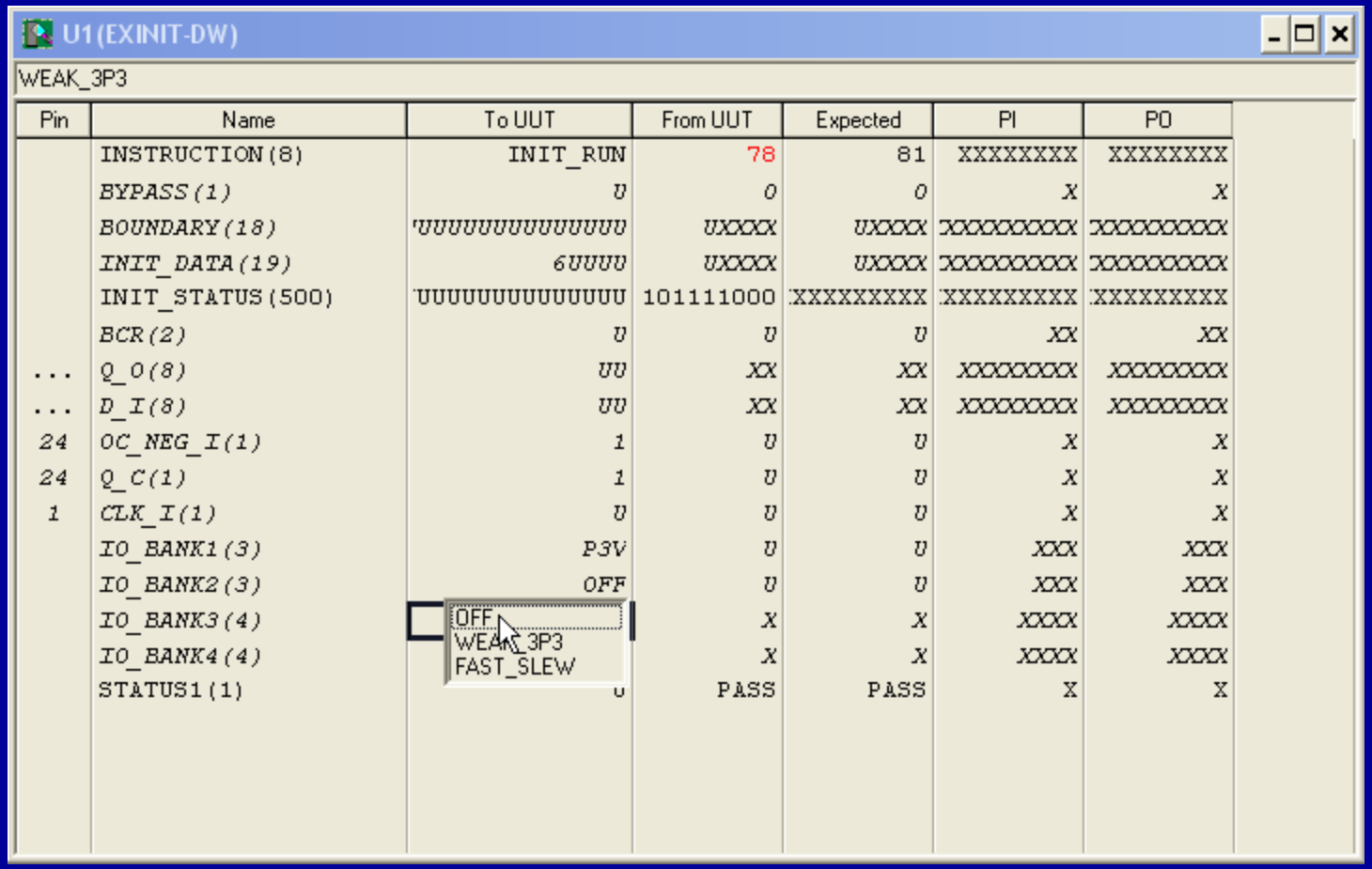

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```
iComment  “Setting of IO_Bank 1-4”

iWrite IO_Bank1  3P3
iWrite IO_Bank2  3P3
iWrite IO_Bank3  Weak_3P3
iWrite IO_Bank4  Weak_3P3
iApply
```

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