Date – 4/13/2010

Attendees: CJ Clark, Bill Tuthill, Carol Pyron, Ken Parker, Carl Barnhart, Adam Ley, Dave Dubberke, Wim Driessen, Roland Latvala, Francisco Russi, Ted Eaton, Adam Cron

Missing with pre-excuse: Heiko Ehrenberg,

Missing: Bill Eklow,

Agenda:
8:00AM PST Status on INIT

8:20AM PST Passing shorts

8:40AM PST Updating figures in standard

Minutes:
Status on INIT.
Carol -Went over rules and made some updates and sent some updates. Took inputs and discussion from last week and formalized. Made recommendation to have INIT_DATA not modified by TRST*
Carl - does this preclude setup registers?
Carol – no it does not.
Carol- added to Permissions is Capture-DR can modify INIT_DATA and what ever you capture will be scanned out during Shift-DR
Carol- Previously Capture-DR will not have any impact on INIT_DATA.
Carol -While you are in TLR a system Reset can alter the contents of the INIT_DATA TDR. This rule was highlighted as something we want to discuss..
Carl – this is normal behavior and not needed
CJ – INIT DATA Permissions. i and j are redundant to 1149.1 standard
Carol – Changed rule 3.m. at Update IR of INIT RUN instruction, INIT RUN will have control of I/Os and put into HIGHZ or CLAMP mode. INIT RUN requires TCKs for successful completion. Mission mode doesn't have control. Not sure if INIT RUN has control until enough clocks are run.
Carol - Init RUN recommendation – INIT RUN state machine should attempt to place the analog controls of the IO into the appropriate state to achieve the clamp or HIGHZ mode as soon as possible for board friendly operation.
Carol - INIT SETUP is not intrusive. Preloading conditions. Will start executing with INIT RUN but can not happen instantaneously. Requires clocks before available.
Carol -Could break out into 2 time limits.
Carl – software can not do anything with the first limit. Will have to wait until 2nd limit
Carol – Added rule – after init run is successfully completed ,the state created in the chip and on the analog controls of the is will remain active as long as the active instructions in the instruction register is either EXTEST,CLAMP,HIGHZ,INTEST,RUNBIST.

Carol - Recommendation 3.o – when invasive instructions are exited to a non-invasive state after completion of INIT_RUN the device should tend to remain in the state which is safe and cool" until reset process is initiated.
CJ – does this address Ted's needs
Ted – yes address issues

Passing shorts on self monitoring pins
Discussion on PDF that Ken had sent out on email. Titled "Falsely Passing Shorts Tests"
Ken – self monitoring BS drivers do not detect shorts by the states they capture.
Ken – drivers tend to be more equal. Example section 3. Voltage at one driver is 2v and .05v due to thresholds for receivers is at midrange voltage. Dead short won't be seen.
Ken – 2 solutions seen - silicon based or enhancing test algorithms. Future devices would be good to fix in silicon. Current devices only can be fixed by using enhanced testing algorithms.
Ken – silicon based- move threshold selection.
Change the monitor point selection. –move closer to the pin
Differentiate the Drive strength. During EXTEST drive strength would change.
Hysteretic Threshold. – voltage in from monitor point compared to voltage reference with feedback resistor and adjust threshold. Moving threshold around based on past history.

Ken – Algorithm based approach. New kind of test that looks for shorted drivers. Adjacent drivers and can be turned off with recognizable state will allow a walking test of an enabled driver in a field of disabled drivers.
CJ describes the driver-off walking 1s/0s test he developed to solve the passing shorts test. Driver-off testing was something he developed in direct contract to Wagner type patterns for detecting shorts when hysteresis is not feasible or too complex.
Ken – In the differential case. would have to monitor both legs of a differential receiver. When enabling one of the differential driver. Diff driver is disabled. Both legs are pulled high. When enabling one diff drive and all others are disabled. Looking for value in the wrong place.
CJ – Z state on monitor is of little use to help solve problem. Pull0 pull1 is of more use. Having this allows for a walking 1's and walking 0's test to work.
Ken – wants standard to recommend ways to solve the problem.. This best way to solve this is to educate designers about some of these issues.
Can't make this normative. Can only educate designers to help them do the right thing for their technology.
Ted – can these tests be done automatically if there is a control cell on driver?
Ken – if your driver isn't making the Z state than you have an opportunity to make this test. New test would be longer though.
CJ –Yes ted when you have bi-direction with a Pull1 or Pull0.
TED – can get benefit of using high z.
CJ – can't predict what the input receive value is with Z. Could be done through experimentation.

CJ – area of problems. DFT (how to describe in BSDL to avoid saying we have fault coverage where we don't) how do we limit self-monitoring output2.
CJ – is not a fan of Z state. When we capture input we get a logic value 1 or 0.
Carol – part of INIT could it control analog settings to change hysteresis. This fits in well with INIT.
CJ –Getting hysteresis cell into design is difficult.
Carol – agreed with it.
CJ - It would be easier to insert the tristate case rather than hysteresis.
Carol – Vt references can be changed during INIT DATA and INIT RUN
Ken – going to not be the desired way of setting Hysteresis.
Carl – want to discourage the Z state. Need a normative recommendation that all drivers have a zero state. At least in one of the states that it drives. Also that 2 state drivers have unbalanced drive.
Ken – Had meant no rules when talking about normative. Recommendations are ok.
CJ – agrees with Carl. It is much easier to have some of the FETs turned off or on to achieve an unbalanced state. But comes down to designer as to decide what is more difficult or best of a certain situation.
Carl – self monitoring 3 state designed as 1, 0, or pull1? just don't drive a Z.
Ken – BSDL already there. Just make people aware of situation.
Carl – need to specify whether it is a "1" dominate or a "0" that dominates. This is needed to allow consistency between different chips. Loose ability to detect shorts if one chip was dominate in 1 and the other dominate in 0
Carl – can't make normative statement on hysteretic receivers. Should be able to make a normative recommendation on "0" or over powering a "1".
CJ – why focus on over powering. why not tristate.
Carl – that is.
CJ – For one thing driving at a time.. Outputs that are tri-state
CJ – Wagners patterns are wonderful – in the low voltage area though makes sense not to take that path
Ken – dead short was a resistive short even if there was down stream receivers they may not see it. Resistive short problem happens much less. Do see resistive joint problems but that is a resistive open not short problem.

CJ – 1149.1 figures need to be updated.
CJ – Carl will you handle updating figures?
Carl – will handle figure redrawing. Just need to know which ones to do first.
CJ – work off line with Ken and see which figures are highest priority.
Carl – is also available for some editing work on INIT.
Carol- ok with that.

Meeting adjourned: 12:10 EST.

Next Meeting: April 20th, 2010 @ 11:00am EST

Current Issues listed and who will champion that issue.

1 Observe only. – Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. "No Connect" – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.