Date – 5/4/2010

Attendees: CJ Clark, Bill Tuthill, Adam Cron, Carol Pyron, Carl Barnhart, Roland Latvala, Ken Parker, Francisco Russi, Heiko Ehrenberg, Dave Dubberke,

Missing with pre-excuse:

Missing: Bill Eklow, Adam Ley, Wim Driessen,

Agenda:

Open agenda – discuss any issues that members may have

Minutes:

Carl – The INIT tiger team will drop the private email list and use .1 reflector
Going to send out clause 8 instruction rules and descriptive text.
Also send the rough draft of Annex E text that Ken is working on

Ken – not ready to discuss the revision code.

CJ – there is some time if you want begin discussions

Ken – responses vary concerning the Revision Code. Not convinced there is a solid idea of the information that we want.
Did a survey of working groups but no solid line of thinking

CJ – Seems to be some portions that are not worked out. So can understand the differing ideas people have.

CJ - we will leave it open. Still some time as we are working out INIT

Carl – the revision code in BSDL should be used at board test. For external customers.

CJ – Ted's position was that in the company that is doing the board test it is useful to know that all the locations of the company are in sync with the BSDL files.

Carl – Yes. that is where I see the greatest use. Coordinating vendors.

Francisco – Are the figures that Carl is going to be updated going to show the latest INIT registers

Carl – haven't been working on the pictures yet. Wasn't intending on redrawing architecture with INIT registers. Is this something we should do?

Francisco – yes should show the INIT registers as other figures show the other .1 registers

Carol – would agree with that

Carl – ok.. will add to the list

Ken – should Carl move to being editor as he has more time now.

CJ – is comfortable being editor right now

Ken – is Intellitech going to provide a test platform to compile and try new attributes?

CJ – yes. Will put BSDL updates to the website BSDL Compiler.

Ken – did Carl mention that we are working on BNF for INIT?
Carl – yes did mention at beginning of meeting.
Ken – have a rough draft for Carl to review.
Carol – will go back and use updated BNF to compare against example and make sure that it syncs up
CJ – how far along is Ken and Carl
Ken – Annex E - done first pass of semantic rules and more descriptions needed.
Carl – INIT - first cut of rules and more description needed.

CJ – make a motion to adjourn early. Use time to go over document from Ken and Carl.
Motion seconded

Meeting adjourned: 11:18 EST.

Next Meeting: 5/11/2010 11:00 am EST

Current Issues listed and who will champion that issue.

1 Observe only. – Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. "No Connect" – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.