Date – May 18th 2010

Attendees: CJ Clark, Bill Tuthill, Carl Barnhart, Adam Ley, Wim Driessen, Ted Eaton, Ken Parker, Roland Latvala, Dave Dubberke, Francisco Russi, Heiko Ehrenberg, Carol Pyron,

Missing with pre-excuse: Adam Cron

Missing: Bill Eklow,

Agenda:

Continue discussion on INIT.

Minutes:

Ted – what is the focus. Enabling init process? Not init architecture.

Carl – never going to get away from IO pins that affect state machine. Can't have all setup through the JTAG tap.

CJ – looking to make a consistent standard. Does realize that not all can be controlled over JTAG.

CJ – Analog voltage pins are ok. Understand that we can't control those. Want to have a defined architecture for initialization within certain boundaries. Defined sequence and defined rules.

Ted – INIT SETUP and INIT RUN instruction and init data are your defined registers.

Ted – no need to put in INIT SETUP instruction if not going to use it.

CJ – There are many reasons to add it as discussed in email.

CJ – advantages of having a single way of doing things for the end users is important.

Ted – Still going to do different things on different ASICS

CJ – understands this but trying to look at things on a global scale.

Ted – what is difficult about INIT RUN and INIT SETUP being separate.

CJ – history of errors in BSDL. Expect errors in init side files. A single consistent way will be less likely to generate errors in the side file.

CJ – side file will contain information. Won't be confused if information is missing or not there intentionally.

CJ – Die hard knowledge that we have is not pervasive throughout the industry.

Ted – agrees. But doesn't feel this is complex or confusing.

Carl – do you have examples of false pass or false fail? How does having separate from each other create bad tests

CJ – if INIT isn't done completely than test will fail.

Ted – example – has an external voltage or current source. IO will adjust analog characteristics to match. This is not Cisco's IP so can't share info. But example of why can't follow some of the requirements

CJ – no one was saying to put an A-D converter on every pin.

Ted – seems we are trying to go to far to dictate architecture. Goal is to initiate an initialization sequence for the IC.

CJ – Trying to meet requirements but it's difficult when you have to get arms around black boxes that don't describe why the functionality is needed or not.

CJ – can do anything you want functionally. Want through tap + power + clocks a basic mechanism to get chip ready for test. Trying to get correct wording for standard. No rules have been defined yet for people to follow.

CJ – trying to get meaningful "compliance" defined.

Ted – our goal is to facilitate the industries initialization sequence. Not re-architecture everyone's chips.

CJ – FPGA vendors could today claim compliance by making you program FPGA with bit stream to setup IO's

Carl – if FPGA vendors say you have to program device before test, don't see where that is illegal.

CJ – board tester needs to learn how to program FPGA?

Carol – design team should provide you with side file

CJ – lots of "shoulds" being thrown around

Carol – market will force vendors to do what is right.

CJ – market force will force chips to market but not boundary scan testing in chips.

Carol – Moving towards BC7 after fully understanding about BC6. But BC6 was legal per the standard.

CJ – exactly the point. People will do what is legal. Not what is good for the user or DFT. Just want check box next to compliant.

Carol – Freescale has a large investment in boundary scan and being compliant and goes through great effort to do so.

Carl – requirement for side file to be there. And also documented. Not sure what is missing from the rules that need adding.

CJ – INIT is the most complex part of standard and has the least amount of rules.

Ted – the group should go through rules and understand what is missing or not. Add what is required and remove what isn't needed.

Adam L – seems clear that if no parameterization (INIT SETUP) is required for INIT RUN it is superfluous to add INIT SETUP. It adds no value.

Ken – it adds more confusion to designer if there is no use for it. Software now needs to ignore it if there is no use of it.

Roland – Carol pointed out each IC vendor has the responsibility to make sure their chips work in testing environment. They have flexibility to setup board or chip. Don't think we should have to force the implementation.

Ted - Establish value on pin and run init setup and or init run and then EXTEST. Lot different than other rules forcing architecture.

Ted – need to look at rules.

Review Ken's spreadsheet on init over different devices of different init needs (emailed to group)

Ken - If in polling situation Clamp would make things easier. Supporting polling could be difficult if it takes thousand of bits to get to the couple that you need to poll on. May not be the winner you think it is.

Carl – clamp instruction is needed for chips without init

CJ – need for both.. Need it for init run

Ken – having init-run do a clamp gave more flexibility and power to keep the board safe. HIGHZ didn't give enough legs to do that.

Carl – high z takes more hardware to implement.

CJ – What is the position on INIT DATA register? Are we allowing any bits to be in INIT DATA register? Or are we creating a rule to minimize the number of redundant cells. Are people wanting to use internal scan chains or would you expect a dedicated INIT DATA register

Carl – rule written to be dedicated register. Rule says that it needs to be protected from functional logic.

Ted – what does dedicated mean.

Carl – covered in rules when it needs to be protected and when it doesn't.

Carol – in a current IC the IO config instruction is less than 200 bits wide and documented ½ to customer. Use for own internal manufacturing tests and don't want customers to change bits. Those bits not for customers are marked as Reserved.

CJ – can't tell the difference between bits that are dedicated or not then ??.

Carol – it is a dedicated register.

CJ – Any type of register that would not be allowed in INIT DATA

Carol – haven't discussed it yet..

CJ – How often are we using external device such as for training that there must be another device on the board to be completed??

Carol – voltage select pins.

Carl – doesn't involve training.

Ted – would be against allowing an external device to performing any training.

CJ – power and tap are methods for setup.

CJ – was for single instruction but may not be able to do because status register is too large.

CJ – for having both instructions, INIT RUN AND INIT SETUP.

CJ – do want to have control through tap. Seems to be some consensus on that.

CJ – need more rules to see what is allowed and what is not.

CJ – Side file is something that will have to be read and interpreted. Something that is executed. Would it be possible to have initialization in the side file including the run test loops and the polling just so it is constantly in one spot.

Ted – not all testers can do polling.. If in side file you are mandating polling.

Carol – polling isn't required.

CJ – if polling is in side file it would make it optional.

Carol – BSDL has max number of clocks to run

Carl – no arguments to have in side file. Should override the BSDL. Default max values in BSDL

CJ – would like it all in side file.

Carol – BSDL comes from IC vendor. IC vendor may not deliver a side file.

Carl- agreed that if it is in side file we should supply fields in mnemonics. If in side file you need documentation or basic defaults. Maximum goes in default.

Carol – original intention as an IC vendor was to not deliver a side file

Carl – original intent of side file was to just deliver data. Not to be an executable.
CJ – need iApply in side file. Otherwise don't know when to load data.
Ted – when you run PDL snippet you must previously load the instruction.
CJ – seems odd to manage it too different ways.
Wim – don't under stand why there is a sequence
Ted – PDL is not there to provide a sequence but used to provide mnemonics and a method to not have to write out long strings of 1's and 0's but to use meaningful names.

Ted – don't want the rules for init to be too restrictive. The ones that Carl wrote and sent in email were too restrictive.
These rules were from Carl and not from CJ. And CJ is not for all the rules that Carl had written.
CJ – Group seems to be closer to coming up with the rules than thought.

Meeting adjourned: 12:47 EST.

Next Meeting: May 25, 2010 @ 11:00am EST

Action Item by Carl to elaborate on concerns that he has with OO s on power pins and any rules that would need to be added to the standard to address those concerns.

Current Issues listed and who will champion that issue.
1 Observe only. – Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. "No Connect" – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:
- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components

- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.