Date – 8/17/2070

Attendees: CJ Clark, Bill Tuthill, Carl Barnhart , Adam Cron, Wim Driessen, Neil Jacobson, Brian Turmelle, Carol Pyron, Adam Ley, Dave Dubberke, Heiko Ehrenberg, Ted Eaton, Craig Stephan,

Missing with pre-excuse: Roland Latvala,

Missing: Ken Parker, Francisco Russi, Bill Eklow,

Agenda:
Work/Update draft
Review basic TDR example figure for hierarchical structures from Friday's Tiger Team meeting

Minutes: called to order at 11:00 EST
Update of Friday's Tiger Team Meeting

Hierarchy

CJ showed figure that he made showing hierarchy with INIT registers and boundary scan to go along with Carl's BNF for hierarchy

(figure different than what Freescale had done with sample BSDL)

Carol – this is another example which is ok. Doesn't need to be the same as Freescale

Carl – will give 3 levels of hierarchy

Figure needs some dummy bits.

Carol – one difference from Freescale is the PLL control for receiver.

CJ – may add RX pair in another example.

Will simplify the drawing after showing the initial detail

Ted – EXTEST = 1? Is this enabling VDD and GND?? (referring to CJ's figure)

CJ – way of providing the biasing without affecting the mission mode. This is what you would use for EXTEST. Not trying to illustrate different ways to set pullup and pulldowns

Ted- is this an example or rule?

CJ – example.

Carl – symbolic.

Carl – may want to drop the biasing. May unnecessarily complicate the issue

CJ - Maybe. Wanted to make the example more complete. But if it is more confusing, we can remove it.

CJ – The group should be focusing on init register and boundary register.

CJ – may want to update BSDL to show a more accurate example of Serial Protocols. Add more clock speeds ore make mnemonics more representative of real world case

Carl reviews BSDL example and hierarchy

Carl – mnemonics didn't change.

No longer having a REGISTER_SEGMENT attribute. all REGISTER_FIELDS now

Before the syntax just defined fields names. Now it is defining a register in terms of its fields.

Array vs. Scalar

Deferred array has gone away.
Uses scalar version.

Changes do not change the way PDL addresses anything.
Only requires REGISTER_MNEMONICS and REGISTER_FIELDS
Carol – thinks it looks good. This method removes some of the tediousness
CJ – need to be compatible with TCL if we want to be somewhat compatible with 1687
CJ - leaning to what is in the "PDL side" file example. (see Carl's Example file)
Adam C – wants Carl to show how it goes from a hard physical register to a soft register.
Carl - BSDL shows INIT_DATA register was defined and associated with INIT_SETUP

So REGISTER_FIELDS breaks down INIT_DATA register into fields.
Points back to lower level REGISTER_FIELDS

Adam C – questions if this is a method that the software folk will want to use.
Carl – this type of hierarchy exists in HSDL now
Ted – does every bit in the INIT_DATA need to be defined and accounted for?
Carl – no. If you don't define all of the bits, the tools will understand this and only change the ones defined since they will know the width.
Ted – how to leave out bits in the middle?
Carl – if you don't define the bits, they are not used or changed.
Ted – how to tell which bits are from the INIT_DATA register
CJ – trying to get away from explicit call-outs. Try to get to something that is not as specific as to what bit is where.
Carl has an alternate way to display the REGISTER_FIELD to make the INIT_DATA ranges less confusing.

INIT_DATA ranges will come first and then the REGISTER_FIELD definition.

```
"init_data ( "&
"((124 DOWNTO 120) IS SerDes_Channel_00 : XYZ_IO.Channel), "&
```

Vs

```
"init_data ( "&
( SerDes_Channel_00 : XYZ_IO.Channel (124 DOWNTO 120)), "&
```

Group prefers this alternate method
Carl – can use this format to build the registers

Carl will send out his example showing the new syntax after the meeting.

Meeting adjourned: 12:00 PM EST.

Next Meeting: 8/24/2010 11:00 AM EST

Action Item by Carl to elaborate on concerns that he has with OO s on power pins and any rules that would need to be added to the standard to address those concerns.

Current Issues listed and who will champion that issue.

1 Observe only. – Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. "No Connect" – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.