IEEE 1149.1 Boundary Scan Working Group Minutes

Date – 8/31/2010

Attendees: CJ Clark, Bill Tuthill, Neil Jacobson, , Ken Parker, Brian Turmelle, Craig Stephan, Carl Barnhart, Adam Ley, Carol Pyron, Ted Eaton, Francisco Russi

Missing with pre-excuse: Adam Cron, Wim Driessen,

Missing:, Heiko Ehrenberg, Dave Dubberke, Roland Latvala, Bill Eklow,

Agenda:
1. Review of Float concept (in draft) from Friday
2. Review of ROO/Discussion on fault cell
3. INIT/BSDL extensions (need a little more time to make clear in draft)

Minutes: called to order at 11:05

CJ and Ken discussed generating a diff copy of the draft to see changes between draft versions easier
CJ will "accept" all changes and make diff copies from this point forward.
        *accept is in MS WORD terms for tracking changes. Not in formalizing changes.

Float1/0 keyword
(this item was introduced and discussed in Friday's tiger team meeting)
- Added key words FLOAT0 and FLOAT1
- float_spec works like disable_spec. But only used with inputs.
- Float spec at B.8.14.1.8 (was added here in draft to keep numbering the same between IEEE 1149.1 versions
- Float_spec - Describing on input pin or clock pin, if it has a predetermined logic state than it can be described in BSDL.
- FLOAT0 for logic 0 state. FLOAT1 for logic 1
- Float_spec not allowed on 2 cell structure
- Why add to draft - Float_spec will enhance fault coverage and help ATPG tools. Will describe the chip more accurately

Ken – wants to make sure that people understand what "2 cell structures" means
CJ – already used in standard. Input cell and output cell used with control cell.
Ken – what is the combination that isn't allowed? BC7 ?
CJ – open for float on BC7. Already have a way to describe Pull1/Pull0 on bidirectional. Could be messy
CJ – 2 cell implementation. Rather than structure. Will change in draft.
CJ – on a BC7 the function type is BIDIR. So there should not be any confusion. It is the 2 cell bidirectional that needs to be specified as not allowed as it has an INPUT and OUTPUT type

CJ - Float 1 and float0 are open behavior of a pin.
Carol – what is complete definition of open?

IEEE 1149.1 JTAG working group   Thursday, September 02, 2010

Ken – opens are infinite impedance. There is a class where it is finite resistance.
CJ – there are resistive shorts and opens that are not managed well by the standard.
      Want to focus on the benefit of more accurately describing the IC.

Ted – will we add enough description to the standard so everyone will know how to check for opens?
CJ – we can address this.
Carol – what are the conditions of a test for Float0 and Float1.
Ken – does there need to be an analog component to the rule?
      How do you verify that the pin does float to a 0 or 1
Carol – How do we describe floating conditions that would result in a 0 or 1
      Can this be implemented with IO's with programmable voltages

CJ – FLOAT0 and FLOAT1 are optional and not required.

Carl – only applies on open pin?? If I have a 2 point net and the output doesn't have a pull1pull0 and input has float1 does the whole net float1 or only if it is open?
CJ – we are describing behavior of an unconnected pin
Carl – is a float1 float0 going to dictate on a 2 point net (BIDIR not driving) will BIDIR see a float value?
CJ – The float1/0 is only valid with an unconnected pin.
CJ – if BIDIR IO is a Z than yes it would follow the float value.
Carl- entire net would go to float value?
CJ – description is the behavior of an open pin. That is all we are describing.
CARL – what is the implication of that on ATPG doing board testing?
CJ – additional fault coverage that we don't get today.
CJ – there will be additional topologies that may or may not work. Up to ATPG tool to analyze that.

Ken –this is useful for pure opens. If connected, the float can't reliably predict the state of the net. Float should be specified when not connected to anything.
CJ – just describing the chip. Not describing the ATPG. Just describing the behavior of an input pin when it is open. Just allowing description to be there. Not creating rule for ATPG.

Carol – has concern on time frame of floating value? How many cycles before you check?
CJ – chip will be powered for some time before test run so that should provide enough time for float

CJ – not comfortable with the word FLOAT.
Carl – float implies a difference between float and pull
CJ – maybe what is more correct would be to change float_spec to include pull1 and pull0
Carl- what is the difference
CJ – implicit pullup and pulldown resistor VS. an intrinsic float

IEEE 1149.1 Boundary Scan Working Group Minutes

Ken – Float 1 will mean in the absence of connectivity you will get a 1

Ted – with float 0 how do you tell that from a short to ground?
Ken- this would be an ambiguous diagnostic. Could be open or short to ground.
Ted – you could do this level of diagnostic today without this description.
Ken – if input was described as an input, ATPG would expect to see a logic 1
       One difference is ATPG coverage report in the absence of float 0 would not be able to report an OPEN.

CJ – adding the key words would help improve the ATPG.

CJ – Semantic checks also added to DRAFT. B.8.14 rules X and Y

ROO
Working Group Meeting adjourned before topic could be discussed. CJ and Carl are continuing discussion and Carl will send out notes on the discussion to the group.

*Wim is out for the next 2 meetings as he is out on Holiday.

Meeting adjourned: 12:01 EST.

Next Meeting: 9/7/2010 11:00 AM EST

Action Item by Carl to elaborate on concerns that he has with OO s on power pins and any rules that would need to be added to the standard to address those concerns.

Current Issues listed and who will champion that issue.
1   Observe only. –   Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. "No Connect" – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

IEEE 1149.1 Boundary Scan Working Group Minutes

Action Items:
- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.